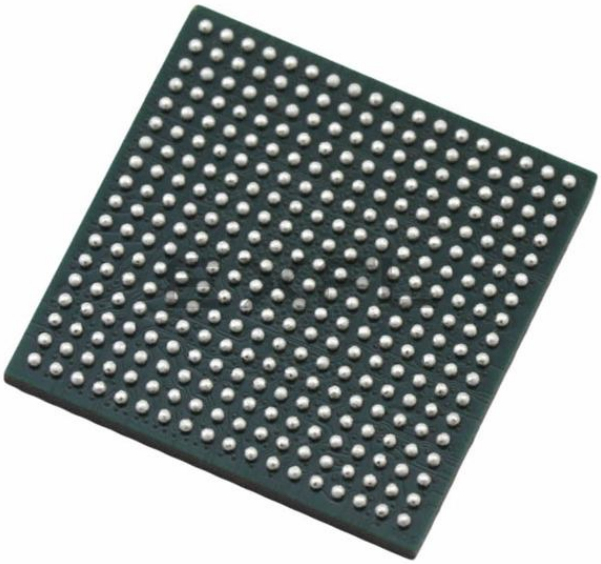

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SCI, SPI, SSP, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.05V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA, CSPBGA
Supplier Device Package	324-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21469kbcz-3

TABLE OF CONTENTS

REVISION HISTORY

3/13—Rev. A to Rev. B

Updated Development Tools 11

Revised termination description, $\overline{\text{AMI\_MS}}_{0\text{-}1}$ pin description, Chip ID description, and V_{DD_THD} pin description in Pin Function Descriptions 13

Corrected parameter from $I_{DD\text{-}INTYP}$ to I_{DD_INT} in Electrical Characteristics 20

Modified Total Power Dissipation 21

Corrected unit values for t_{CLKRST}, t_{PLLRST}, and $t_{CORERST}$ in Table 18 in Power-Up Sequencing 25

Modified note in Figure 8 in Clock Signals 26

Added footnote 3 to Table 31in AMI Read 35

Changed min value for parameter t_{DLACLK} from t_{LCLK} – 2 to 4 in Link Ports 39

Added Table 35 in Link Ports 39

Added Figure 24 in Link Ports 39

Relabeled table tile for Table 36 in Link Ports 39

Relabeled figure title for Figure 25 in Link Ports 39

Changed Max values in Table 46 in Pulse-Width Modulation (PWM) Generators 51

Added BOOT_CFG2 signal to Table 61 (CSP_BGA Ball Assignment) in CSP_BGA Ball Assignment—Automotive Models 67

Revised footnote for Table 61 (CSP_BGA Ball Assignment) in CSP_BGA Ball Assignment—Automotive Models 67

Corrected ball assignments in Figure 60 in CSP_BGA Ball Assignment—Automotive Models 67

Added BOOT_CFG2 signal to Table 62 (CSP_BGA Ball Assignment) in CSP_BGA Ball Assignment—Standard Models 70

Added footnote to Table 62 (CSP_BGA Ball Assignment) in CSP_BGA Ball Assignment—Standard Models 70

Corrected ball assignments in Figure 61 in CSP_BGA Ball Assignment—Standard Models 70

Added leaded model ADSP-21469BBC-3 to Ordering Guide 74

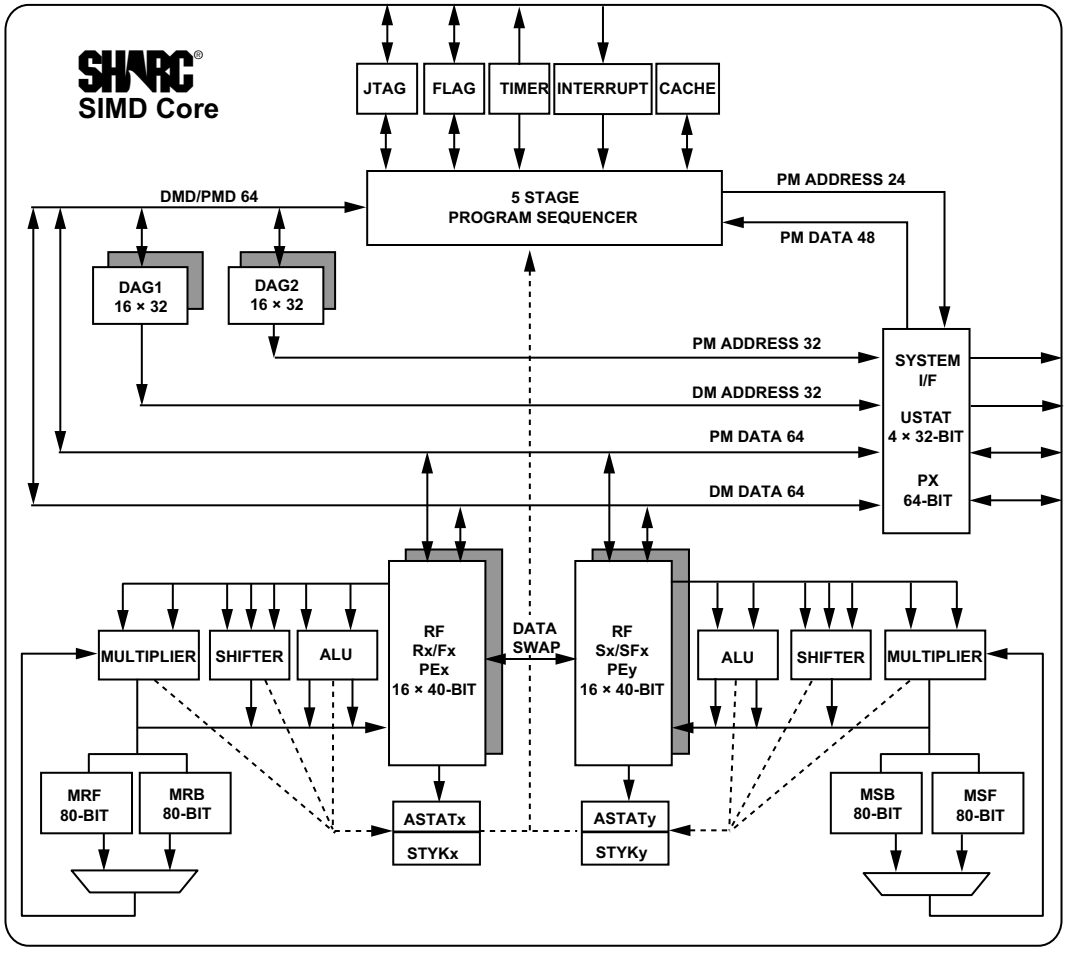


Figure 2. SHARC Core Block Diagram

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the processors support new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external DDR2 memory. Source modules need to be built using the VISA option in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The processors contain 5 Mbits of internal RAM. Each block can be configured for different combinations of code and data storage (see Table 4). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor in a single cycle.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mbits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

FAMILY PERIPHERAL ARCHITECTURE

The processors contain a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Port

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, Flash, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 2M words of external memory in bank 0 and 4M words of external memory in bank 1, bank 2, and bank 3.
- A DDR2 DRAM controller. External memory devices up to 2 Gbits in size can be supported.
- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

External Memory

The external port on the processors provide a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal DDR2 memory controller. The 16-bit DDR2 DRAM controller connects to industry-standard synchronous DRAM devices, while the second 8-bit asynchronous memory controller is intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non-DDR2 DRAM external memory address space is shown in Table 4.

Table 4. External Memory for Non-DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	2M	0x0020 0000 – 0x003F FFFF
Bank 1	4M	0x0400 0000 – 0x043F FFFF
Bank 2	4M	0x0800 0000 – 0x083F FFFF
Bank 3	4M	0x0C00 0000 – 0x0C3F FFFF

SIMD Access to External Memory

The DDR2 controller supports SIMD access on the 64-bit EPD (external port data bus) which allows to access the complementary registers on the PEy unit in the normal word space (NW). This improves performance since there is no need to explicitly load the complimentary registers as in SISD mode.

VISA and ISA Access to External Memory

The DDR2 controller also supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. Table 5 shows the address ranges for instruction fetch in each mode.

Table 5. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000 – 0x005F FFFF
VISA (SW)	10M	0x0060 0000 – 0x00FF FFFF

Shared External Memory

The processors support connection to common shared external DDR2 memory with other ADSP-2146x processors to create shared external bus processor systems. This support includes:

- Distributed, on-chip arbitration for the shared external bus
- Fixed and rotating priority bus arbitration
- Bus time-out logic
- Bus lock

Multiple processors can share the external bus with no additional arbitration logic. Arbitration logic is included on-chip to allow the connection of up to two processors. Table 10 on Page 14 provides descriptions of the pins used in multiprocessor systems.

DDR2 Support

The processors support a 16-bit DDR2 interface operating at a maximum frequency of half the core clock. Execution from external memory is supported. External memory devices up to 2 Gbits in size can be supported.

DDR2 DRAM Controller

The DDR2 DRAM controller provides a 16-bit interface to up to four separate banks of industry-standard DDR2 DRAM devices. Fully compliant with the DDR2 DRAM standard, each bank can have its own memory select line (DDR2_CS3 – DDR2_CS0), and can be configured to contain between 32 Mbytes and 256 Mbytes of memory. DDR2 DRAM external memory address space is shown in Table 6.

A set of programmable timing parameters is available to configure the DDR2 DRAM banks to support memory devices.

Table 6. External Memory for DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000 – 0x03FF FFFF
Bank 1	64M	0x0400 0000 – 0x07FF FFFF
Bank 2	64M	0x0800 0000 – 0x0BFF FFFF
Bank 3	64M	0x0C00 0000 – 0x0FFF FFFF

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21467/ADSP-21469 architecture and functionality. For detailed information on the core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

Use the termination descriptions in Table 9 when not using the DDR2 or MLB interfaces.

Warning: System designs must comply with these termination rules to avoid causing issues of quality, reliability, and power leakage at these pins.

Table 9. Unused Pin Terminations

Pin Name	Unused Termination
DDR2_CKE, $\overline{\text{DDR2\_CS}}$, DDR2_DM, DDR2_DQSx, $\overline{\text{DDR2\_DQSx}}$, $\overline{\text{DDR2\_RAS}}$, $\overline{\text{DDR2\_CAS}}$, $\overline{\text{DDR2\_WE}}$, DDR2_CLKx, $\overline{\text{DDR2\_CLKx}}$ DDR2_ADDR, DDR2_BA, DDR2_DATA	Leave floating. Internally three-state by setting the DIS_DDR2CTL bit of the DDR2CTL0 register
V_{DD_DDR2}[1]	Connect to the V_{DD_INT} supply
V_{REF}	Leave floating/unconnected
MLBCLK, MLBDAT, MLBSIG, MLBDO, MLBSO	Available on automotive models only. In standard products using silicon revision 0.2 and above connect to ground (GND). In standard products using silicon revisions previous to revision 0.2, leave these pins floating if unused.

[1] When the DDR2 controller is not used power down the receive path by setting the PWD bits of the DDR2PADCTLx register.

Table 10. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{RESET}}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$	I/O (ipu)		**Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.
BOOT_CFG_{2-0}	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is de-asserted.

The following symbols appear in the Type column of Table 10: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open-drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

Table 11. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	Internal Power
V_{DD_EXT}	P	External Power
V_{DD_A}	P	Analog Power for PLL
V_{DD_THD}	P	Thermal Diode Power; if thermal diode is not used then this pin can be left floating
V_{DD_DDR2}[1]	P	DDR2 Interface Power
V_{REF}	P	DDR2 Input Voltage Reference
GND	G	Ground
AGND	G	Analog Ground

[1] Applies to DDR2 signals.

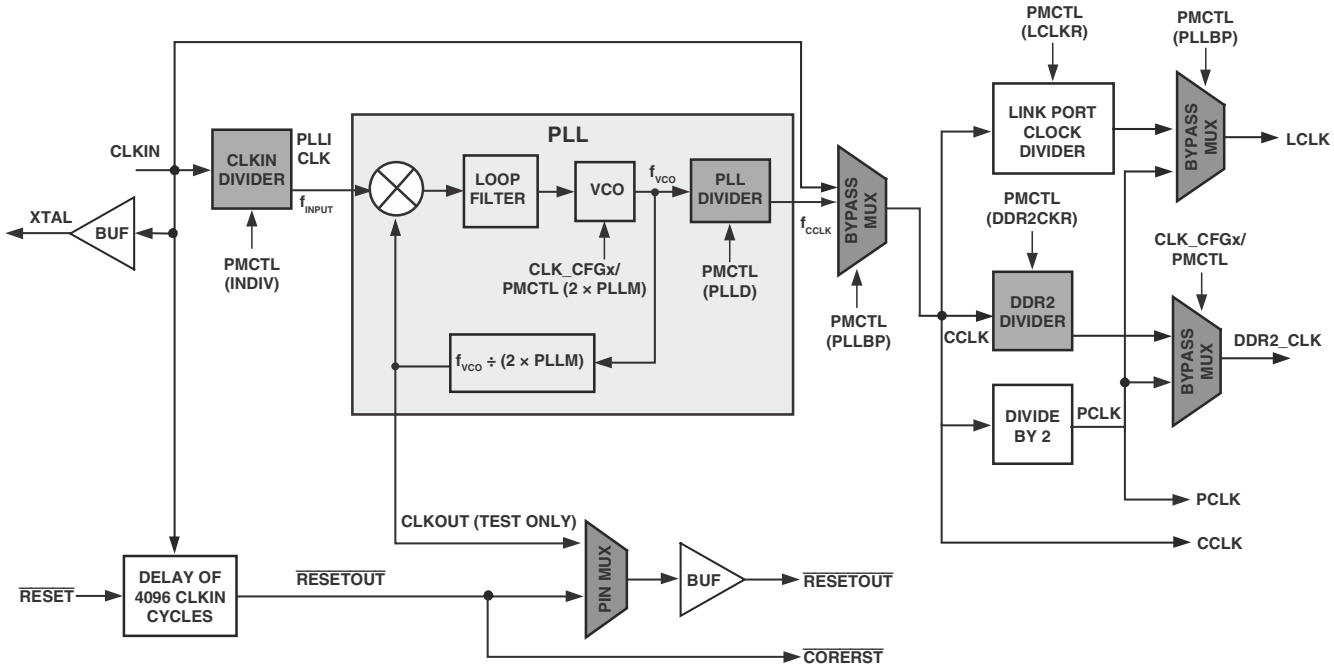


Figure 5. Core Clock and System Clock Relationship to CLKIN

Clock Input

Table 19. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	450 MHz[2] Min	450 MHz[2] Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	15[3]	100	13.26	100	ns
t_{CKL}	CLKIN Width Low	7.5	45	6.63	45	ns
t_{CKH}	CLKIN Width High	7.5	45	6.63	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3[4]		3[4]	ns
t_{CCLK}[5]	CCLK Period	2.5	10	2.22	10	ns
f_{VCO}[6]	VCO Frequency	200	900	200	900	MHz
t_{CKJ}[7, 8]	CLKIN Jitter Tolerance	–250	+250	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 74.
[2] Applies to all 450 MHz models. See Ordering Guide on Page 74.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[4] Guaranteed by simulation but not tested on silicon.
[5] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[6] See Figure 5 on Page 24 for VCO diagram.
[7] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[8] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

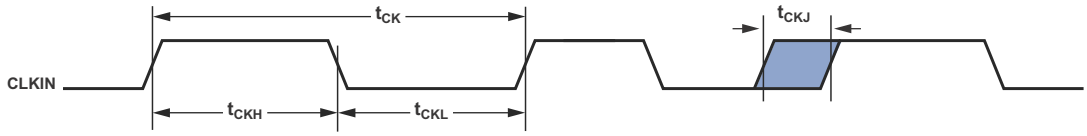


Figure 7. Clock Input

Clock Signals

The processor can use an external clock or a crystal. See the CLKIN pin description in Table 10. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz).

To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

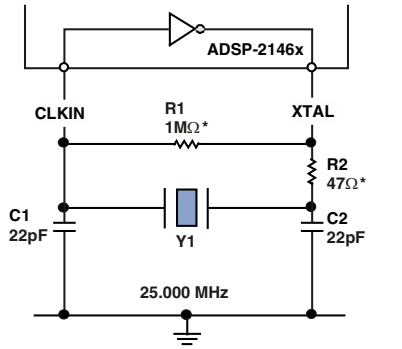


Figure 8. Recommended Circuit for Fundamental Mode Crystal Operation

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 22. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

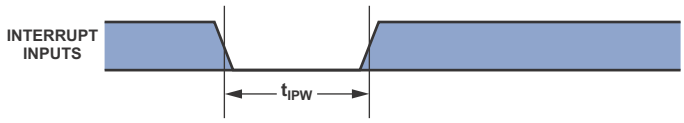


Figure 11. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 23. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1$		ns

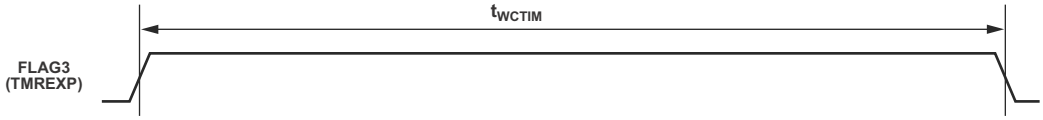


Figure 12. Core Timer

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 31. Memory Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2, 3]		W + t_{DDR2_CLK} −5.4	ns
t_{DRLD}	$\overline{\text{AMI\_RD}}$ Low to Data Valid[1]		W – 3.2	ns
t_{SDS}	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.5		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High[4, 5]	0		ns
t_{DAAK}	AMI_ACK Delay from Address, Selects[2, 6]		t_{DDR2_CLK} −9.5 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low[4]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RH + 0.20		ns
t_{DARL}	Address Selects to $\overline{\text{AMI\_RD}}$ Low[2]	t_{DDR2_CLK} – 3.8		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	HI + t_{DDR2_CLK} – 1		ns

W = (number of wait states specified in AMICTLx register) × t_{DDR2_CLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{DDR2_CLK}
Where PREDIS = 0
HI = RHC: Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{DDR2_CLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{DDR2_CLK})): Read to Write from same or different bank
HI = RHC + (3 × tDDR2_CLK): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{DDR2_CLK})): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{DDR2_CLK}H = (number of hold cycles specified in AMICTLx register) × tDDR2_CLK

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 62 for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).

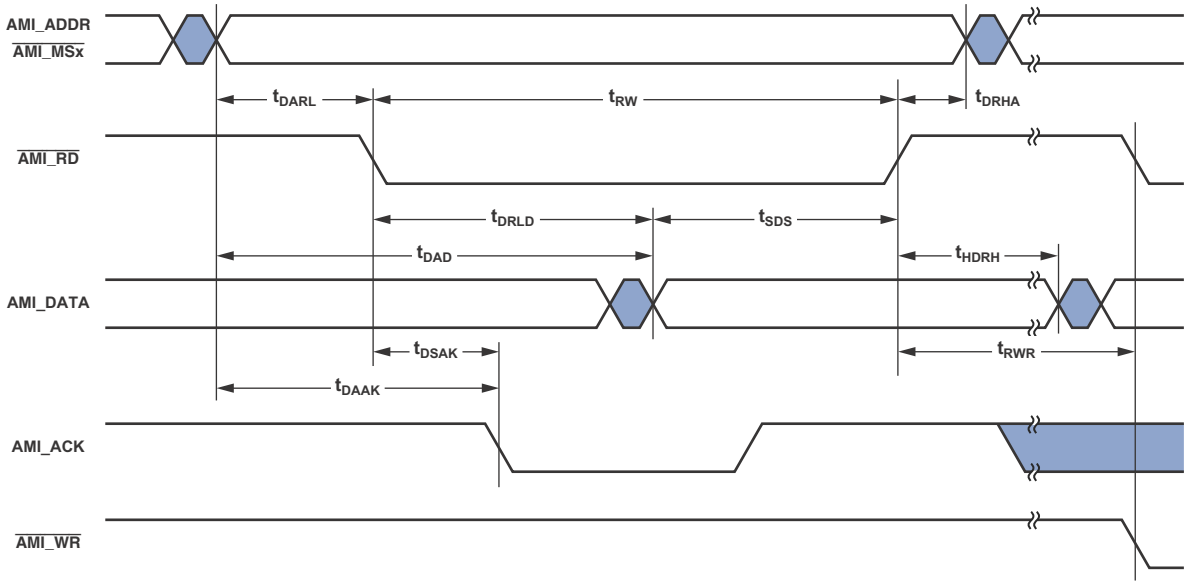
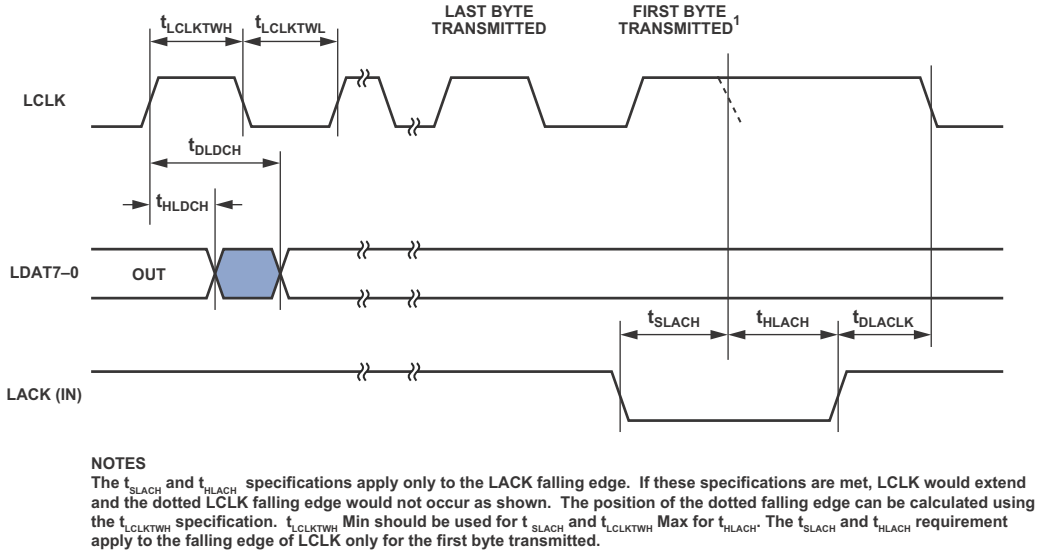


Figure 20. AMI Read



NOTES
The t_{SLACH} and t_{HLACH} specifications apply only to the LACK falling edge. If these specifications are met, LCLK would extend and the dotted LCLK falling edge would not occur as shown. The position of the dotted falling edge can be calculated using the $t_{LCLKTWH}$ specification. $t_{LCLKTWH}$ Min should be used for t_{SLACH} and $t_{LCLKTWH}$ Max for t_{HLACH}. The t_{SLACH} and t_{HLACH} requirement apply to the falling edge of LCLK only for the first byte transmitted.

Figure 24. Link Ports—Transmit (Bit 6 Cleared)

The data in Table 36 and timing information in Figure 25 apply when the LSYNC_EN bit (bit 6 in the LCTLx register) is set.

Table 36. Link Ports—Transmit (Bit 6 Set)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	8.5		ns
t_{HLACH}	LACK Hold After LCLK High	0		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		1	ns
t_{HLDCH}	Data Hold After LCLK High	–1		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5 \times t_{LCLK} - 0.4$	$0.6 \times t_{LCLK} + 0.4$[1]	ns
$t_{LCLKTWH}$	LCLK Width High	$0.4 \times t_{LCLK} - 0.4$[1]	$0.5 \times t_{LCLK} + 0.4$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$0.5 \times t_{LCLK} + 4$	$1.5 \times t_{LCLK} + 4$	ns

[1] For 1:2.5 ratio. For other ratios this specification is $0.5 \times t_{LCLK} - 1$.

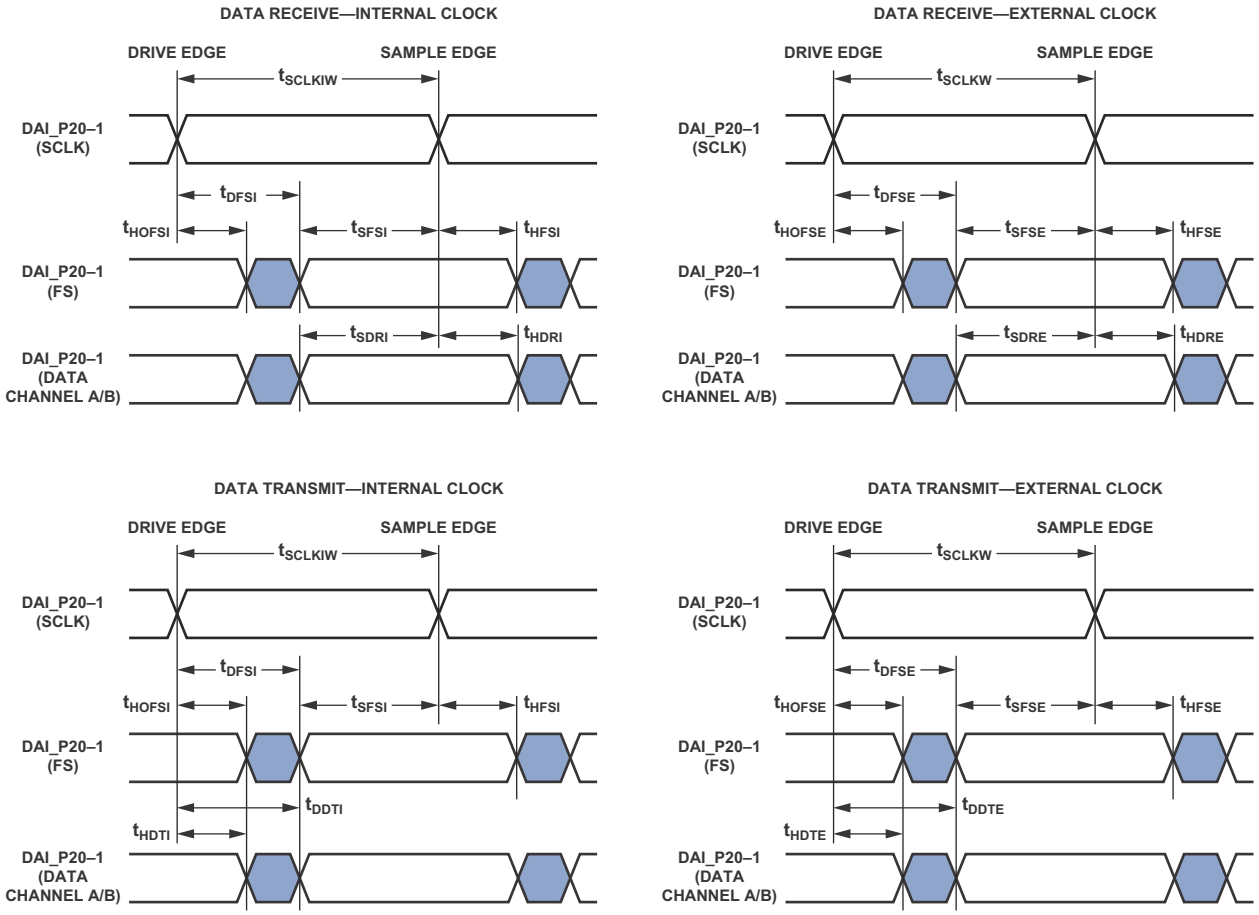


Figure 26. Serial Ports

Sample Rate Converter—Serial Input Port

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 44 are valid at the DAI_P20–1 pins.

Table 44. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

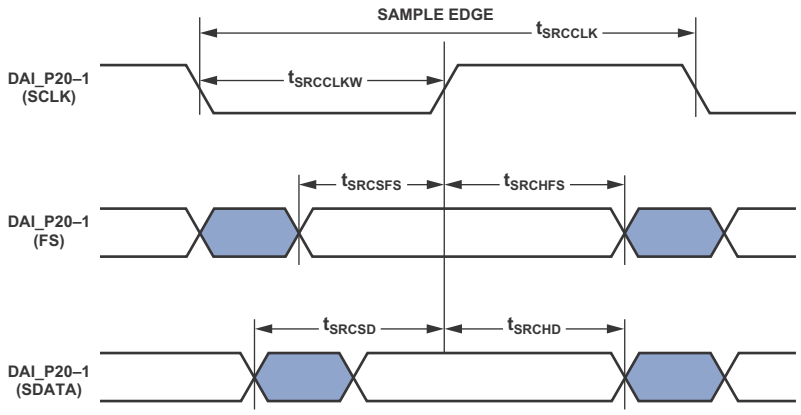


Figure 32. ASRC Serial Input Port Timing

Media Local Bus

All the numbers given are applicable for all speed modes (1024 FS, 512 FS, and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

Table 55. MLB Interface, 3-Pin Specifications

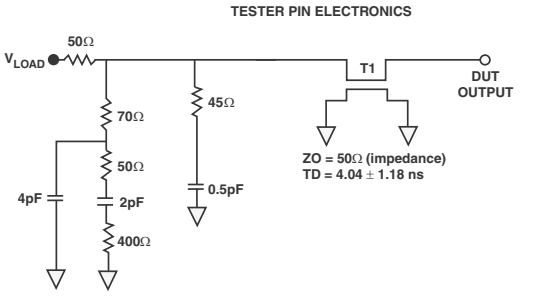
Parameter		Min	Typ	Max	Unit
3-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024 FS		20.3		ns
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024 FS	6.1			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	1024 FS	9.3			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
T_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024 FS			0.7	ns p-p
	512 FS/256 FS			2.0	ns p-p
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	1			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-state	0		15	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024 FS	2			ns
	512 FS/256 FS	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024 FS			40	pf
	512 FS/256 FS			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in nanoseconds peak-to-peak (ns p-p).
[2] The board must be designed to ensure that the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 20 on Page 27 through Table 57 on Page 61. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 46.

Timing is measured on signals when they cross the V_{MEAS} level as described in Figure 47. All delays (in nanoseconds) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS}. The value of V_{MEAS} is 1.5 V for non-DDR pins and 0.9 V for DDR pins.



NOTES:
THE WORST-CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 46. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 47. Voltage Reference Levels for AC Measurements

OUTPUT DRIVE CURRENTS

Figure 48 and Figure 49 shows typical I-V characteristics for the output drivers of the processor, and Table 58 shows the pins associated with each driver. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 58. Driver Types

Driver Type	Associated Pins
A	LACK1–0, LDAT0[7:0], LDAT1[7:0], MLBCLK, MLBDAT, MLBDO, MLBSIG, MLBSO, AMI_ACK, AMI_ADDR23–0, AMI_DATA7–0, $\overline{\text{AMI\_MS1–0}}$, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, DAI_P, DPI_P, $\overline{\text{EMU}}$, FLAG3–0, RESETOUT, TDO
B	LCLK1–0
C	DDR2_ADDR15–0, DDR2_BA2–0, $\overline{\text{DDR2\_CAS}}$, DDR2_CKE, $\overline{\text{DDR2\_CS3–0}}$, DDR2_DATA15–0, DDR2_DM1–0, DDR2_ODT, $\overline{\text{DDR2\_RAS}}$, $\overline{\text{DDR2\_WE}}$
D (TRUE)	DDR2_CLK1–0, DDR2_DQS1–0
D (COMP)	$\overline{\text{DDR2\_CLK1–0}}$, $\overline{\text{DDR2\_DQS1–0}}$

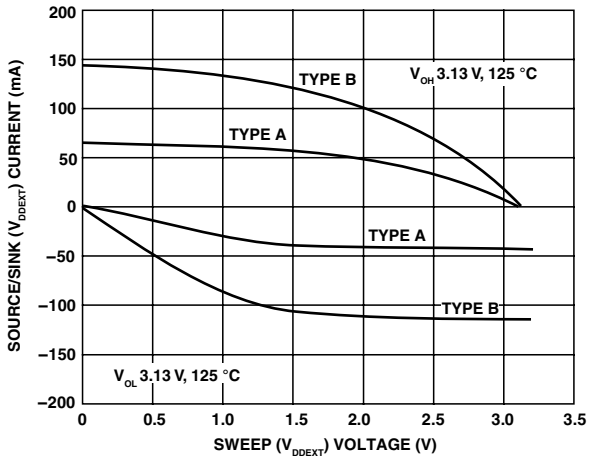


Figure 48. Output Buffer Characteristics (Worst-Case Non-DDR2)

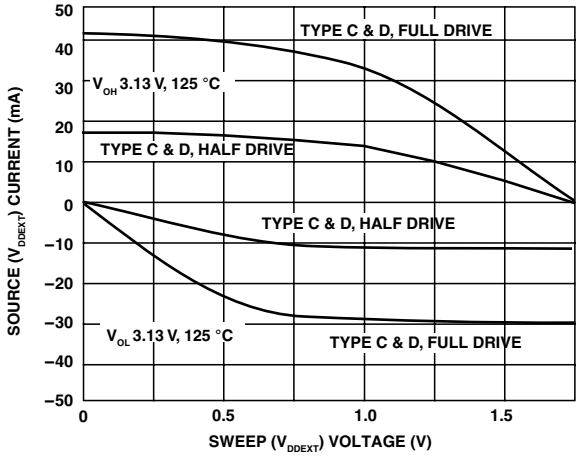


Figure 49. Output Buffer Characteristics (Worst-Case DDR2)

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Table 58). Figure 54 through Figure 59 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 50 through Figure 59 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

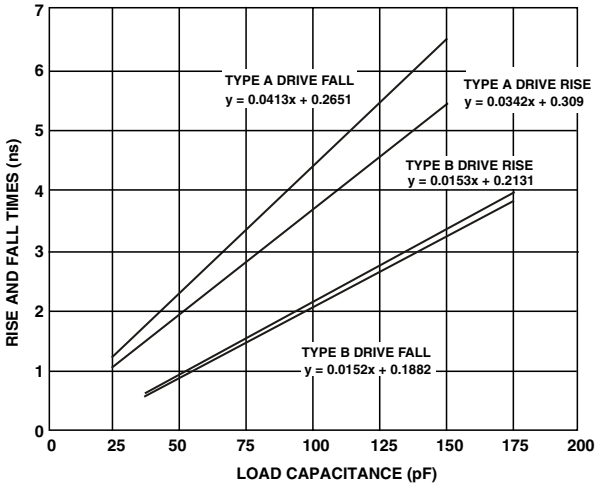


Figure 50. Typical Output Rise/Fall Time Non-DDR2 (20% to 80%, V_{DD_EXT} = Max)

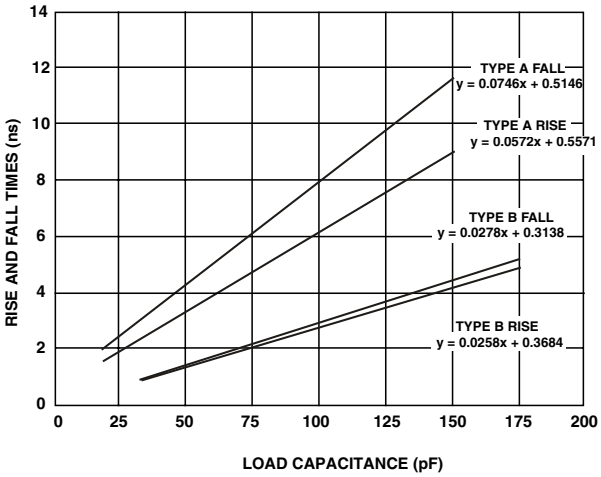


Figure 51. Typical Output Rise/Fall Time Non-DDR2 (20% to 80%, V_{DD_EXT} = Min)

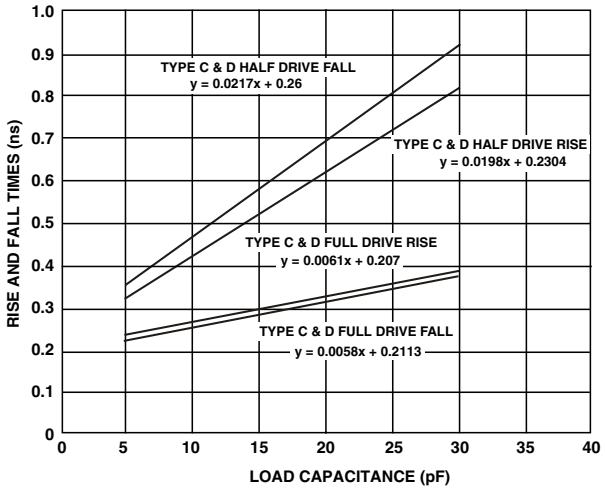


Figure 52. Typical Output Rise/Fall Time DDR2 (20% to 80%, V_{DD_EXT} = Max)

CSP_BGA BALL ASSIGNMENT—STANDARD MODELS

Table 62 lists the standard model CSP_BGA ball assignments by signal.

Table 62. CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
AGND	H02	BOOT_CFG2	H03	DDR2_BA0	C18	DPI_P03	T01
AMI_ACK	R10	CLK_CFG0	G01	DDR2_BA1	C17	DPI_P04	R01
AMI_ADDR0	V16	CLK_CFG1	G02	DDR2_BA2	B18	DPI_P05	P01
AMI_ADDR01	U16	CLKIN	L01	$\overline{\text{DDR2\_CAS}}$	C07	DPI_P06	P02
AMI_ADDR02	T16	DAI_P01	R06	DDR2_CKE	E01	DPI_P07	P03
AMI_ADDR03	R16	DAI_P02	V05	$\overline{\text{DDR2\_CLK0}}$	A07	DPI_P08	P04
AMI_ADDR04	V15	DAI_P03	R07	DDR2_CLK0	B07	DPI_P09	N01
AMI_ADDR05	U15	DAI_P04	R03	$\overline{\text{DDR2\_CLK1}}$	A13	DPI_P10	N02
AMI_ADDR06	T15	DAI_P05	U05	DDR2_CLK1	B13	DPI_P11	N03
AMI_ADDR07	R15	DAI_P06	T05	$\overline{\text{DDR2\_CS0}}$	C01	DPI_P12	N04
AMI_ADDR08	V14	DAI_P07	V06	$\overline{\text{DDR2\_CS1}}$	D01	DPI_P13	M03
AMI_ADDR09	U14	DAI_P08	V02	$\overline{\text{DDR2\_CS2}}$	C02	DPI_P14	M04
AMI_ADDR10	T14	DAI_P09	R05	$\overline{\text{DDR2\_CS3}}$	D02	$\overline{\text{EMU}}$	K02
AMI_ADDR11	R14	DAI_P10	V04	DDR2_DATA0	B02	FLAG0	R08
AMI_ADDR12	V13	DAI_P11	U04	DDR2_DATA01	A02	FLAG1	V07
AMI_ADDR13	U13	DAI_P12	T04	DDR2_DATA02	B03	FLAG2	U07
AMI_ADDR14	T13	DAI_P13	U06	DDR2_DATA03	A03	FLAG3	T07
AMI_ADDR15	R13	DAI_P14	U02	DDR2_DATA04	B05	GND	A01
AMI_ADDR16	V12	DAI_P15	R04	DDR2_DATA05	A05	GND	A18
AMI_ADDR17	U12	DAI_P16	V03	DDR2_DATA06	B06	GND	C04
AMI_ADDR18	T12	DAI_P17	U03	DDR2_DATA07	A06	GND	C06
AMI_ADDR19	R12	DAI_P18	T03	DDR2_DATA08	B08	GND	C08
AMI_ADDR20	V11	DAI_P19	T06	DDR2_DATA09	A08	GND	D05
AMI_ADDR21	U11	DAI_P20	T02	DDR2_DATA10	B09	GND	D07
AMI_ADDR22	T11	DDR2_ADDR0	D13	DDR2_DATA11	A09	GND	D09
AMI_ADDR23	R11	DDR2_ADDR01	C13	DDR2_DATA12	A11	GND	D10
AMI_DATA0	U18	DDR2_ADDR02	D14	DDR2_DATA13	B11	GND	D17
AMI_DATA1	T18	DDR2_ADDR03	C14	DDR2_DATA14	A12	GND	E03
AMI_DATA2	R18	DDR2_ADDR04	B14	DDR2_DATA15	B12	GND	E05
AMI_DATA3	P18	DDR2_ADDR05	A14	DDR2_DM0	C03	GND	E12
AMI_DATA4	V17	DDR2_ADDR06	D15	DDR2_DM1	C11	GND	E13
AMI_DATA5	U17	DDR2_ADDR07	C15	DDR2_DQS0	A04	GND	E16
AMI_DATA6	T17	DDR2_ADDR08	B15	$\overline{\text{DDR2\_DQS0}}$	B04	GND	F01
AMI_DATA7	R17	DDR2_ADDR09	A15	DDR2_DQS1	A10	GND	F02
$\overline{\text{AMI\_MS0}}$	T10	DDR2_ADDR10	D16	$\overline{\text{DDR2\_DQS1}}$	B10	GND	F04
$\overline{\text{AMI\_MS1}}$	U10	DDR2_ADDR11	C16	DDR2_ODT	B01	GND	F14
$\overline{\text{AMI\_RD}}$	J04	DDR2_ADDR12	B16	$\overline{\text{DDR2\_RAS}}$	C09	GND	F16
$\overline{\text{AMI\_WR}}$	V10	DDR2_ADDR13	A16	$\overline{\text{DDR2\_WE}}$	C10	GND	G05
BOOT_CFG0	J02	DDR2_ADDR14	B17	DPI_P01	R02	GND	G07
BOOT_CFG1	J03	DDR2_ADDR15	A17	DPI_P02	U01	GND	G08

Table 62. CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
GND	G09	GND	M09	TMS	K16	V_{DD_INT}	E08
GND	G10	GND	M10	$\overline{TRST}$	N15	V_{DD_INT}	E09
GND	G11	GND	M11	VDD_A	H01	V_{DD_INT}	E14
GND	G12	GND	M12	V_{DD_DDR2}	C05	V_{DD_INT}	E15
GND	G15	GND	N14	V_{DD_DDR2}	C12	V_{DD_INT}	F06
GND	H04	GND	N17	V_{DD_DDR2}	D03	V_{DD_INT}	F07
GND	H07	GND	P05	V_{DD_DDR2}	D06	V_{DD_INT}	F08
GND	H08	GND	P07	V_{DD_DDR2}	D08	V_{DD_INT}	F09
GND	H09	GND	P09	V_{DD_DDR2}	D18	V_{DD_INT}	F10
GND	H10	GND	P11	V_{DD_DDR2}	E02	V_{DD_INT}	F11
GND	H11	GND	P13	V_{DD_DDR2}	E04	V_{DD_INT}	F12
GND	H12	GND	R09	V_{DD_DDR2}	E07	V_{DD_INT}	F13
GND	J01	GND	V01	V_{DD_DDR2}	E10	V_{DD_INT}	G06
GND	J07	GND	V18	V_{DD_DDR2}	E11	V_{DD_INT}	G13
GND	J08	GND/ID0[1]	G03	V_{DD_DDR2}	E17	V_{DD_INT}	H05
GND	J09	GND/ID1[1]	G04	V_{DD_DDR2}	F03	V_{DD_INT}	H06
GND	J10	LACK_0	K17	V_{DD_DDR2}	F05	V_{DD_INT}	H13
GND	J11	LACK_1	P17	V_{DD_DDR2}	F15	V_{DD_INT}	H14
GND	J12	LCLK_0	J18	V_{DD_DDR2}	G14	V_{DD_INT}	J06
GND	J14	LCLK_1	N18	V_{DD_DDR2}	G16	V_{DD_INT}	J13
GND	J17	LDAT0_0	E18	V_{DD_EXT}	H15	V_{DD_INT}	K06
GND	K03	LDAT0_1	F17	V_{DD_EXT}	H18	V_{DD_INT}	K13
GND	K04	LDAT0_2	F18	V_{DD_EXT}	J05	V_{DD_INT}	L06
GND	K05	LDAT0_3	G17	V_{DD_EXT}	J15	V_{DD_INT}	L13
GND	K07	LDAT0_4	G18	V_{DD_EXT}	K14	V_{DD_INT}	M06
GND	K08	LDAT0_5	H16	V_{DD_EXT}	L05	V_{DD_INT}	M13
GND	K09	LDAT0_6	H17	V_{DD_EXT}	M14	V_{DD_INT}	N06
GND	K10	LDAT0_7	J16	V_{DD_EXT}	M18	V_{DD_INT}	N07
GND	K11	LDAT1_0	K18	V_{DD_EXT}	N05	V_{DD_INT}	N08
GND	K12	LDAT1_1	L16	V_{DD_EXT}	P06	V_{DD_INT}	N09
GND	L02	LDAT1_2	L17	V_{DD_EXT}	P08	V_{DD_INT}	N13
GND	L03	LDAT1_3	L18	V_{DD_EXT}	P10	V_{DD_THD}	N10
GND	L04	LDAT1_4	M16	V_{DD_EXT}	P12	V_{REF}	D04
GND	L07	LDAT1_5	M17	V_{DD_EXT}	P14	V_{REF}	D11
GND	L08	LDAT1_6	N16	V_{DD_EXT}	P15	XTAL	K01
GND	L09	LDAT1_7	P16	V_{DD_EXT}	T08		
GND	L10	$\overline{RESET}$	M01	V_{DD_EXT}	T09		
GND	L11	$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	M02	V_{DD_EXT}	U09		
GND	L12	TCK	K15	V_{DD_EXT}	V09		
GND	L14	TDI	L15	V_{DD_EXT}/$\overline{BR1}$[1]	V08		
GND	M05	TDO	M15	V_{DD_EXT}/$\overline{BR2}$[1]	U08		
GND	M07	THD_M	N12	V_{DD_INT}	D12		
GND	M08	THD_P	N11	V_{DD_INT}	E06		

[1] This pin can be used for shared DDR2 memory between two processors. If shared memory functionality is not used then $\overline{BRx}$ pins should be tied to V_{DD_EXT} and IDx pins should be tied to GND. Table 10 on Page 14 for appropriate connections.