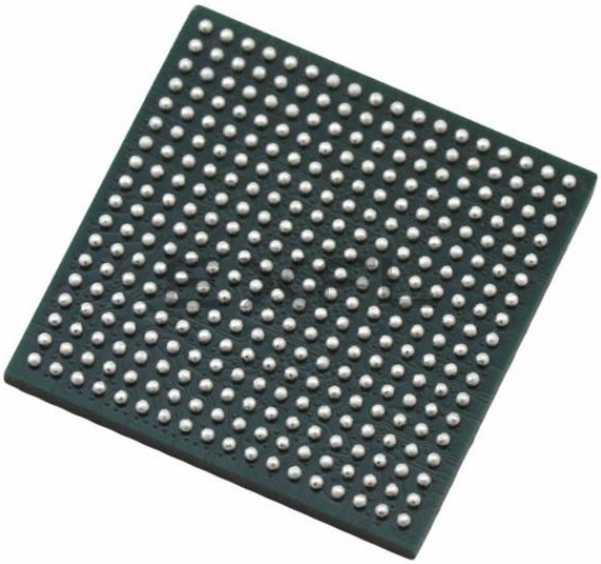

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SCI, SPI, SSP, UART/USART
Clock Rate	450MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA, CSPBGA
Supplier Device Package	324-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21469kbcz-4

GENERAL DESCRIPTION

The ADSP-21467/ADSP-21469 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. These 32-bit/40-bit floating-point processors are optimized for high performance audio applications with their large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications/peripheral interfaces (DAI/DPI).

Table 1 shows performance benchmarks for the processor, and Table 2 shows the product's features.

Table 1. Processor Benchmarks

Benchmark Algorithm	Speed (at 450 MHz)
1024 Point Complex FFT (Radix 4, with Reversal)	20.44 µs
FIR Filter (Per Tap)[1]	1.11 ns
IIR Filter (Per Biquad)[1]	4.43 ns
Matrix Multiply (Pipelined)	
[3 × 3] × [3 × 1]	10.0 ns
[4 × 4] × [4 × 1]	17.78 ns
Divide (y/x)	6.67 ns
Inverse Square Root	10.0 ns

[1] Assumes two files in multichannel SIMD mode

Table 2. SHARC Family Features

Feature	ADSP-21467	ADSP-21469
Maximum Frequency	450 MHz	
RAM	5 Mbits	
ROM	4 Mbits	N/A
Audio Decoders in ROM[1]	Yes	No
DTCP Hardware Accelerator[2]	No	
Pulse-Width Modulation	Yes	
S/PDIF	Yes	
DDR2 Memory Interface	Yes	
DDR2 Memory Bus Width	16 Bits	
Shared DDR2 External Memory	Yes	
Direct DMA from SPORTs to External Memory	Yes	
FIR, IIR, FFT Accelerator	Yes	
MLB Interface	Automotive Models Only	
IDP	Yes	
Serial Ports	8	
DAI (SRU)/DPI (SRU2)	20/14 pins	
UART	1	
Link Ports	2	
AMI Interface with 8-Bit Support	Yes	
SPI	2	
TWI	Yes	
SRC Performance	–128 dB	
Package	324-Ball CSP_BGA	

[1] Factory programmed ROM includes: Dolby AC-3 5.1 Decode, Dolby Pro Logic IIx, Dolby Intelligent Mixer (eMix), Dolby Volume postprocessor, Dolby Headphone v2, DTS Neo:6 and Decode, DTS 5.1 Decode (96/24), Math Tables/Twiddle Factors/256 and 512 FFT, and ASRC. Please visit www.analog.com for complete product information and availability.

[2] Contact your local Analog Devices sales office for more information regarding availability of ADSP-21467/ADSP-21469 processors which support DTCP.

Figure 1 on Page 1 shows the two clock domains that make up the processor. The core clock domain contains the following features:

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- One periodic interval timer with pinout
- PM and DM buses capable of supporting 2 × 64-bit data transfers between memory and the core at every core processor cycle
- On-chip SRAM (5 Mbits)
- On-chip mask-programmable ROM (4 Mbits)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

Figure 1 on Page 1 also shows the peripheral clock domain (also known as the I/O processor) which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and DDR2 controller
- 4 units for PWM control
- 1 MTM unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP) for serial and parallel interconnect, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface, one UART, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG) and a flexible signal routing unit (DPI SRU).

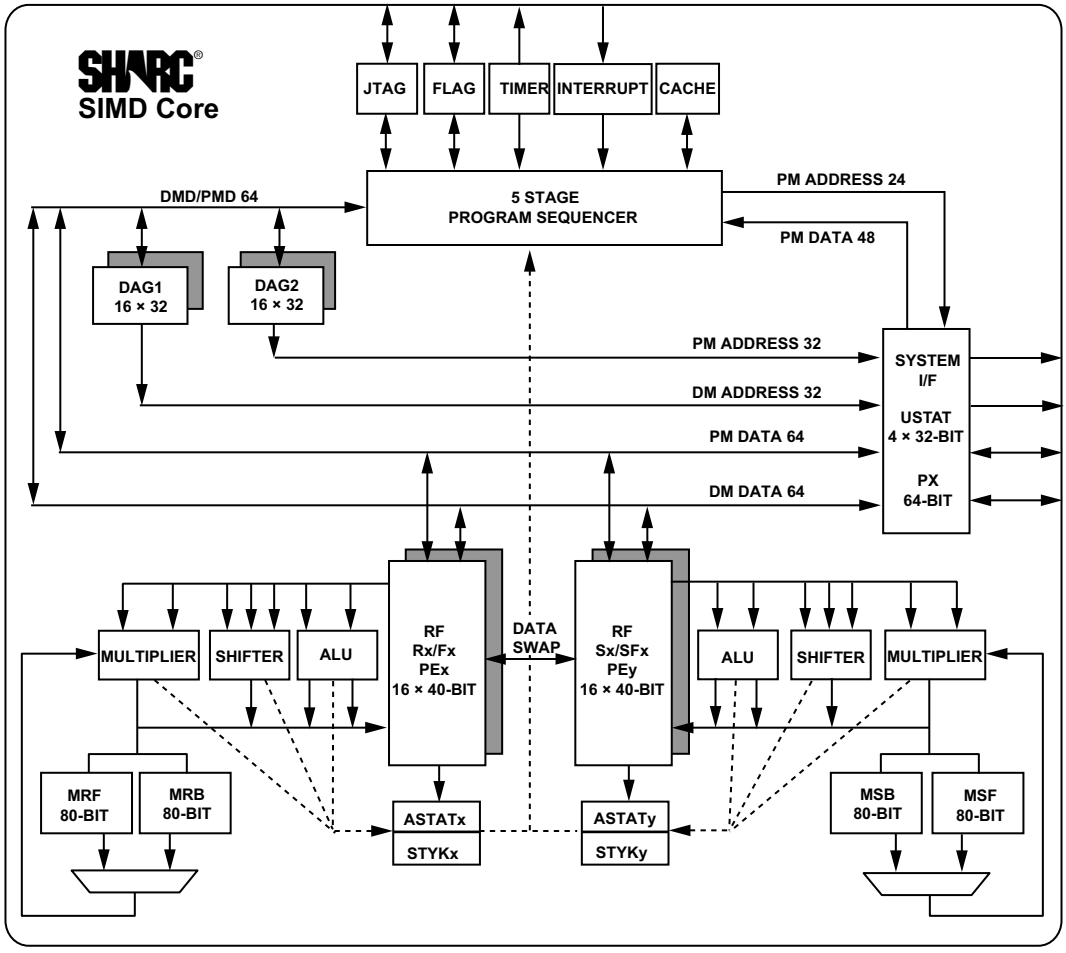

Figure 2. SHARC Core Block Diagram

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the processors support new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external DDR2 memory. Source modules need to be built using the VISA option in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The processors contain 5 Mbits of internal RAM. Each block can be configured for different combinations of code and data storage (see Table 4). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor in a single cycle.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mbits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory map in Table 3 displays the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2 × 64-bits, CCLK speed) and the IOD0/1 buses (2 × 32-bit, PCLK speed).

Nonsecured ROM

For nonsecured ROM, booting modes are selected using the BOOTCFG pins as shown in Table 8 on Page 10. In this mode, emulation is always enabled, and the IVT is placed on the internal RAM except for the case where BOOTCFGx = 011.

ROM-Based Security

The ROM security feature provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processors do not boot-load any external code, executing exclusively from internal ROM. Additionally, the processors are not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer.

Digital Transmission Content Protection

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system.

Table 3. Internal Memory Space[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 EFFF	Block 0 SRAM 0x0008 C000–0x0009 3FFF	Block 0 SRAM 0x0009 2000–0x0009 DFFF	Block 0 SRAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 EFFF	Block 1 SRAM 0x000A C000–0x000B 3FFF	Block 1 SRAM 0x000B 2000–0x000B DFFF	Block 1 SRAM 0x0016 4000–0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 3FFF	Block 2 SRAM 0x000C 0000–0x000C 5554	Block 2 SRAM 0x000C 0000–0x000C 7FFF	Block 2 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000– 0x0006 FFFF	Reserved 0x000C 5555–0x000D FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 3FFF	Block 3 SRAM 0x000E 0000–0x000E 5554	Block 3 SRAM 0x000E 0000–0x000E 7FFF	Block 3 SRAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x0000F FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

[1] Some processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21467/ADSP-21469 architecture and functionality. For detailed information on the core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 10. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{BR}_{2-1}$	I/P (ipu)	$\overline{BR1}$ = driven low by the processor with (ID1=0, ID0=1) $\overline{BR2}$ = driven high by the processor with (ID1=1, ID0=0) $\overline{BR2–1}$ = High-Z if ID pins are at zero	**Bus request.** Used by the processor to arbitrate for bus mastership. A processor only drives its own $\overline{BRx}$ line (corresponding to the value of its ID1–0 inputs) and monitors all others. The processor's own $\overline{BRx}$ line must not be tied high or low because it is an output.
ID_{1-0}	I		**Chip ID.** Determines which bus request ($\overline{BR}_{2-1}$) is used by the processor. ID = 00 corresponds to $\overline{BR1}$ and ID = 10 corresponds to $\overline{BR2}$. Use ID = 00 or 01 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset. ID = 11 is reserved.
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O /T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. The TCK signal must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{TRST}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. The $\overline{TRST}$ signal must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{EMU}$	O/D (ipu)	High-Z	**Emulation Status.** Must be connected to the ADSP-21467/ADSP-21469 Analog Devices DSP Tools product line of JTAG emulators target board connector only.
CLK_CFG_{1-0}	I		**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are: 00 = 6:1 01 = 32:1 10 = 16:1 11 = reserved
CLKIN	I		**Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processor to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processor to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.

The following symbols appear in the Type column of Table 10: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open-drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	450 MHz Min	450 MHz Max	400 MHz Min	400 MHz Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4		2.4		V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]		0.4		0.4	V
V_{OH_DDR2}	High Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, I_{OH} = –13.4 mA	1.4		1.4		V
V_{OL_DDR2}	Low Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, IOL = 13.4 mA		0.29		0.29	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		10		10	µA
I_{IL}[4, 6]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V		10		10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200	µA
I_{IHPD}[6]	High Level Input Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DD_EXT}/V_{DD_DDR} = Max, V_{IN} = V_{DD_EXT}/V_{DD_DDR} Max		10		10	µA
I_{OZL}[7, 9]	Three-State Leakage Current	@ V_{DD_EXT}/V_{DD_DDR} = Max, V_{IN} = 0 V		10		10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200	µA
I_{OZHPD}[9]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200	µA
I_{DD_INT}[10]	Supply Current (Internal)	f_{CCLK} > 0 MHz		Table 13 + Table 14 × ASF		Table 13 + Table 14 × ASF	mA
I_{DD_A}[11]	Supply Current (Analog)	V_{DD_A} = Max		10		10	mA
C_{IN}[12, 13]	Input Capacitance	T_{CASE} = 25°C		5		5	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AMI_ADDR23-0, AMI_DATA7-0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO.
[3] See Output Drive Currents on Page 62 for typical drive current capabilities.
[4] Applies to input pins: BOOTCFGx, CLKCFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[6] Applies to input pins with internal pull-downs: MLBCLK
[7] Applies to three-statable pins: all DDR2 pins.
[8] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[9] Applies to three-statable pins with pull-downs: MLBDAT, MLBSIG, MLBDO, MLBSO, LDAT07-0, LDAT17-0, LCLK0, LCLK1, LACK0, LACK1.
[10] See Engineer-to-Engineer Note EE-348 “Estimating Power Dissipation for ADSP-214xx SHARC Processors” for further information.
[11] Characterized but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

Table 14. Dynamic Current in CCLK Domain—$I_{DD\_INT\_DYNAMIC}$ (mA, with ASF = 1.0)[1]

f_{CCLK} (MHz)[2]	V_{DD_INT}(V)[2]				
	0.95 V	**1.0 V**	**1.05 V**	**1.10 V**	**1.15 V**
100	78	82	86	91	98
150	115	121	130	136	142
200	150	159	169	177	188
250	186	197	208	219	231
300	222	236	249	261	276
350	259	275	288	304	319
400	293	309	328	344	361
450	N/A	N/A	366	385	406

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 20.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 19.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 15 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 15. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32 V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.15 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +3.6 V
Thermal Diode Supply Voltage (V_{DD_THD})	–0.3 V to +3.6 V
DDR2 Controller Supply Voltage (V_{DD_DDR2})	–0.3 V to +1.9 V
DDR2 Input Voltage	–0.3 V to +1.9 V
Input Voltage	–0.3 V to +3.6 V
Output Voltage Swing	–0.3 V to V_{DD_EXT} +0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

PACKAGE INFORMATION

The information presented in Figure 4 and Table 16 provides details about the package branding for the processor. For a complete listing of product availability, see Ordering Guide on Page 74.

Figure 4. Typical Package Brand

Table 16. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non-automotive only. For branding information specific to automotive products, contact Analog Devices, Inc.

AMI Write

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. Memory Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address, Selects[1, 2]		t_{DDR2_CLK} – 9.7 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low [1, 3]		W – 6	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{\text{AMI\_WR}}$ Deasserted[2]	t_{DDR2_CLK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{\text{AMI\_WR}}$ Low[2]	t_{DDR2_CLK} – 3		ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	t_{DDR2_CLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted[4]	t_{DDR2_CLK} – 1.37 + H	t_{DDR2_CLK} + 4.9 + H	ns
t_{WWR}	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$ Low[5]	t_{DDR2_CLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	$2t_{DDR2\_CLK}$ – 6		ns
t_{WDE}	$\overline{\text{AMI\_WR}}$ Low to Data Enabled	t_{DDR2_CLK} – 3.5		ns
W = (number of wait states specified in AMICTLx register) × t_{DDR2_CLK}, H = (number of hold cycles specified in AMICTLx register) × t_{DDR2_CLK}				

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).
[2] The falling edge of $\overline{\text{AMI\_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 62 for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: t_{DDR2_CLK} + H, for both same bank and different bank. For Write to Read: (3 × t_{DDR2_CLK}) + H, for the same bank and different banks.

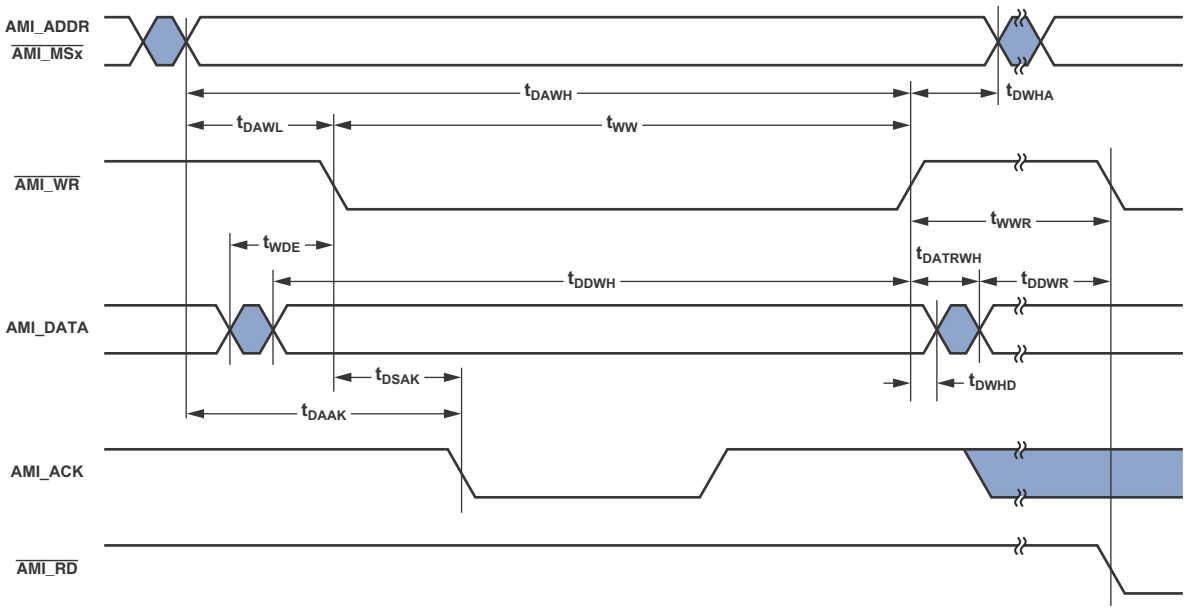

Figure 21. AMI Write

Shared Memory Bus Request

Use these specifications for passing bus mastership between processors ($\overline{BRx}$).

Table 33. Shared Memory Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$, Setup Before CLKIN High	$2 \times t_{PCLK} + 4$		ns
t_{HBRI}	$\overline{BRx}$, Hold After CLKIN High	5		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		20	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	$1 - t_{PCLK}$		ns

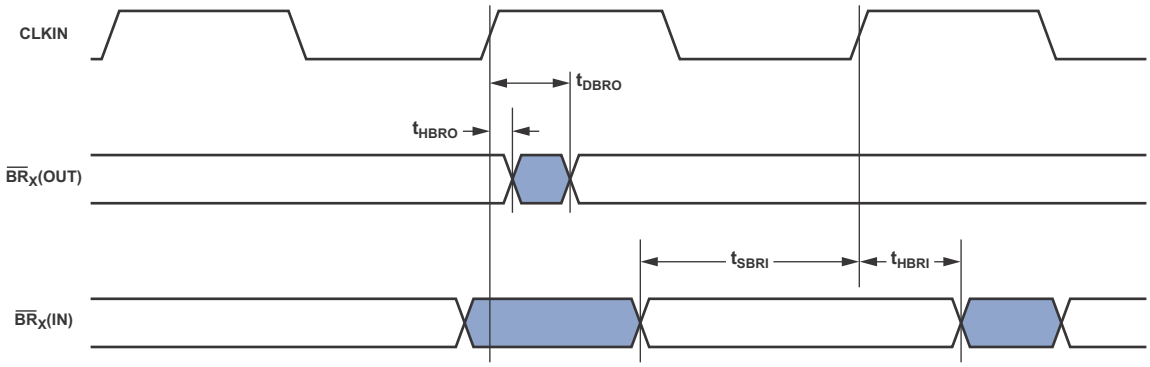

Figure 22. Shared Memory Bus Request

Serial Ports

In slave transmitter mode and master receiver mode the maximum serial port frequency is $f_{PCLK}/8$. To determine whether communication is possible between two devices at clock speed *n*, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins. In Figure 26 either the rising edge or the falling edge of SCLK (external or internal) can be used as the active sampling edge.

Table 37. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.2$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		10.25	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		8.5	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 38. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.25		ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.2$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 41. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		7.75	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as DSP serial mode, and MCE = 1, MFD = 0.

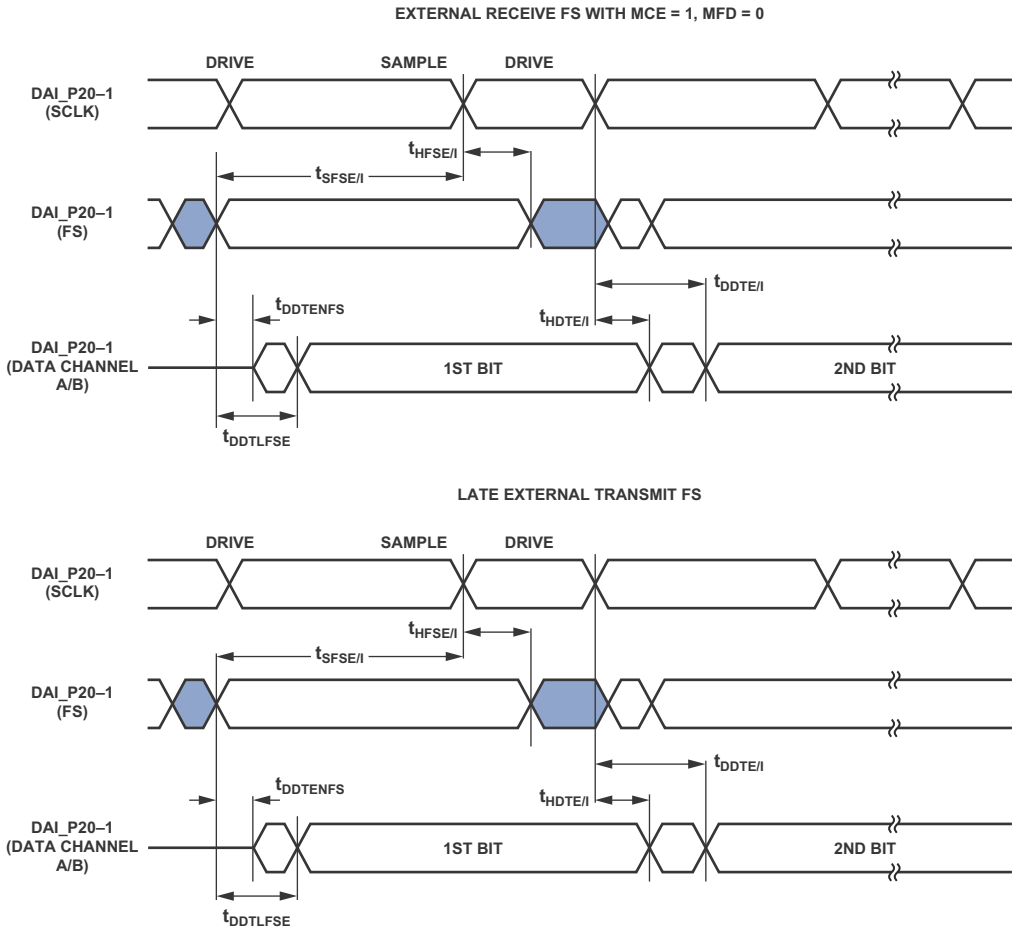

Figure 29. External Late Frame Sync

Sample Rate Converter—Serial Input Port

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 44 are valid at the DAI_P20–1 pins.

Table 44. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

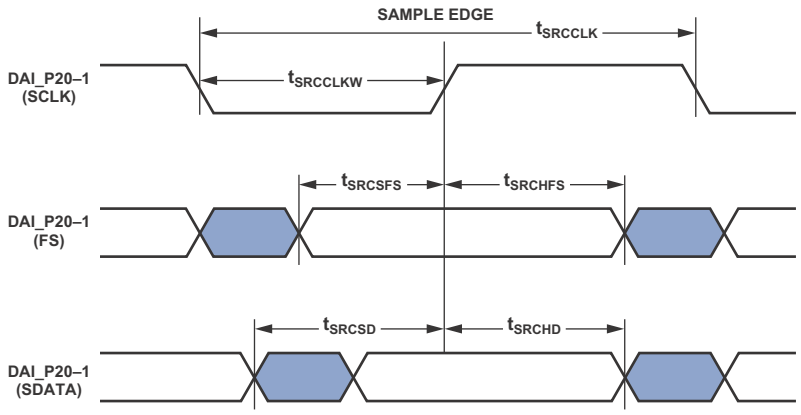

Figure 32. ASRC Serial Input Port Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 35 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed minimum in 24-bit output mode or maximum in 16-bit output mode from an LRCLK transition, so that when there are 64 serial clock periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

Figure 36 shows the default I²S-justified mode. LRCLK is low for the left channel and HI for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition but with a delay.

Figure 37 shows the left-justified mode. LRCLK is high for the left channel and LO for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition with no delay.

Table 47. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	LRCLK to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

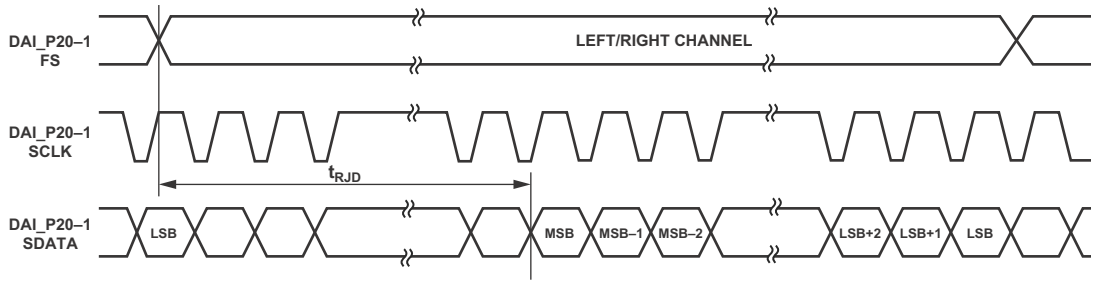

Figure 35. Right-Justified Mode

Table 48. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	LRCLK to MSB Delay in I²S Mode	1	SCLK

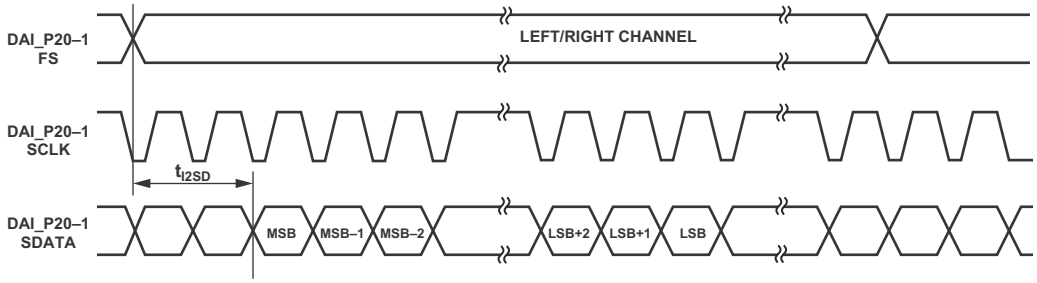

Figure 36. I²S-Justified Mode

SPI Interface—Master

The processor contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 53 and Table 54 applies to both.

Table 53. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

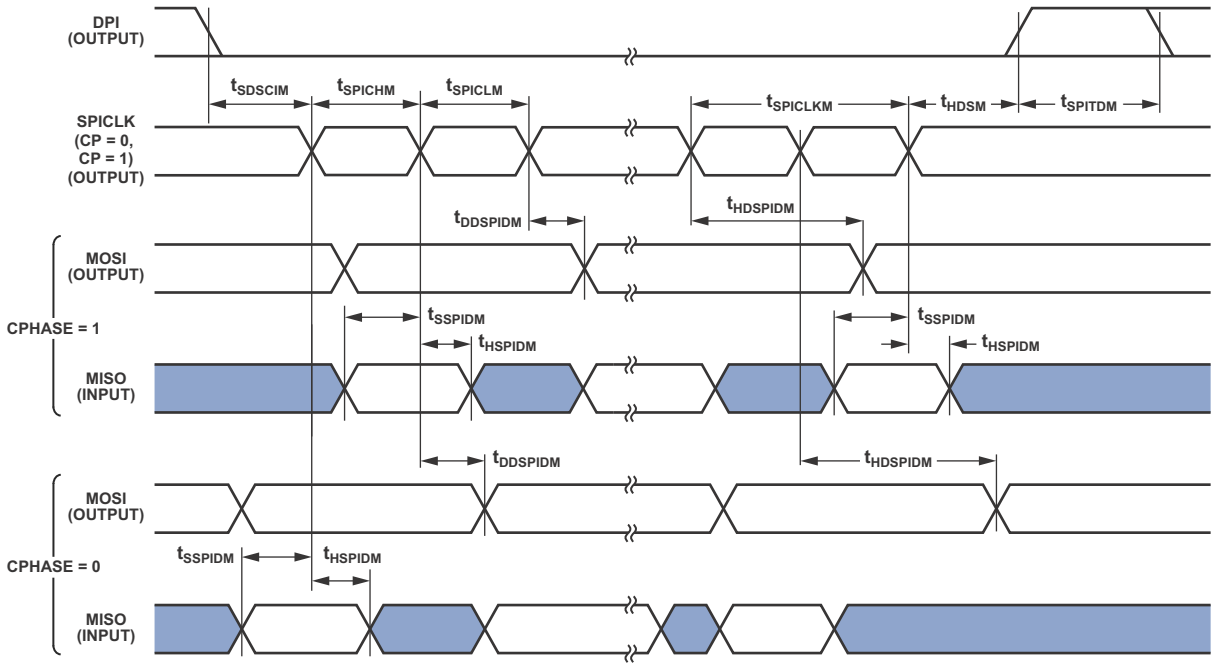

Figure 40. SPI Master Timing

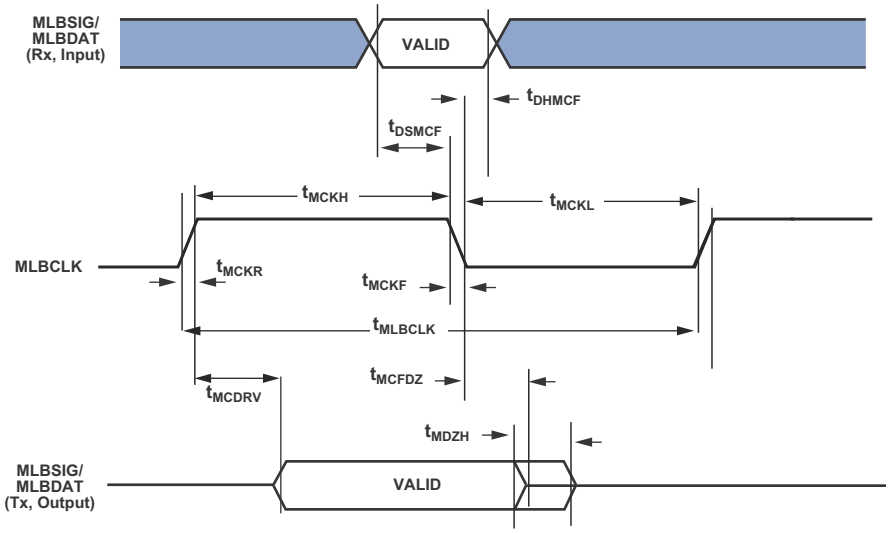

Figure 42. MLB Timing (3-Pin Interface)

Table 56. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	ns p-p
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{MLB}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in nanoseconds peak-to-peak (ns p-p).
[2] Gate delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

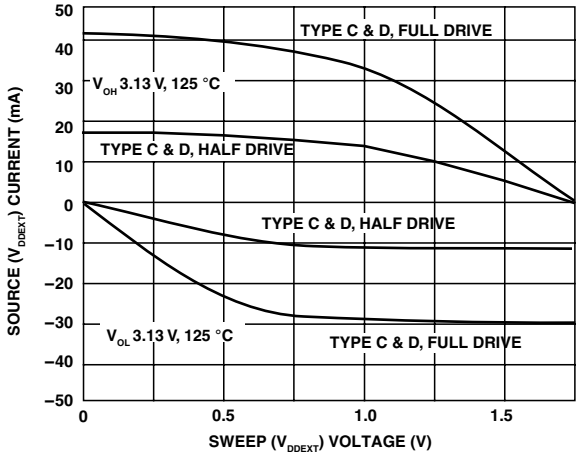

Figure 49. Output Buffer Characteristics (Worst-Case DDR2)

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Table 58). Figure 54 through Figure 59 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 50 through Figure 59 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

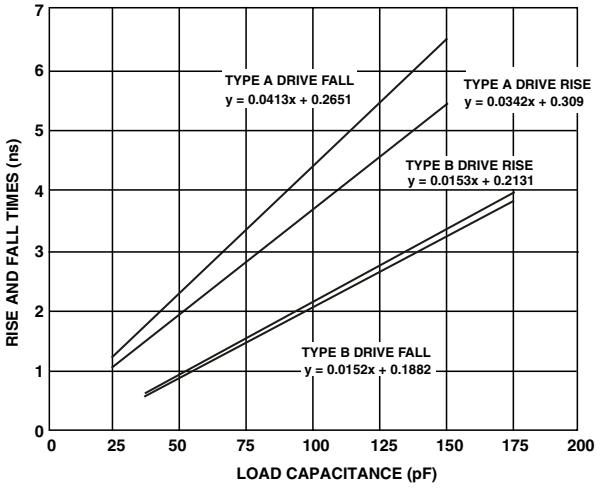

Figure 50. Typical Output Rise/Fall Time Non-DDR2 (20% to 80%, V_{DD_EXT} = Max)

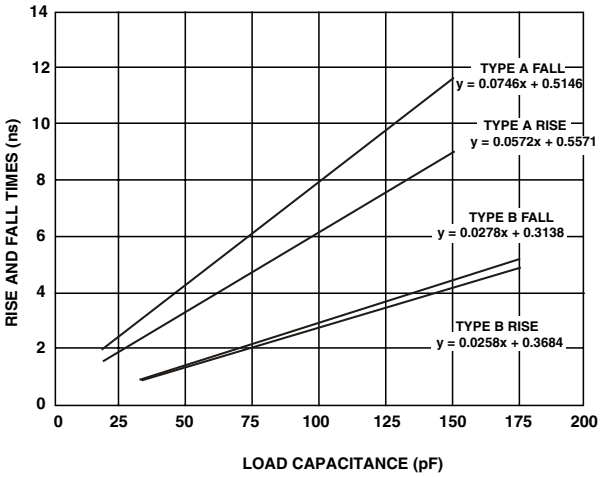

Figure 51. Typical Output Rise/Fall Time Non-DDR2 (20% to 80%, V_{DD_EXT} = Min)

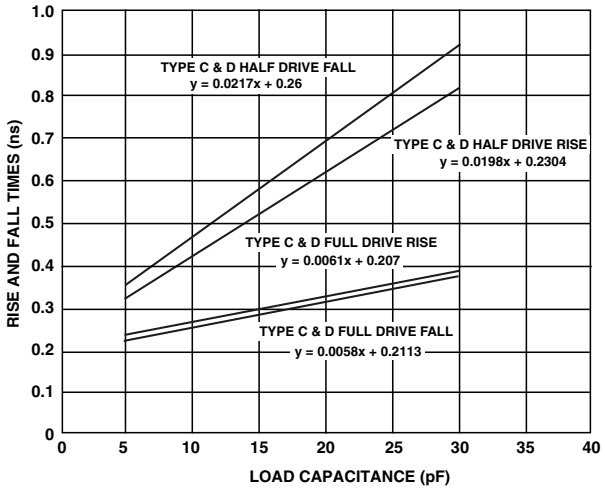

Figure 52. Typical Output Rise/Fall Time DDR2 (20% to 80%, V_{DD_EXT} = Max)

CSP_BGA BALL ASSIGNMENT—AUTOMOTIVE MODELS

Table 61 lists the automotive CSP_BGA ball assignments by signal.

Table 61. CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
AGND	H02	BOOT_CFG2	H03	DDR2_BA0	C18	DPI_P03	T01
AMI_ACK	R10	CLK_CFG0	G01	DDR2_BA1	C17	DPI_P04	R01
AMI_ADDR0	V16	CLK_CFG1	G02	DDR2_BA2	B18	DPI_P05	P01
AMI_ADDR01	U16	CLKIN	L01	$\overline{\text{DDR2\_CAS}}$	C07	DPI_P06	P02
AMI_ADDR02	T16	DAI_P01	R06	DDR2_CKE	E01	DPI_P07	P03
AMI_ADDR03	R16	DAI_P02	V05	$\overline{\text{DDR2\_CLK0}}$	A07	DPI_P08	P04
AMI_ADDR04	V15	DAI_P03	R07	DDR2_CLK0	B07	DPI_P09	N01
AMI_ADDR05	U15	DAI_P04	R03	$\overline{\text{DDR2\_CLK1}}$	A13	DPI_P10	N02
AMI_ADDR06	T15	DAI_P05	U05	DDR2_CLK1	B13	DPI_P11	N03
AMI_ADDR07	R15	DAI_P06	T05	$\overline{\text{DDR2\_CS0}}$	C01	DPI_P12	N04
AMI_ADDR08	V14	DAI_P07	V06	$\overline{\text{DDR2\_CS1}}$	D01	DPI_P13	M03
AMI_ADDR09	U14	DAI_P08	V02	$\overline{\text{DDR2\_CS2}}$	C02	DPI_P14	M04
AMI_ADDR10	T14	DAI_P09	R05	$\overline{\text{DDR2\_CS3}}$	D02	$\overline{\text{EMU}}$	K02
AMI_ADDR11	R14	DAI_P10	V04	DDR2_DATA0	B02	FLAG0	R08
AMI_ADDR12	V13	DAI_P11	U04	DDR2_DATA01	A02	FLAG1	V07
AMI_ADDR13	U13	DAI_P12	T04	DDR2_DATA02	B03	FLAG2	U07
AMI_ADDR14	T13	DAI_P13	U06	DDR2_DATA03	A03	FLAG3	T07
AMI_ADDR15	R13	DAI_P14	U02	DDR2_DATA04	B05	GND	A01
AMI_ADDR16	V12	DAI_P15	R04	DDR2_DATA05	A05	GND	A18
AMI_ADDR17	U12	DAI_P16	V03	DDR2_DATA06	B06	GND	C04
AMI_ADDR18	T12	DAI_P17	U03	DDR2_DATA07	A06	GND	C06
AMI_ADDR19	R12	DAI_P18	T03	DDR2_DATA08	B08	GND	C08
AMI_ADDR20	V11	DAI_P19	T06	DDR2_DATA09	A08	GND	D05
AMI_ADDR21	U11	DAI_P20	T02	DDR2_DATA10	B09	GND	D07
AMI_ADDR22	T11	DDR2_ADDR0	D13	DDR2_DATA11	A09	GND	D09
AMI_ADDR23	R11	DDR2_ADDR01	C13	DDR2_DATA12	A11	GND	D10
AMI_DATA0	U18	DDR2_ADDR02	D14	DDR2_DATA13	B11	GND	D17
AMI_DATA1	T18	DDR2_ADDR03	C14	DDR2_DATA14	A12	GND	E03
AMI_DATA2	R18	DDR2_ADDR04	B14	DDR2_DATA15	B12	GND	E05
AMI_DATA3	P18	DDR2_ADDR05	A14	DDR2_DM0	C03	GND	E12
AMI_DATA4	V17	DDR2_ADDR06	D15	DDR2_DM1	C11	GND	E13
AMI_DATA5	U17	DDR2_ADDR07	C15	DDR2_DQS0	A04	GND	E16
AMI_DATA6	T17	DDR2_ADDR08	B15	$\overline{\text{DDR2\_DQS0}}$	B04	GND	F01
AMI_DATA7	R17	DDR2_ADDR09	A15	DDR2_DQS1	A10	GND	F02
$\overline{\text{AMI\_MS0}}$	T10	DDR2_ADDR10	D16	$\overline{\text{DDR2\_DQS1}}$	B10	GND	F04
$\overline{\text{AMI\_MS1}}$	U10	DDR2_ADDR11	C16	DDR2_ODT	B01	GND	F14
$\overline{\text{AMI\_RD}}$	J04	DDR2_ADDR12	B16	$\overline{\text{DDR2\_RAS}}$	C09	GND	F16
$\overline{\text{AMI\_WR}}$	V10	DDR2_ADDR13	A16	$\overline{\text{DDR2\_WE}}$	C10	GND	G05
BOOT_CFG0	J02	DDR2_ADDR14	B17	DPI_P01	R02	GND	G07
BOOT_CFG1	J03	DDR2_ADDR15	A17	DPI_P02	U01	GND	G08

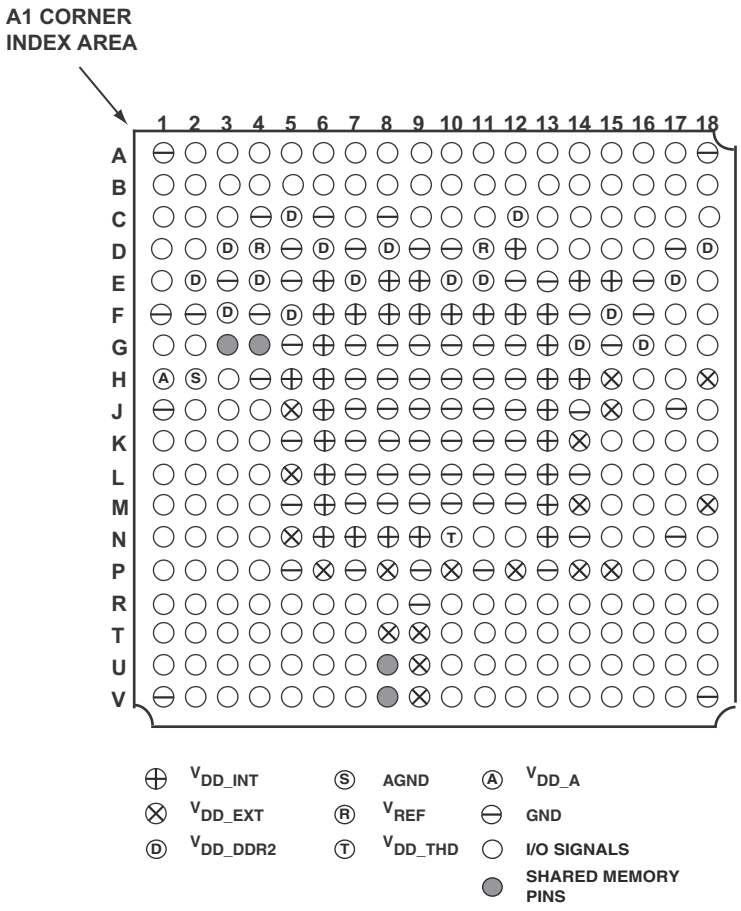

Figure 60. Ball Configuration, Automotive Model

CSP_BGA BALL ASSIGNMENT—STANDARD MODELS

Table 62 lists the standard model CSP_BGA ball assignments by signal.

Table 62. CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
AGND	H02	BOOT_CFG2	H03	DDR2_BA0	C18	DPI_P03	T01
AMI_ACK	R10	CLK_CFG0	G01	DDR2_BA1	C17	DPI_P04	R01
AMI_ADDR0	V16	CLK_CFG1	G02	DDR2_BA2	B18	DPI_P05	P01
AMI_ADDR01	U16	CLKIN	L01	$\overline{\text{DDR2\_CAS}}$	C07	DPI_P06	P02
AMI_ADDR02	T16	DAI_P01	R06	DDR2_CKE	E01	DPI_P07	P03
AMI_ADDR03	R16	DAI_P02	V05	$\overline{\text{DDR2\_CLK0}}$	A07	DPI_P08	P04
AMI_ADDR04	V15	DAI_P03	R07	DDR2_CLK0	B07	DPI_P09	N01
AMI_ADDR05	U15	DAI_P04	R03	$\overline{\text{DDR2\_CLK1}}$	A13	DPI_P10	N02
AMI_ADDR06	T15	DAI_P05	U05	DDR2_CLK1	B13	DPI_P11	N03
AMI_ADDR07	R15	DAI_P06	T05	$\overline{\text{DDR2\_CS0}}$	C01	DPI_P12	N04
AMI_ADDR08	V14	DAI_P07	V06	$\overline{\text{DDR2\_CS1}}$	D01	DPI_P13	M03
AMI_ADDR09	U14	DAI_P08	V02	$\overline{\text{DDR2\_CS2}}$	C02	DPI_P14	M04
AMI_ADDR10	T14	DAI_P09	R05	$\overline{\text{DDR2\_CS3}}$	D02	$\overline{\text{EMU}}$	K02
AMI_ADDR11	R14	DAI_P10	V04	DDR2_DATA0	B02	FLAG0	R08
AMI_ADDR12	V13	DAI_P11	U04	DDR2_DATA01	A02	FLAG1	V07
AMI_ADDR13	U13	DAI_P12	T04	DDR2_DATA02	B03	FLAG2	U07
AMI_ADDR14	T13	DAI_P13	U06	DDR2_DATA03	A03	FLAG3	T07
AMI_ADDR15	R13	DAI_P14	U02	DDR2_DATA04	B05	GND	A01
AMI_ADDR16	V12	DAI_P15	R04	DDR2_DATA05	A05	GND	A18
AMI_ADDR17	U12	DAI_P16	V03	DDR2_DATA06	B06	GND	C04
AMI_ADDR18	T12	DAI_P17	U03	DDR2_DATA07	A06	GND	C06
AMI_ADDR19	R12	DAI_P18	T03	DDR2_DATA08	B08	GND	C08
AMI_ADDR20	V11	DAI_P19	T06	DDR2_DATA09	A08	GND	D05
AMI_ADDR21	U11	DAI_P20	T02	DDR2_DATA10	B09	GND	D07
AMI_ADDR22	T11	DDR2_ADDR0	D13	DDR2_DATA11	A09	GND	D09
AMI_ADDR23	R11	DDR2_ADDR01	C13	DDR2_DATA12	A11	GND	D10
AMI_DATA0	U18	DDR2_ADDR02	D14	DDR2_DATA13	B11	GND	D17
AMI_DATA1	T18	DDR2_ADDR03	C14	DDR2_DATA14	A12	GND	E03
AMI_DATA2	R18	DDR2_ADDR04	B14	DDR2_DATA15	B12	GND	E05
AMI_DATA3	P18	DDR2_ADDR05	A14	DDR2_DM0	C03	GND	E12
AMI_DATA4	V17	DDR2_ADDR06	D15	DDR2_DM1	C11	GND	E13
AMI_DATA5	U17	DDR2_ADDR07	C15	DDR2_DQS0	A04	GND	E16
AMI_DATA6	T17	DDR2_ADDR08	B15	$\overline{\text{DDR2\_DQS0}}$	B04	GND	F01
AMI_DATA7	R17	DDR2_ADDR09	A15	DDR2_DQS1	A10	GND	F02
$\overline{\text{AMI\_MS0}}$	T10	DDR2_ADDR10	D16	$\overline{\text{DDR2\_DQS1}}$	B10	GND	F04
$\overline{\text{AMI\_MS1}}$	U10	DDR2_ADDR11	C16	DDR2_ODT	B01	GND	F14
$\overline{\text{AMI\_RD}}$	J04	DDR2_ADDR12	B16	$\overline{\text{DDR2\_RAS}}$	C09	GND	F16
$\overline{\text{AMI\_WR}}$	V10	DDR2_ADDR13	A16	$\overline{\text{DDR2\_WE}}$	C10	GND	G05
BOOT_CFG0	J02	DDR2_ADDR14	B17	DPI_P01	R02	GND	G07
BOOT_CFG1	J03	DDR2_ADDR15	A17	DPI_P02	U01	GND	G08