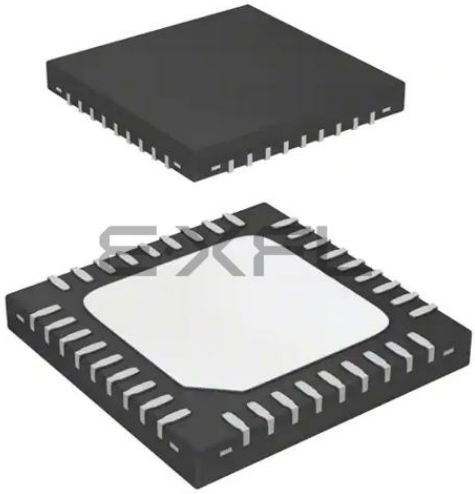

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	8MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFQFN Exposed Pad
Supplier Device Package	36-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m37546g4hp-u0

7546 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0160-0122
Rev.1.22
Mar 13, 2009

DESCRIPTION

The 7546 Group is the QzROM version of 7542 Group.
The 7546 Group has the pin-compatibility with the 7542 Group. As new functions, the power-on reset, the low voltage detection circuit, and the function set ROM are added.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.25 μs (at 8 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size
  - ROM ..... 8K, 16K bytes
  - RAM ..... 384, 512 bytes
- Programmable I/O ports 25
- Interrupts ..... 18 sources, 16 vectors
- Timers ..... 8-bit × 2
  ..... 16-bit × 2
- Output compare 4-channel
- Input capture 2-channel
- Serial interface ..... 8-bit × 2 (UART or Clock-synchronized)
- A/D converter ..... 10-bit × 6 channels
- Clock generating circuit ..... Built-in type
  (low-power dissipation by an on-chip oscillator)
  (connected to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer ..... 16-bit × 1
- Power-on reset circuit ..... Built-in type
- Low voltage detection circuit ..... Built-in type
- Power source voltage
  - XIN oscillation frequency at ceramic oscillation, in double-speed mode
    - At 8 MHz ..... 4.5 to 5.5 V
    - At 6.5 MHz ..... 4.0 to 5.5 V
    - At 2 MHz ..... 2.4 to 5.5 V
    - At 1 MHz ..... 2.2 to 5.5 V
  - XIN oscillation frequency at ceramic oscillation, in high-speed mode or middle-speed mode
    - At 8 MHz ..... 4.0 to 5.5 V
    - At 4 MHz ..... 2.4 to 5.5 V
    - At 2 MHz ..... 2.2 to 5.5 V
  - XIN oscillation frequency at RC oscillation in high-speed mode or middle-speed mode
    - At 4 MHz ..... 4.0 to 5.5 V
    - At 2 MHz ..... 2.4 to 5.5 V
    - At 1 MHz ..... 2.2 to 5.5 V
  - XIN oscillation frequency at on-chip oscillation ..... 1.8 to 5.5 V
- Power dissipation ..... 29.5 mW (Typ.)
- Operating temperature range ..... –20 to 85 °C

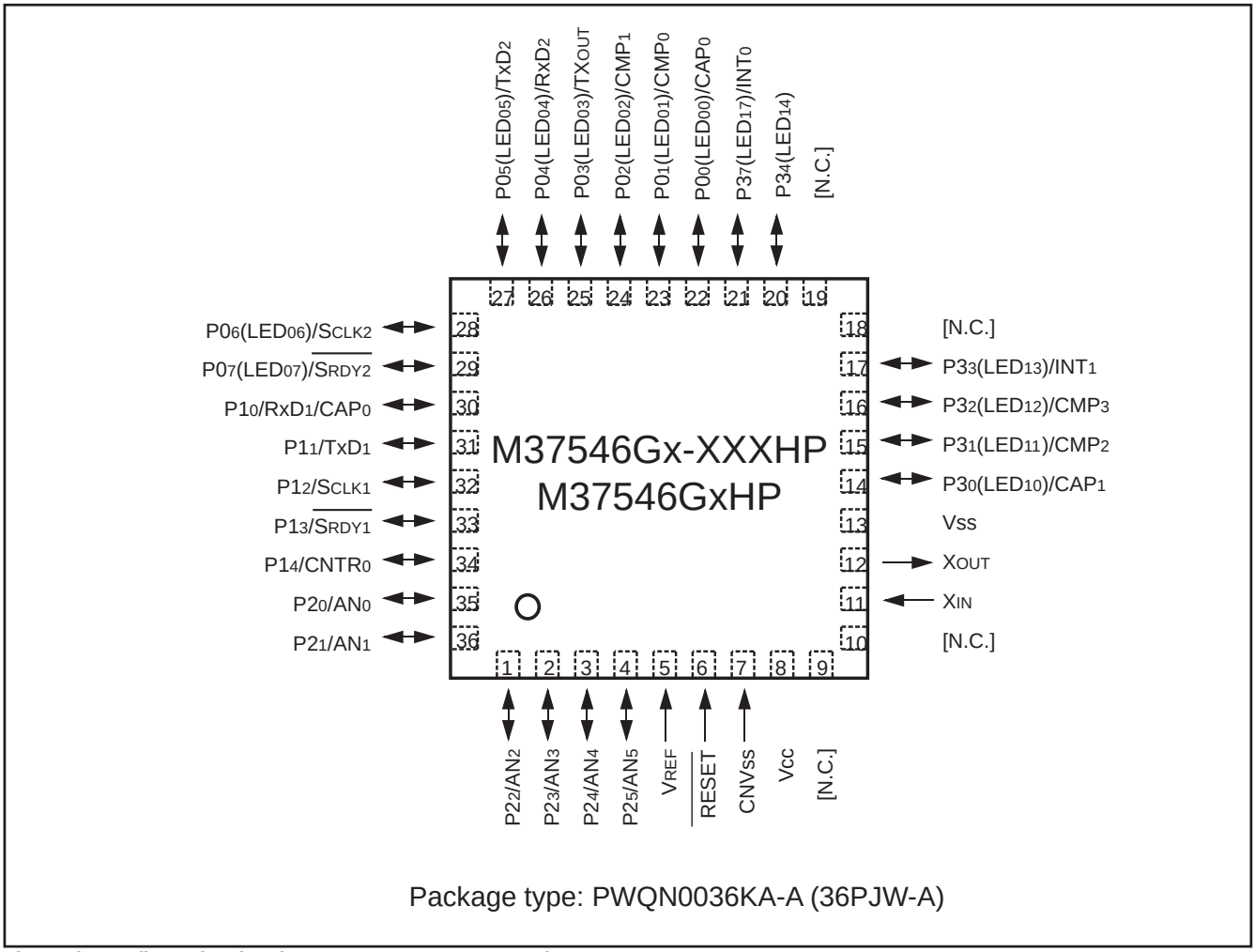


Fig. 3 Pin configuration (Package type: PWQN0036KA-A)

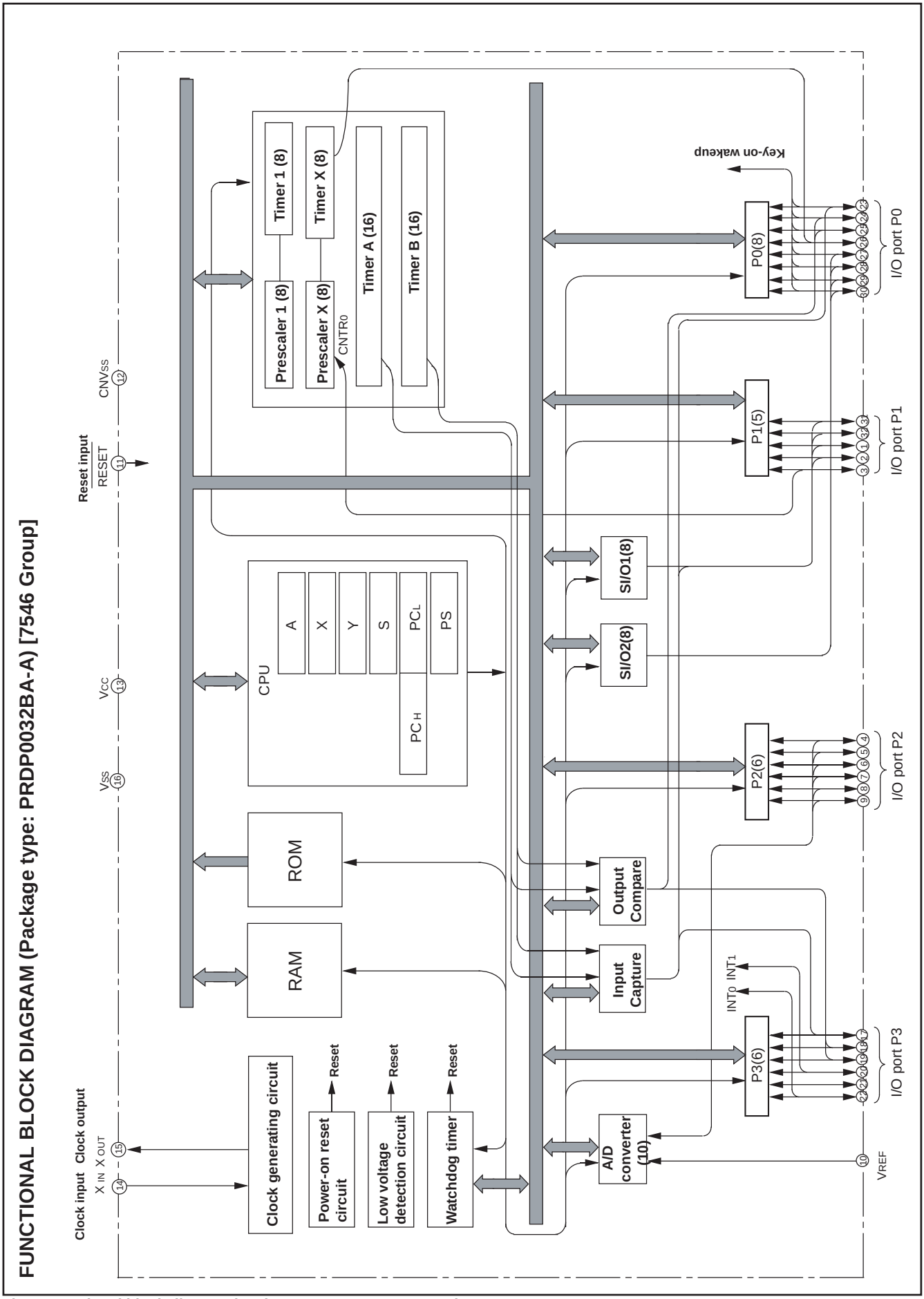


Fig. 5 Functional block diagram (Package type: PRDP0032BA-A)

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Code Protect Address (address $FFDB_{16}$)

Address $FFDB_{16}$, which is the reserved ROM area of QzROM, is the ROM code protect address. "00_{16}" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00_{16}" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "00_{16}" (protect enabled) or "FF_{16}" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "00_{16}" or "FF_{16}" can be selected as the ROM option setup (referred to as "Mask option setup" in MM) when ordering.

■ **Notes**

Because the contents of RAM are indefinite at reset, set initial values before using.

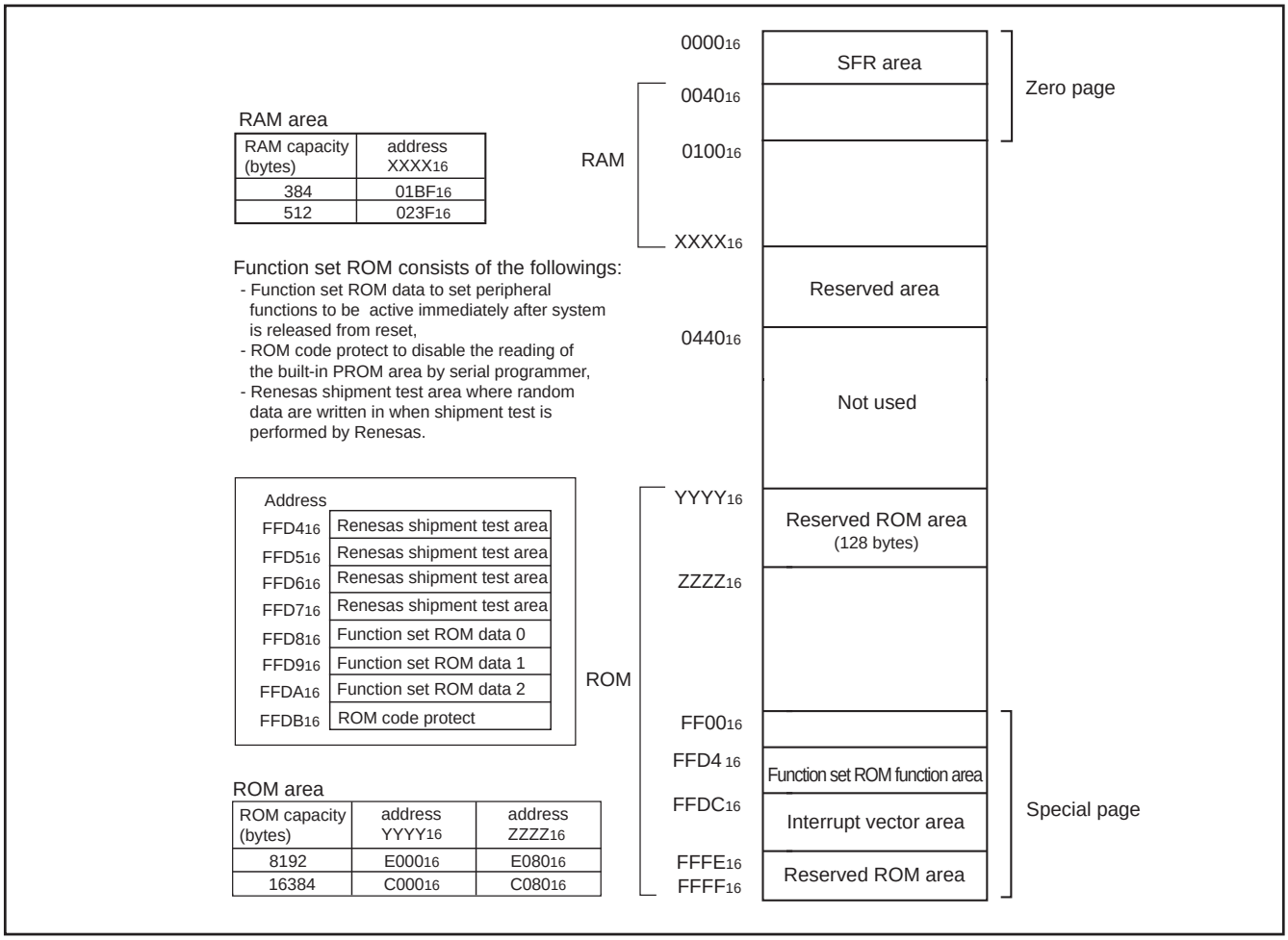


Fig. 10 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Capture mode register (CAPM)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Compare output mode register (CMOM)
0002_{16}	Port P1 (P1)	0022_{16}	Capture/compare status register (CCSR)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Compare interrupt source set register (CISR)
0004_{16}	Port P2 (P2)	0024_{16}	Timer A (low-order) (TAL)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer A (high-order) (TAH)
0006_{16}	Port P3 (P3)	0026_{16}	Timer B (low-order) (TBL)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer B (high-order) (TBH)
0008_{16}	Reserved	0028_{16}	Prescaler 1 (PRE1)
0009_{16}	Reserved	0029_{16}	Timer 1 (T1)
$000A_{16}$	Interrupt source set register (INTSET)	$002A_{16}$	Timer count source set register (TCSS)
$000B_{16}$	Interrupt source discrimination register (INTDIS)	$002B_{16}$	Timer X mode register (TXM)
$000C_{16}$	Capture register 0 (low-order) (CAP0L)	$002C_{16}$	Prescaler X (PREX)
$000D_{16}$	Capture register 0 (high-order) (CAP0H)	$002D_{16}$	Timer X (TX)
$000E_{16}$	Capture register 1 (low-order) (CAP1L)	$002E_{16}$	Transmit 2 / Receive 2 buffer register (TB2/RB2)
$000F_{16}$	Capture register 1 (high-order) (CAP1H)	$002F_{16}$	Serial I/O2 status register (SIO2STS)
0010_{16}	Compare register (low-order) (CMPL)	0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}	Compare register (high-order) (CMPH)	0031_{16}	UART2 control register (UART2CON)
0012_{16}	Capture/compare register R/W pointer (CCRP)	0032_{16}	Baud rate generator 2 (BRG2)
0013_{16}	Capture software trigger register (CSTR)	0033_{16}	Reserved
0014_{16}	Compare register re-load register (CMPR)	0034_{16}	A/D control register (ADCON)
0015_{16}	Port P0P3 drive capacity control register (DCCR)	0035_{16}	A/D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A/D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	On-chip oscillation division ratio selection register (RODR)
0018_{16}	Transmit 1 /Receive 1 buffer register (TB1/RB1)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART1 control register (UART1CON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator 1 (BRG1)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Timer A, B mode register (TABM)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Capture/compare port register (CCPR)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Timer source selection register (TMSR)	$003F_{16}$	Interrupt control register 2 (ICON2)

Notes 1: Do not access to the SFR area including nothing.

Fig. 13 Memory map of special function register (SFR)

Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

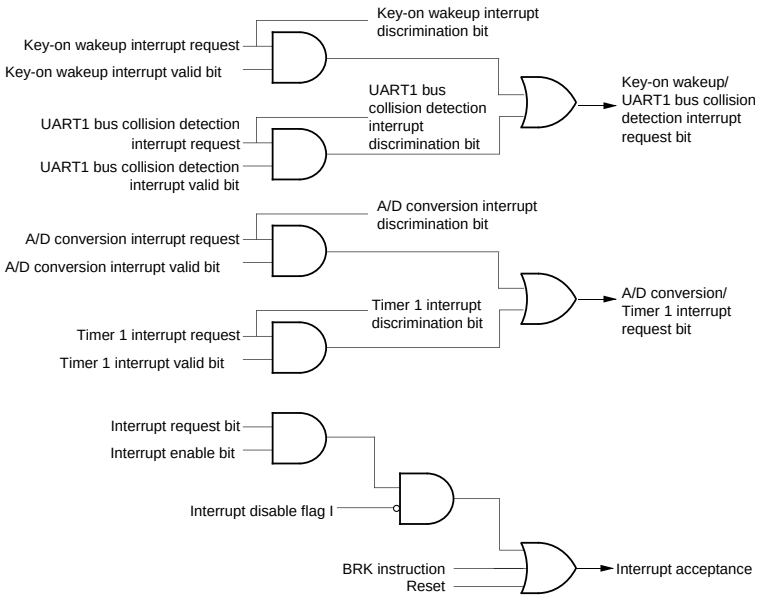
Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase. Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).

We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.

Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 7 Termination of unused pins

Pin	Termination 1 (recommend)	Termination 2	Termination 3	Termination 4
P0$_0$/CAP$_0$	I/O port	When selecting CAP function, perform termination of input port.	-	When selecting key-on wakeup function, perform termination of input port.
P0$_1$/CMP$_0$		When selecting CMP$_0$ function, perform termination of output port.	-	
P0$_2$/CMP$_1$		When selecting CMP$_1$ function, perform termination of output port.	-	
P0$_3$/TXOUT		When selecting TXOUT function, perform termination of output port.	-	
P0$_4$/RxD$_2$		When selecting RxD$_2$ function, perform termination of input port.	-	
P0$_5$/TxD$_2$		When selecting TxD$_2$ function, perform termination of output port.	-	
P0$_6$/SCLK2		When selecting external clock input, perform termination of output port.	When selecting internal clock output, perform termination of output port.	
P0$_7$/$\overline{\text{SRDY2}}$		When selecting $\overline{\text{SRDY2}}$ function, perform termination of output port.	-	
P1$_0$/RxD$_1$/CAP$_0$		When selecting RxD$_1$ function, perform termination of input port.	When selecting CAP function, perform termination of input port.	-
P1$_1$/TxD$_1$		When selecting TxD$_1$ function, perform termination of output port.	-	-
P1$_2$/SCLK1		When selecting external clock input, perform termination of input port.	When selecting internal clock output, perform termination of output port.	-
P1$_3$/$\overline{\text{SRDY1}}$		When selecting $\overline{\text{SRDY1}}$ function, perform termination of output port.	-	-
P1$_4$/CNTR$_0$		When selecting CNTR input function, perform termination of input port.	When selecting CNTR output function, perform termination of output port.	-
P2$_0$/AN$_0$–P2$_5$/AN$_5$		When selecting AN function, perform termination of input port.	-	-
P3$_0$/CAP$_1$		When selecting CAP function, perform termination of input port.	-	-
P3$_1$/CMP$_2$		When selecting CMP$_2$ function, perform termination of output port.	-	-
P3$_2$/CMP$_3$		When selecting CMP$_3$ function, perform termination of output port.	-	-
P3$_3$/INT$_1$		When selecting INT function, perform termination of input port.	-	-
P3$_4$		-	-	-
P3$_7$/INT$_0$		When selecting INT function, perform termination of input port.	-	-
VREF	Connect to Vss.	-	-	-
XIN	When only on-chip oscillator is used, connect to VCC through a registor.	-	-	-
XOUT	When external clock is input or when only on-chip oscillator is used, open.	-	-	-



Note: For key-on wakeup, UART1 bus collision detection, A/D conversion and Timer 1 interrupt, even if interrupt valid bit ($000A_{16}$) is set "0: Invalid", interrupt discrimination bit ($000B_{16}$) is set to "1: interrupt occurs" when corresponding interrupt request occurs.
But corresponding interrupt request bit ($003C_{16}$, $003D_{16}$) is not set to "1".

Fig. 20 Interrupt control

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", the acceptance of interrupt requests is enabled. This flag is set to "1" with the SEI instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled.

To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", the acceptance of the corresponding interrupt request is enabled.

Each interrupt enable bit can be set to "0" or "1" by software.

The interrupt enable bit for an unused interrupt should be set to "0".

• Interrupt Enable Setting

The following interrupt sources can be set to valid or invalid by the interrupt source set register ($000A_{16}$).

- Key-on wakeup
- UART1 bus collision detection interrupt
- A/D conversion
- Timer 1 interrupt

• Interrupt edge selection

The valid edge of external interrupt INT_0 and INT_1 can be selected by the interrupt edge selection bit of the interrupt edge selection register ($003A_{16}$), respectively.

Set bit 2 of interrupt edge selection register to "1".

• Key-on wakeup

Enable/disable of a key-on wakeup of pins $P0_0$, $P0_4$, and $P0_6$ can be selected by the key-on wakeup enable bit of the interrupt edge selection register ($003A_{16}$), respectively.

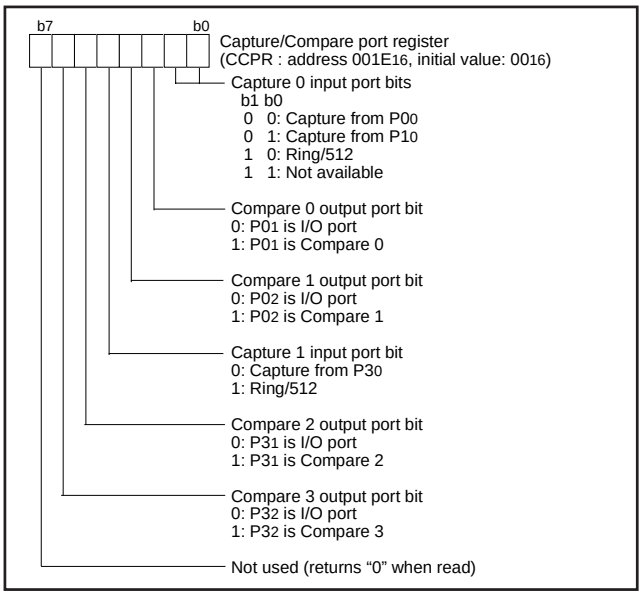


Fig. 34 Structure of capture/compare port register

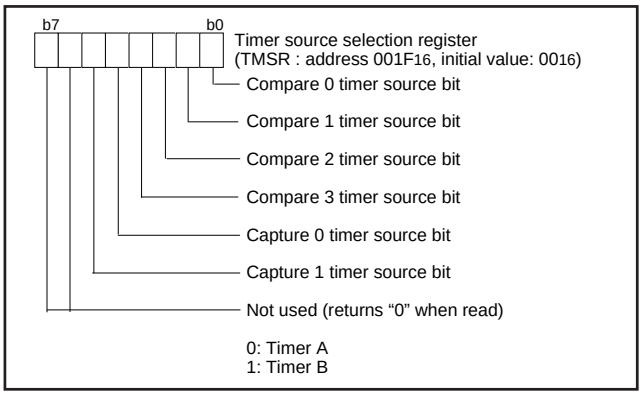


Fig. 35 Structure of timer source selection register

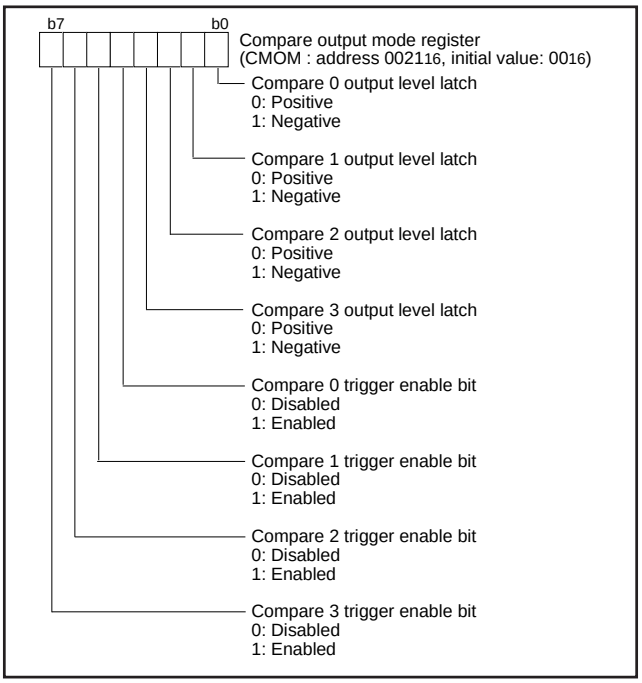


Fig. 36 Structure of compare output mode register

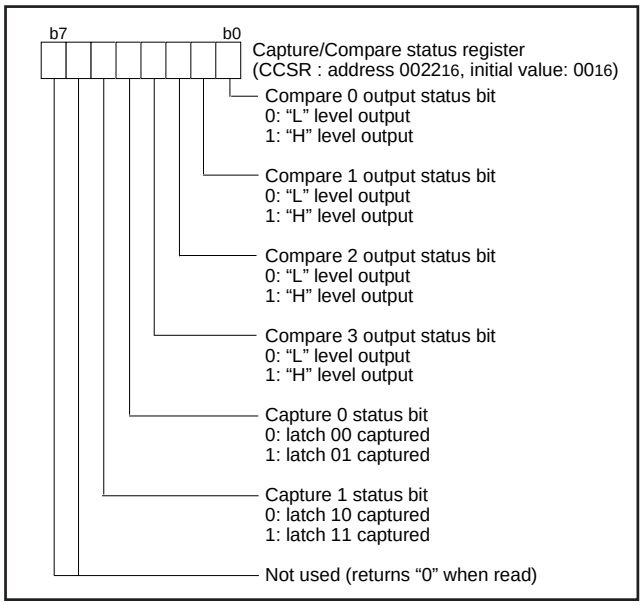


Fig. 37 Structure of capture/compare status register

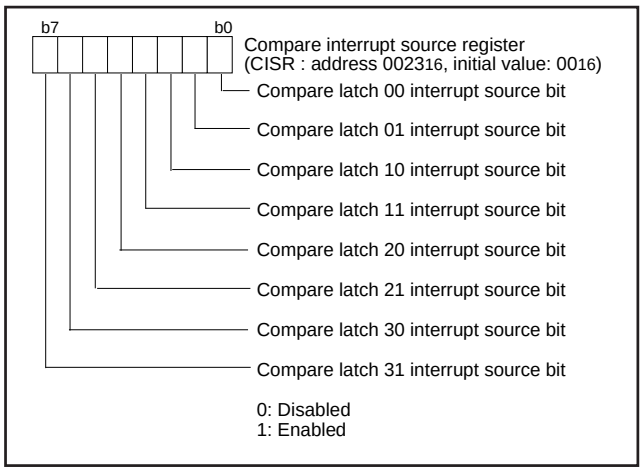


Fig. 38 Structure of compare interrupt source register

(2) Asynchronous Serial I/O2 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O2 mode selection bit of the serial I/O2 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

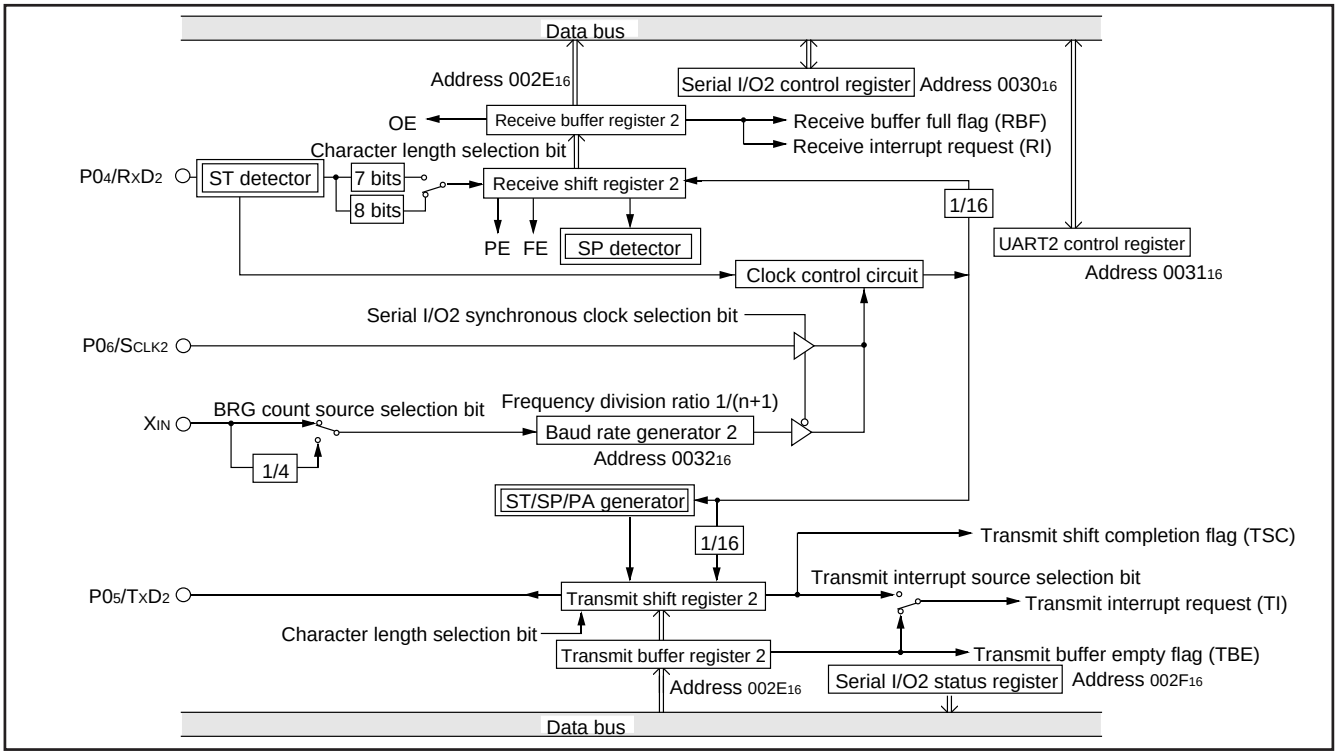
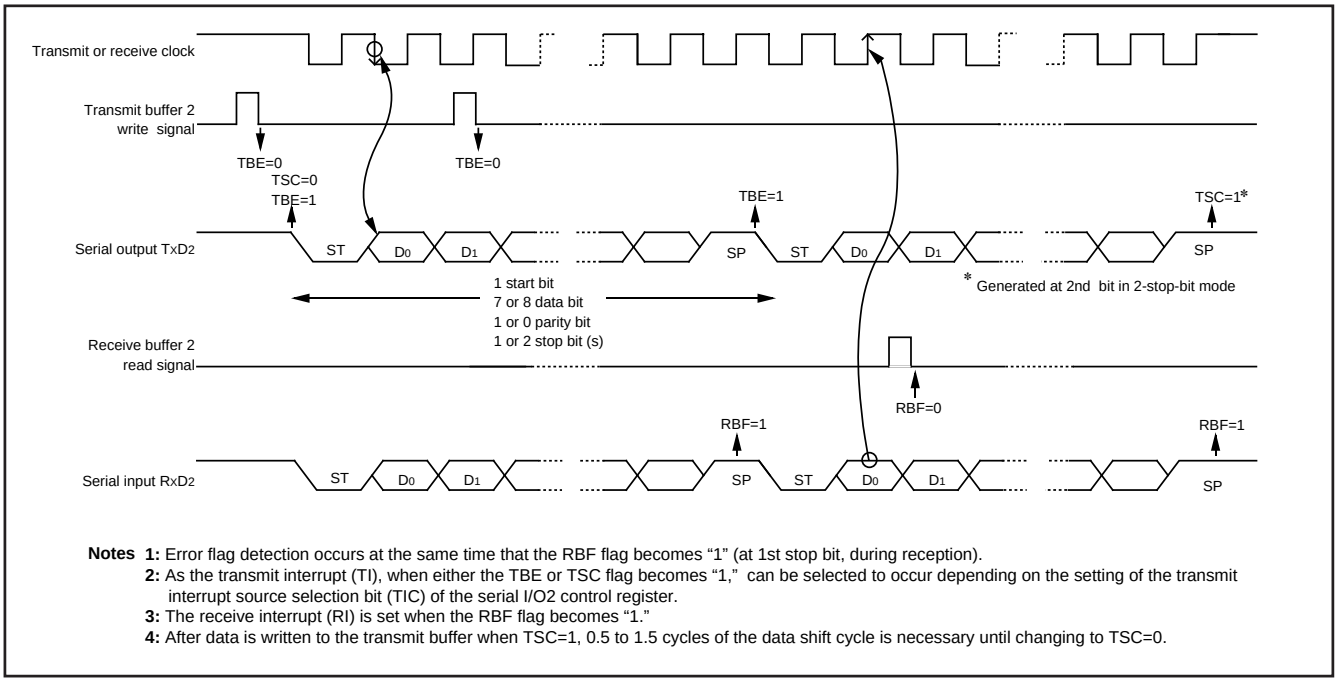


Fig. 62 Block diagram of UART serial I/O2



Notes
1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O2 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 63 Operation of UART serial I/O2 function

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.
Use the circuit constants in accordance with the resonator manufacturer's recommended values.
No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.)

(1) On-chip oscillator operation

When the MCU operates by the on-chip oscillator for the main clock, connect XIN pin to VCC through a resistor and leave XOUT pin open.
The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies when designing application products.

(2) Ceramic resonator

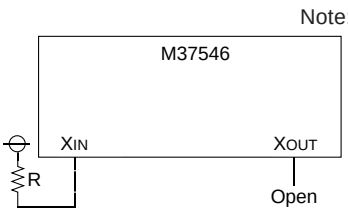
When the ceramic resonator is used for the main clock, connect the ceramic resonator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT.

(3) RC oscillation

When the RC oscillation is used for the main clock, connect the XIN pin and XOUT pin to the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

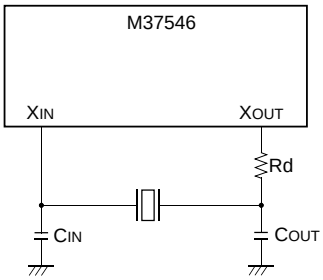
(4) External clock

When the external signal clock is used for the main clock, connect the XIN pin to the clock source and leave XOUT pin open.
Select “0” (ceramic oscillation) to oscillation mode selection bit of CPU mode register ($003B_{16}$).



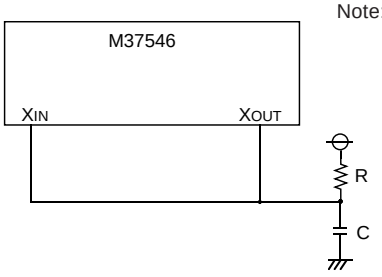
Note: The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies and obtain the sufficient margin.

Fig. 74 Processing of XIN and XOUT pins at on-chip oscillator operation



Note: Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer’s data sheet specifies that a feedback resistor be added external to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 75 External circuit of ceramic resonator



Note: Connect the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

Fig. 76 External circuit of RC oscillation

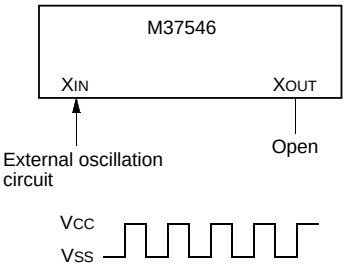


Fig. 77 External clock input circuit

(1) Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock φ stops at an "H" level and the XIN oscillator stops. At this time, timer 1 is set to "01$_{16}$" and prescaler 1 is set to "FF$_{16}$" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. f(XIN)/16 is forcibly connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock φ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock φ is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable, or set the wait time by on-chip oscillator operation after system is released from reset until the oscillation is stabled.

• Wait mode

If the WIT instruction is executed, the internal clock φ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

■ Notes on Clock Generating Circuit

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting an on-chip oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

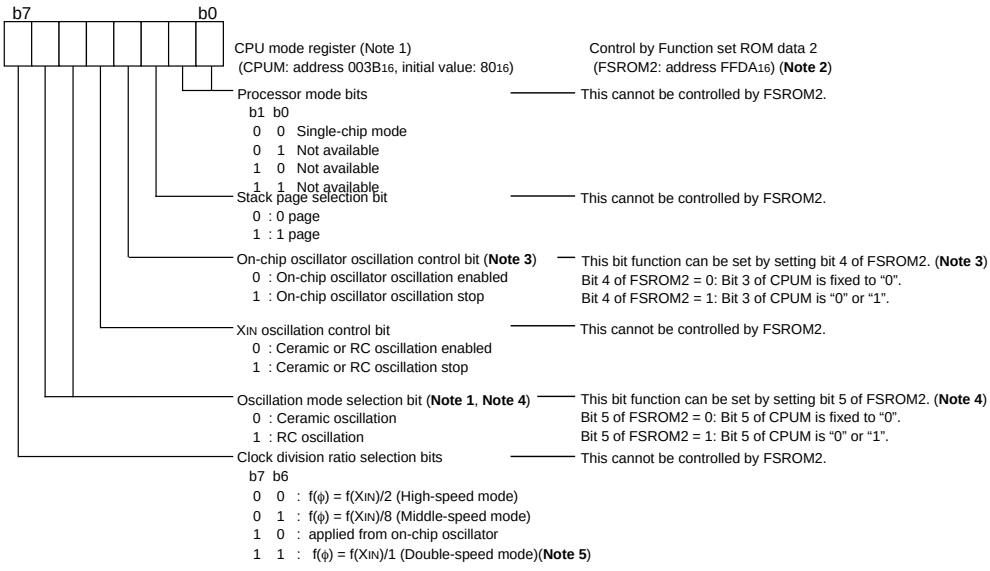
• Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

• CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37542RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.



Note 1: When the setting by the function set ROM data 2 (FSROM2) is performed, the initial value of CPUM is changed after releasing reset since bit 5 of CPUM is fixed.

2: The setting values of FSROM2 become valid by setting "0" to bit 0 of function set ROM data 0 (FSROM0). The setting values of FSROM2 are invalid by setting "1" to this bit. (In order that FSROM2 is invalid, write to CPUM after releasing reset.)

3: When bit 4 of FSROM2 is set to "0", the operation of on-chip oscillator cannot be stopped. Since the on-chip oscillator is not stopped also in the stop mode, the dissipation current in the stop mode is increased.

4: The setting value of bit 5 of CPUM can be fixed after releasing reset by setting value of bit 5 of FSROM2. Also, when the setting of FSROM2 is invalid, this bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit. This bit is initialized by reset, and then, rewriting it is enabled.

5: This setting can be used only at ceramic oscillation. Do not use this at RC oscillation.

Fig. 78 Structure of CPU mode register

• Clock division ratio, XIN oscillation control, on-chip oscillator control
The state transition shown in Fig. 82 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), on-chip oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 82.

• Count source (Timer 1, Timer A, Timer B, Timer X, Serial I/O, Serial I/O2, A/D converter, Watchdog timer)
The count sources of these functions are affected by the clock division selection bit of the CPU mode register.
The f(XIN) clock is supplied to the watchdog timer when selecting f(XIN) as the CPU clock.
The on-chip oscillator output is supplied to these functions when selecting the on-chip oscillator output as the CPU clock.
However, the watchdog timer is also affected by the function set ROM.

● On-chip oscillation division ratio

At on-chip oscillator mode, division ratio of on-chip oscillator for CPU clock is selected by setting value of on-chip oscillation division ratio selection register. The division ratio of on-chip oscillation for CPU clock is selected from among 1/1, 1/2, 1/8, 1/128. The operation clock for the peripheral function block is not changed by setting value of this register.

■ Notes on On-chip Oscillation Division Ratio

• When system is released from reset, ROSC/8 (on-chip oscillator middle-speed mode) is selected for CPU clock.
• When state transition from the ceramic or RC oscillation to on-chip oscillator, ROSC/8 (on-chip oscillator middle-speed mode) is selected for CPU clock.
• When the MCU operates by on-chip oscillator for the main clock without external oscillation circuit, connect XIN pin to VCC through a resistor and leave XOUT pin open.
Set “10010x00$_2$” (x = 0 or 1) to CPUM.

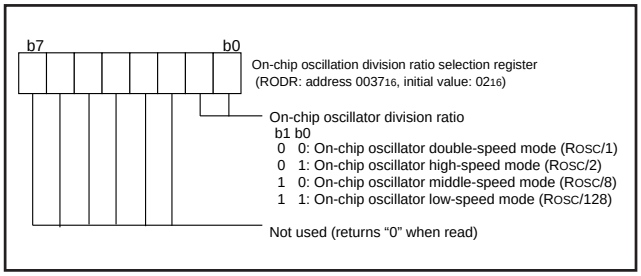
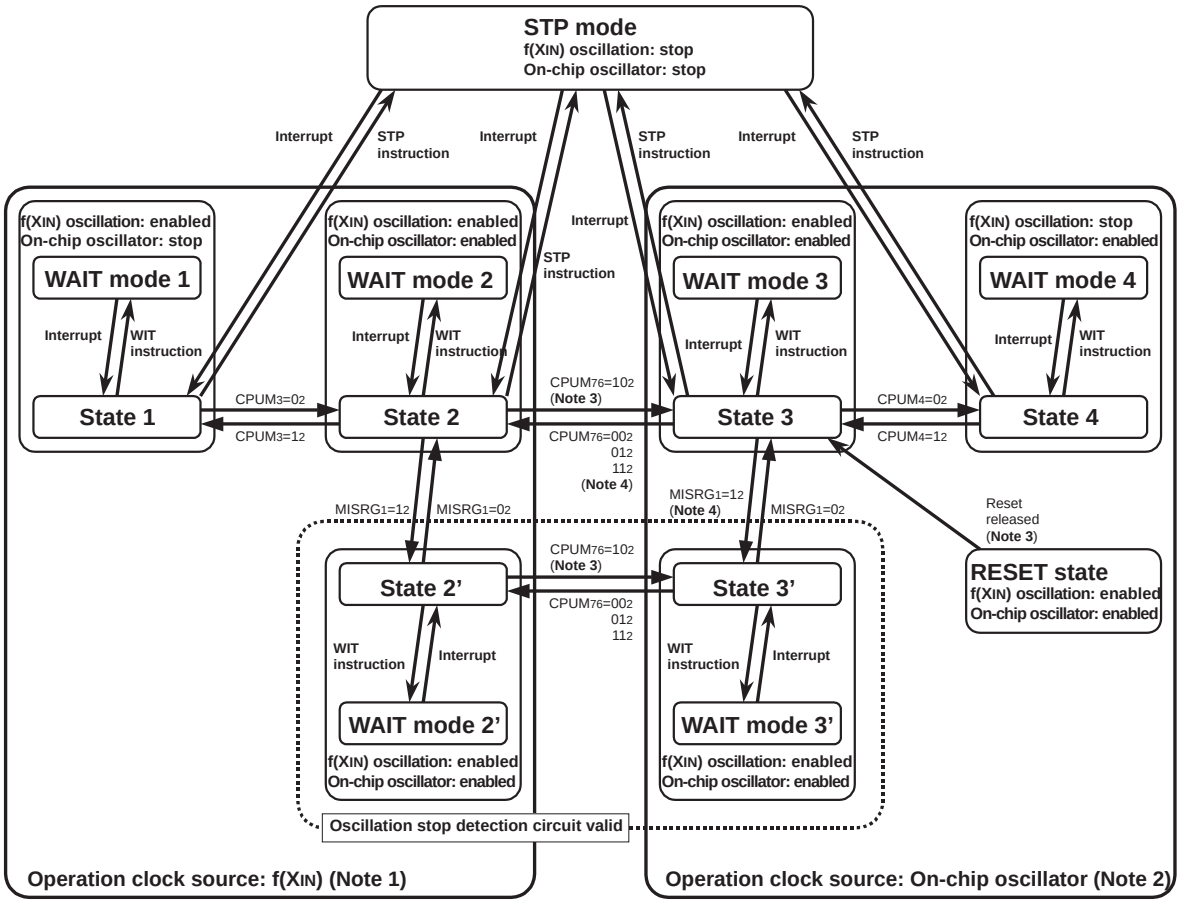


Fig. 79 Structure of on-chip oscillation division ratio selection register



Notes on switch of clock

(1) In operation clock = f(XIN), the following can be selected for the CPU clock division ratio.
f(XIN)/2 (high-speed mode)
f(XIN)/8 (middle-speed mode)
f(XIN) (double-speed mode, only at a ceramic oscillation)

(2) In operation clock = On-chip oscillator, the following can be selected for the CPU clock division ratio.
ROSC/1 (On-chip oscillator double-speed mode)
ROSC/2 (On-chip oscillator high-speed mode)
ROSC/8 (On-chip oscillator middle-speed mode)
ROSC/128 (On-chip oscillator low-speed mode)

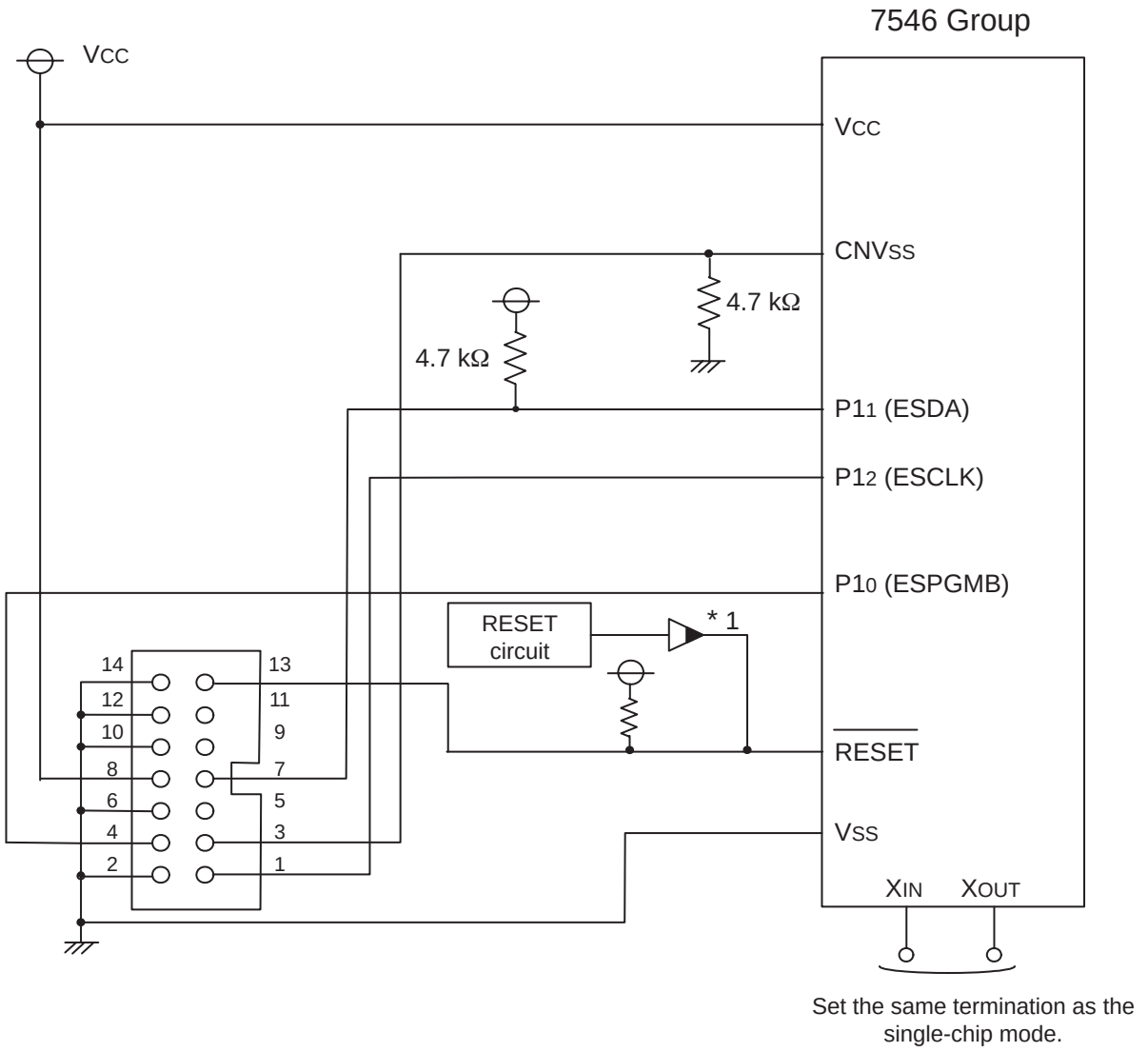
(3) After system is released from reset, and state transition of state 2 → state 3 and state transition of state 2' → state 3', ROSC/8 (On-chip oscillator middle-speed mode) is selected for CPU clock.

(4) Executing the state transition state 3 to 2 or state 3' to 2' after stabilizing XIN oscillation.

(5) When the state 2 → state 3 → state 4 is performed, execute the NOP instruction as shown below according to the division ratio of CPU clock.
1. CPUM76 = 102 (state 2 → state 3)
2. NOP instruction
Transition from Double-speed mode: NOP × 3
Transition from High-speed mode: NOP × 1
Transition from Middle-speed mode: NOP × 0
3. CPU4 = 12 (state 3 → state 4)

(6) When the state 3 → state 2 → state 1 is performed, execute the NOP instruction as shown below according to the division ratio of CPU clock.
1. CPUM76 = 002 or 012 or 112 (state 3 → state 2)
2. NOP instruction
Transition from On-chip oscillator double-speed mode: NOP × 4
Transition from On-chip oscillator high-speed mode: NOP × 2
Transition from On-chip oscillator middle-speed mode: NOP × 0
Transition from On-chip oscillator low-speed mode: NOP × 0
3. CPUM3 = 12 (state 2 → state 1)

Fig. 82 State transition



* 1: Open-collector buffer

Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 92 When using E8 programmer, connection example

ELECTRICAL CHARACTERISTICS of 7546 Group

Absolute Maximum Ratings

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	Ta = 25°C	300 (Note)	mW
T_{opr}	Operating temperature	–	–20 to 85	°C
T_{stg}	Storage temperature	–	–40 to 125	°C

Note : 200 mW for the PLQP0032GB-A package product.

Electrical Characteristics

Electrical characteristics (1)
(Vcc = 1.8 to 5.5V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
		I_{OH} = –1.0 mA V_{CC} = 1.8 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$ (Drive capacity = "L") $P1_0$–$P1_4$, $P2_0$–$P2_5$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA V_{CC} = 1.8 to 5.5 V			1.0	V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$ (Drive capacity = "H")	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA V_{CC} = 1.8 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 (Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD_0, $SCLK_0$, RxD_1, $SCLK_1$			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		μA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	μA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	μA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		μA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage	When clock stopped	1.6		5.5	V
R_{OSC}	On-chip oscillator oscillation frequency	V_{CC} = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
D_{OSC}	Oscillation stop detection circuit detection frequency	V_{CC} = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes1: $P1_1$ is measured when the $P1_1/TxD_1$ P-channel output disable bit of the UART1 control register (bit 4 of address $001B_{16}$) is "0".
$P0_5$ is measured when the $P0_5/TxD_2$ P-channel output disable bit of the UART2 control register (bit 4 of address 0031_{16}) is "0".
2: RxD_1, $SCLK_1$ and INT_0 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

A/D Converter Characteristics

A/D Converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy	Ta = 25 °C V_{CC} = V_{REF} = 2.7 to 5.5 V			± 3	LSB
t_{CONV}	Conversion time	AD conversion clock = f(X_{IN})/2			122	tc(X_{IN})
		AD conversion clock = f(X_{IN})			61	
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	μA
		V_{REF} = 3.0 V	30	90	120	
$I_{I(AD)}$	A/D port input current				5.0	μA

Note: AD conversion accuracy may be low under the following conditions;

(1) When the V_{REF} voltage is set to be lower than the V_{CC} voltage, an analog circuit in this microcomputer is affected by noise. The accuracy is lower than the case the V_{REF} voltage is the same as V_{CC} voltage.

(2) When the V_{REF} voltage is 3.0 V or less at the low temperature, the AD conversion accuracy may be very lower than at room temperature. When system is used at low temperature, that V_{REF} is 3.0 V or more is recommended.

Timing Requirements

Timing requirements (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			μs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input “H” pulse width (Note 1)	80			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input “L” pulse width (Note 1)	80			ns
$t_{C(SCLK1)}$	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	800			ns
$t_{WH(SCLK1)}$	Serial I/O1, serial I/O2 clock input “H” pulse width (Note 2)	370			ns
$t_{WL(SCLK1)}$	Serial I/O1, serial I/O2 clock input “L” pulse width (Note 2)	370			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1, serial I/O2 input set up time	220			ns
$t_{h(SCLK1–RxD1)}$	Serial I/O1, serial I/O2 input hold time	100			ns

Notes 1: As for CAP_0, CAP_1, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 0030_{16}) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Timing requirements (2)

(Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			μs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	500			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input “H” pulse width (Note 1)	230			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input “L” pulse width (Note 1)	230			ns
$t_{C(SCLK1)}$	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1, serial I/O2 clock input “H” pulse width (Note 2)	950			ns
$t_{WL(SCLK1)}$	Serial I/O1, serial I/O2 clock input “L” pulse width (Note 2)	950			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1, serial I/O2 input set up time	400			ns
$t_{h(SCLK1–RxD1)}$	Serial I/O1, serial I/O2 input hold time	200			ns

Notes 1: As for CAP_0, CAP_1, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 0030_{16}) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

3. Interrupt discrimination bit
Use an LDM instruction to clear to “0” an interrupt discrimination bit.
LDM #%0000XXXX, $0B
Set the following values to “X”
“0”: an interrupt discrimination bit to clear
“1”: other interrupt discrimination bits
Ex.) When a key-on wakeup interrupt discrimination bit is cleared;
LDM #%00001110 and $0B.

4. Interrupt discrimination bit and interrupt request bit
For key-on wakeup, UART1 bus collision detection, A/D conversion and Timer 1 interrupt, even if each interrupt valid bit (interrupt source set register (address $000A_{16}$)) is set “0: Invalid”, each interrupt discrimination bit (interrupt source discrimination register (address $000B_{16}$)) is set to “1: interrupt occurs” when corresponding interrupt request occurs.
But corresponding interrupt request bit (interrupt request registers 1, 2 (addresses $003C_{16}$, $003D_{16}$) is not affected.

Notes on Timers

1. When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

2. When a count source of timer X, timer A or timer B is switched, stop a count of the timer.

Notes on Timer X

1. $CNTR_0$ interrupt active edge selection
$CNTR_0$ interrupt active edge depends on the $CNTR_0$ active edge switch bit (bit 2 of timer X mode register (address $002B_{16}$)).
When this bit is “0”, the $CNTR_0$ interrupt request bit is set to “1” at the falling edge of $CNTR_0$ pin input signal. When this bit is “1”, the $CNTR_0$ interrupt request bit is set to “1” at the rising edge of $CNTR_0$ pin input signal.

2. Timer X count source selection
The f(X_{IN}) (frequency not divided) can be selected by the timer X count source selection bits (bits 1 and 0 of timer count source set register (address $002A_{16}$)) only when the ceramic oscillation or the on-chip oscillator is selected.
Do not select it for the timer X count source at the RC oscillation.

3. Pulse output mode
Set the direction register of port $P1_4$, which is also used as $CNTR_0$ pin, to output.
When the TX_{OUT} pin is used, set the direction register of port $P0_3$, which is also used as TX_{OUT} pin, to output.

4. Pulse width measurement mode
Set the direction register of port $P1_4$, which is also used as $CNTR_0$ pin, to input.

Notes on Timer A, B

1. Setting of timer value
When “1: Write to only latch” is set to the timer A (B) write control bit (bit 0 (bit 2) of timer X mode register (address $001D_{16}$)), written data to timer register is set to only latch even if timer is stopped or operating. Accordingly, in order to set the initial value for timer when it is stopped, set “0: Write to latch and timer simultaneously” to timer A (B) write control bit.

2. Read/write of timer A
Stop timer A to read/write its data in the following state;
X_{IN} oscillation selected by clock division ratio selection bits (bits 7 and 6 of CPU mode register (address $003B_{16}$)), and the on-chip oscillator output is selected as the timer A count source.

3. Read/write of timer B
Stop timer B to read/write its data in the following state;
X_{IN} oscillation selected by clock division ratio selection bits, the timer A underflow is selected as the timer B count source, and the on-chip oscillator output is selected as the timer A count source.

Notes on Output Compare

1. When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.

2. Do not write the same data to both of compare latch x0 (x=0, 1, 2, 3) and x1.

3. When setting value of the compare register is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to “L” or “H” level.
However, when setting value of another compare register is smaller than timer setting value, this compare match signal is generated. Accordingly, if the corresponding compare latch y (y=00, 01, 10, 11, 20, 21, 30, 31) interrupt source bit is set to “1” (valid), compare match interrupt request occurs.

4. When the compare x trigger enable bit is cleared to “0” (disabled), the match trigger to the waveform output circuit is disabled. Accordingly, the output waveform can be fixed to “L” or “H” level.
However, in this case, the compare match signal is generated. Accordingly, if the corresponding compare latch y (y=00, 01, 10, 11, 20, 21, 30, 31) interrupt source bit is set to “1” (valid),compare match interrupt request occurs.

3. Notes common to clock synchronous serial I/O and UART

(1) Set the serial I/Oi (i=1, 2) control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0.”

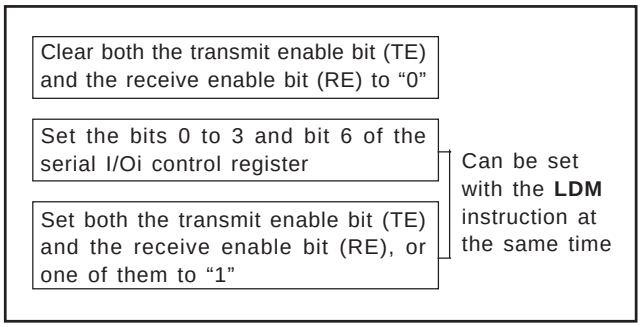


Fig. 6 Sequence of setting serial I/Oi control register again

(2) The transmit shift completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(3) When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set “1” to the transmit enable bit while the SCLKi is “H” state. Also, write to the transmit buffer register while the SCLKi is “H” state.

(4) When the transmit interrupt is used, set as the following sequence.

① Serial I/Oi transmit interrupt enable bit is set to “0” (disabled).
② Serial I/Oi transmit enable bit is set to “1”.
③ Serial I/Oi transmit interrupt request bit is set to “0” after 1 or more instructions have been executed.
④ Serial I/Oi transmit interrupt enable bit is set to “1” (enabled).

<Reason>

When the transmit enable bit is set to “1”, the transmit buffer empty flag and transmit shift completion flag are set to “1”.
Accordingly, even if the timing when any of the above flags is set to “1” is selected for the transmit interrupt source, interrupt request occurs and the transmit interrupt request bit is set.

(5) Write to the baud rate generator (BRGi) while the transmit/receive operation is stopped.

Notes on Serial I/O1

1. I/O pin function when serial I/O1 is enabled.

The pin functions of P12/SCLK1 and P13/SRDY1 are switched to as follows according to the setting values of a serial I/O1 mode selection bit (bit 6 of serial I/O1 control register (address $001A_{16}$)) and a serial I/O1 synchronous clock selection bit (bit 1 of serial I/O1 control register).

(1) Serial I/O1 mode selection bit → “1” :
Clock synchronous type serial I/O is selected.
• Setup of a serial I/O1 synchronous clock selection bit
“0” : P12 pin turns into an output pin of a synchronous clock.
“1” : P12 pin turns into an input pin of a synchronous clock.
• Setup of a SRDY1 output enable bit (SRDY)
“0” : P13 pin can be used as a normal I/O pin.
“1” : P13 pin turns into a SRDY1 output pin.

(2) Serial I/O1 mode selection bit → “0” :
Clock asynchronous (UART) type serial I/O is selected.
• Setup of a serial I/O1 synchronous clock selection bit
“0”: P12 pin can be used as a normal I/O pin.
“1”: P12 pin turns into an input pin of an external clock.
• When clock asynchronous (UART) type serial I/O is selected, it functions P13 pin. It can be used as a normal I/O pin.

Note on Bus Collision Detection

When serial I/O1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

Notes on Serial I/O2

1. I/O pin function when serial I/O2 is enabled

The pin functions of P06/SCLK2 and P07/SRDY2 are switched to as follows according to the setting values of a serial I/O2 mode selection bit (bit 6 of serial I/O2 control register (address 0030_{16})) and a serial I/O2 synchronous clock selection bit (bit 2 of serial I/O2 control register).

(1) Serial I/O2 mode selection bit → “1” :
Clock synchronous type serial I/O is selected.
• Setup of a serial I/O2 synchronous clock selection bit
“0” : P06 pin turns into an output pin of a synchronous clock.
“1” : P06 pin turns into an input pin of a synchronous clock.
• Setup of a SRDY2 output enable bit (SRDY)
“0” : P07 pin can be used as a normal I/O pin.
“1” : P07 pin turns into a SRDY2 output pin.

(2) Serial I/O2 mode selection bit → “0” :
Clock asynchronous (UART) type serial I/O is selected.
• Setup of a serial I/O2 synchronous clock selection bit
“0”: P06 pin can be used as a normal I/O pin.
“1”: P06 pin turns into an input pin of an external clock.
• When clock asynchronous (UART) type serial I/O is selected, it functions P07 pin. It can be used as a normal I/O pin.