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#### Understanding Embedded - PLDs (Programmable Logic Devices)

Embedded - PLDs, or Programmable Logic Devices, are a type of digital electronic component used to build reconfigurable digital circuits. Unlike fixed-function logic devices, PLDs can be programmed to perform specific functions by the user. This flexibility allows designers to customize the logic to meet the exact needs of their applications, making PLDs a crucial component in modern embedded systems.

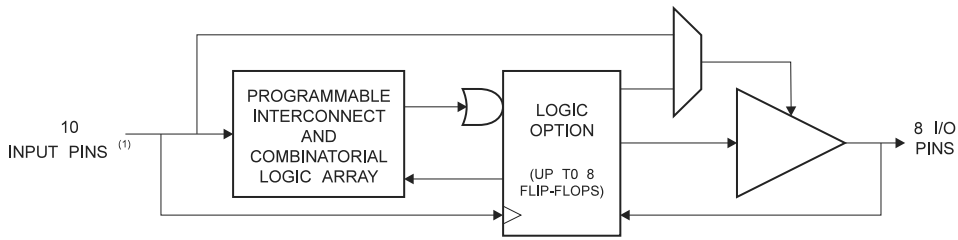
#### Applications of Embedded - PLDs (Programmable Logic Devices)

The versatility of PLDs makes them suitable for a wide range of applications. In consumer electronics, PLDs are used to enhance the functionality and performance of

#### Details

Product Status	Obsolete
Programmable Type	EE PLD
Number of Macrocells	8
Voltage - Input	5V
Speed	7.5 ns
Mounting Type	Surface Mount
Package / Case	20-LCC (J-Lead)
Supplier Device Package	20-PLCC (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf16v8c-7jc">https://www.e-xfl.com/product-detail/microchip-technology/atf16v8c-7jc</a>

Figure 0-1. Block diagram

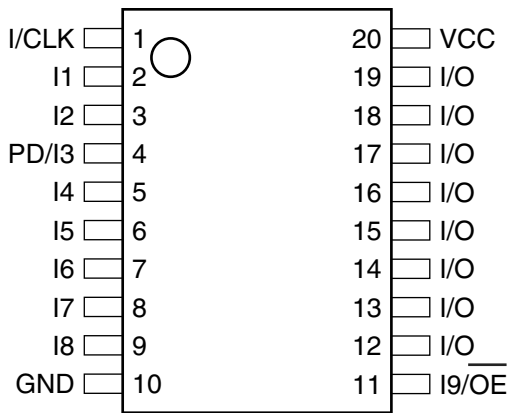


Note: 1. Includes optional PD control pin

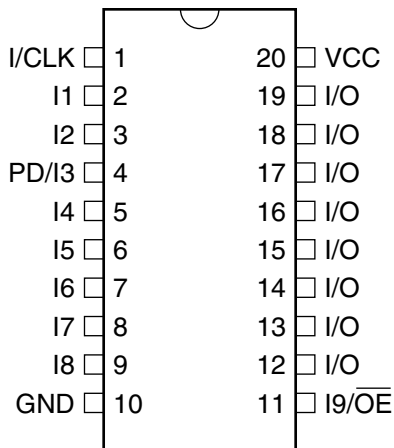
Figure 0-2. Pin configurations

Pin name	Function
CLK	Clock
I	Logic inputs
I/O	Bidirectional buffers
$\overline{OE}$	Output enable
V <sub>CC</sub>	+5V supply
PD	Power-down

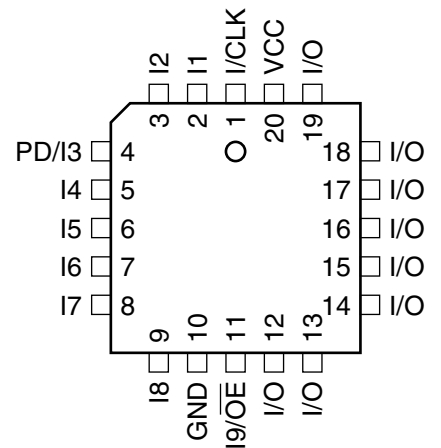
TSSOP  
Top view



DIP/SOIC  
Top view



PLCC  
Top view



## 1. Absolute maximum ratings\*

Temperature under bias . . . . .	-40°C to +85°C
Storage temperature . . . . .	-65°C to +150°C
Voltage on any pin with respect to ground . . . . .	-2.0V to +7.0V <sup>(1)</sup>
Voltage on input pins with respect to ground during programming . . . . .	-2.0V to +14.0V <sup>(1)</sup>
Programming voltage with respect to ground . . . . .	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20ns.

## 2. DC and AC characteristics

Table 2-1. DC and AC operating conditions

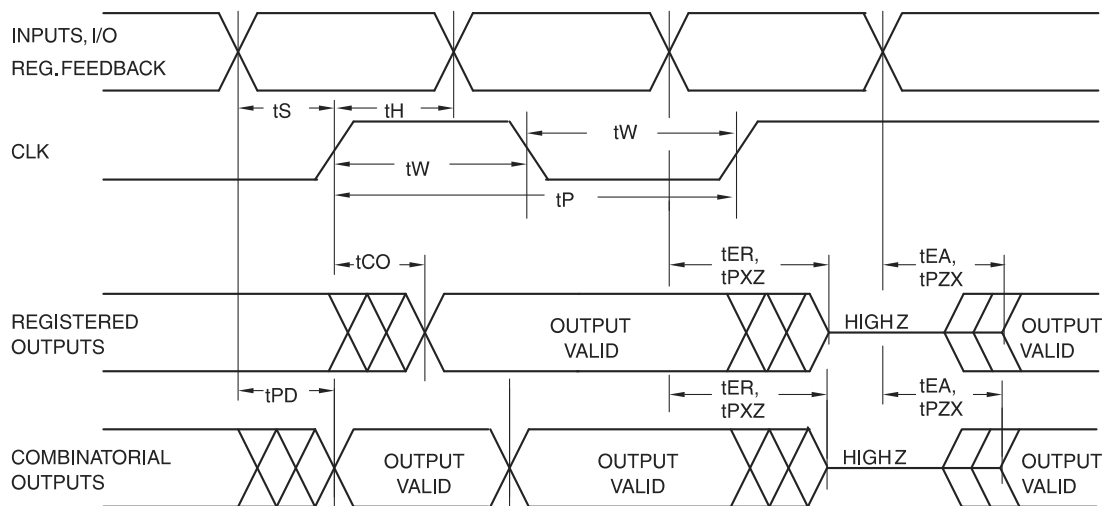
	Commercial	Industrial
Operating temperature (Ambient)	0°C - 70°C	-40°C - 85°C
$V_{CC}$ power supply	5V ± 5%	5V ± 10%

Table 2-2. DC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{IL}$	Input or I/O low leakage current	$0 \leq V_{IN} \leq V_{IL} (Max)$			-10.0	µA
$I_{IH}$	Input or I/O high leakage current	$3.5 \leq V_{IN} \leq V_{CC}$			10.0	µA
$I_{CC1}^{(1)}$	Power supply current, standby	15MHz, $V_{CC} = Max$ , $V_{IN} = 0$ , $V_{CC}$ , outputs open	Com.		115	mA
			Ind.		130	mA
$I_{PD}$	Power supply current, Power-down mode	$V_{CC} = Max$ , $V_{IN} = 0$ , $V_{CC}$	Com.	10	100	µA
			Ind.	10	105	µA
$I_{OS}$	Output short circuit current	$V_{OUT} = 0.5V$ ; $V_{CC} = 5V$ ; $T_A = 25^\circ C$			-150	mA
$V_{IL}$	Input low voltage	$Min < V_{CC} < Max$	-0.5		0.8	V
$V_{IH}$	Input high voltage		2.0		$V_{CC} + 1$	V
$V_{OL}$	Output low voltage	$V_{CC} = Min$ ; All outputs $I_{OL} = 24mA$			0.5	V
$V_{OH}$	Output high voltage	$V_{CC} = Min$ $I_{OL} = -4.0mA$	2.4			V
$I_{OL}$	Output low current	$V_{CC} = Min$	Com.	24.0		mA
			Ind.	12.0		mA
$I_{OH}$	Output high current	$V_{CC} = Min$	-4.0			mA

Note: 1. All  $I_{CC}$  parameters measured with outputs open

Figure 3. AC waveforms



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

Table 3-1. AC characteristics

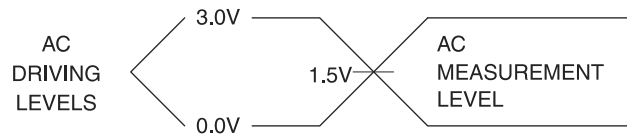
Symbol	Parameter	-5		-7		-10		Units
		Min	Max	Min	Max	Min	Max	
$t_{PD}$	Input or feedback to non-registered output	1	5	3	7.5	3	10	ns
$t_{CF}$	Clock to feedback		3		3		6	ns
$t_{CO}$	Clock to output	1	4	2	5	2	7	ns
$t_S$	Input or feedback setup time	3		5		7.5		ns
$t_H$	Input hold time	0		0		0		ns
$t_P$	Clock period	6		8		12		ns
$t_W$	Clock width	3		4		6		ns
$f_{MAX}$	External feedback $1/(t_S + t_{CO})$		142		100		68	MHz
	Internal feedback $1/(t_S + t_{CF})$		166		125		74	MHz
	No feedback $1/(t_P)$		166		125		83	MHz
$t_{EA}$	Input to output enable – product term	2	6	3	9	3	10	ns
$t_{ER}$	Input to output disable – product term	2	5	2	9	2	10	ns
$t_{PZX}$	$\overline{OE}$ pin to output enable	2	5	2	6	2	10	ns
$t_{PZ}$	$\overline{OE}$ pin to output disable	1.5	5	1.5	6	1.5	10	ns

Table 3-2. Power-down AC characteristics<sup>(1)(2)(3)</sup>

Symbol	Parameter	-5		-7		-10		Units
		Min	Max	Min	Max	Min	Max	
$t_{VDH}$	Valid Input before PD High	5.0		7.5		10		ns
$t_{GVDH}$	Valid $\overline{OE}$ before PD High	0		0		0		ns
$t_{CVDH}$	Valid Clock before PD High	0		0		0		ns
$t_{DHIX}$	Input Don't Care after PD High		5.0		7.5		10	ns
$t_{DHGX}$	$\overline{OE}$ Don't Care after PD High		5.0		7.5		10	ns
$t_{DHCX}$	Clock Don't Care after PD High		5.0		7.5		10	ns
$t_{DLIV}$	PD Low to Valid Input		5.0		7.5		10	ns
$t_{DLGV}$	PD Low to Valid $\overline{OE}$		15.0		20.0		25	ns
$t_{DLCV}$	PD Low to Valid Clock		15.0		20.0		25	ns
$t_{DLOV}$	PD Low to Valid Output		20.0		25.0		30	ns

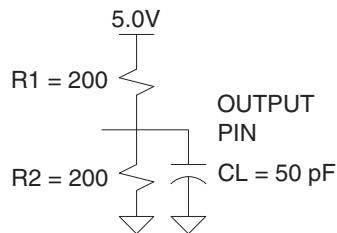
- Note:
1. Output data is latched and held
  2. HI-Z outputs remain HI-Z
  3. Clock and input transitions are ignored

#### 4. Input test waveforms and measurement levels:



$t_R, t_F < 1.5\text{ns}$  (10% to 90%)

#### 5. Output test loads



#### 6. Pin capacitance

Table 6-1. Pin capacitance

	Typ	Max	Units	Conditions
$C_{IN}$	5	8	pF	$V_{IN} = 0V$
$C_{OUT}$	6	8	pF	$V_{OUT} = 0V$

- Note:
1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## 7. Power-up reset

Registers of the ATF16V8C are designed to reset during power-up. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

1. The  $V_{CC}$  rise must be monotonic, from below 0.7V
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during  $t_{PR}$

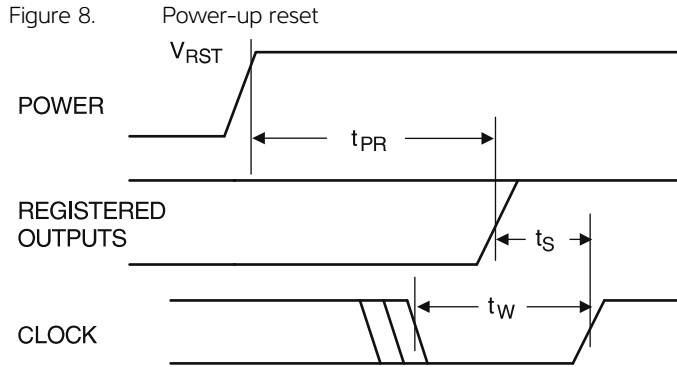


Table 8-1. Power-up reset parameters

Parameter	Description	Typ	Max	Units
$t_{PR}$	Power-up Reset Time	600	1,000	ns
$V_{RST}$	Power-up Reset Voltage	3.8	4.5	V

## 9. Power-down mode

The ATF16V8C includes an optional pin controlled powerdown feature. Device pin 4 may be configured as the power-down pin. When this feature is enabled and the power-down pin is high, total current consumption drops to less than 100 $\mu$ A. In the power-down mode, all output data and internal logic states are latched and held. All registered and combinatorial output data remains valid. Any outputs that were in a high-Z state at the onset of power-down will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. The input and I/O pin-keeper circuits remain active to insure that pins do not float to indeterminate levels. This helps to further reduce system power.

Selection of the power-down option is specified in the ATF16V8C logic design file. The logic compiler will include this option selection in the otherwise standard 16V8 JEDEC fuse file. When the power-down feature is not specified in the design file, pin 4 is available as a logic input, and there is no power-down pin. This allows the ATF16V8C to be programmed using any existing standard 16V8 fuse file.

Note: Some programmers list the JEDEC-compatible 16V8C (No PD used) separately from the non-JEDEC compatible 16V8CEXT. (EXT for extended features.)

## 10. Registered output preload

Registers of the ATF16V8C are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by approved programmers.

## 11. Security fuse usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit user signature remains accessible.

The security fuse will be programmed last, as its effect is immediate.

## 12. Input and I/O pin-keeper circuits

The ATF16V8C contains internal input and I/O pin-keeper circuits. These circuits allow each ATF16V8C pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 $\mu$ A.

Figure 13. Input diagram

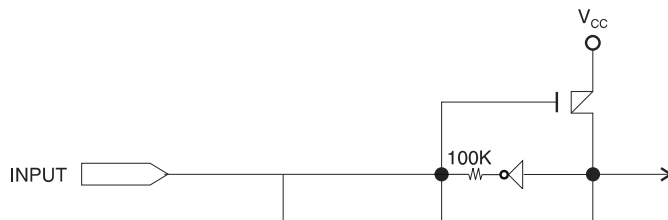
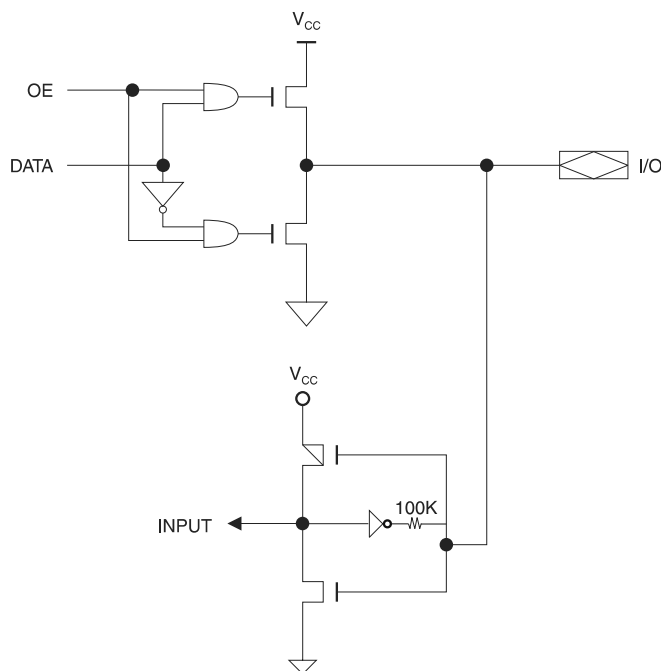


Figure 14. I/O diagram



In **simple mode**, all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

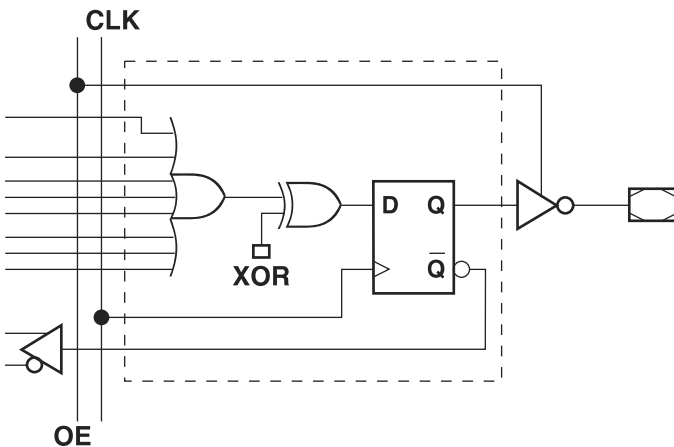
## 16.1 Atmel ATF16V8C registered mode

**PAL device emulation/PAL replacement.** The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the  $\overline{OE}$  pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

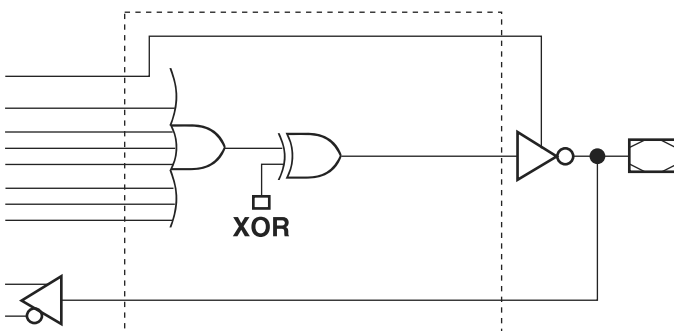
16R8	16RP8
16R6	16RP6
16R4	16RP4

Figure 17. Registered configuration for registered mode<sup>(1)(2)</sup>



- Notes:
1. Pin 1 controls common CLK for the registered outputs.  
Pin 11 controls common  $\overline{OE}$  for the registered outputs.  
Pin 1 and Pin 11 are permanently configured as CLK and  $\overline{OE}$ .
  2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

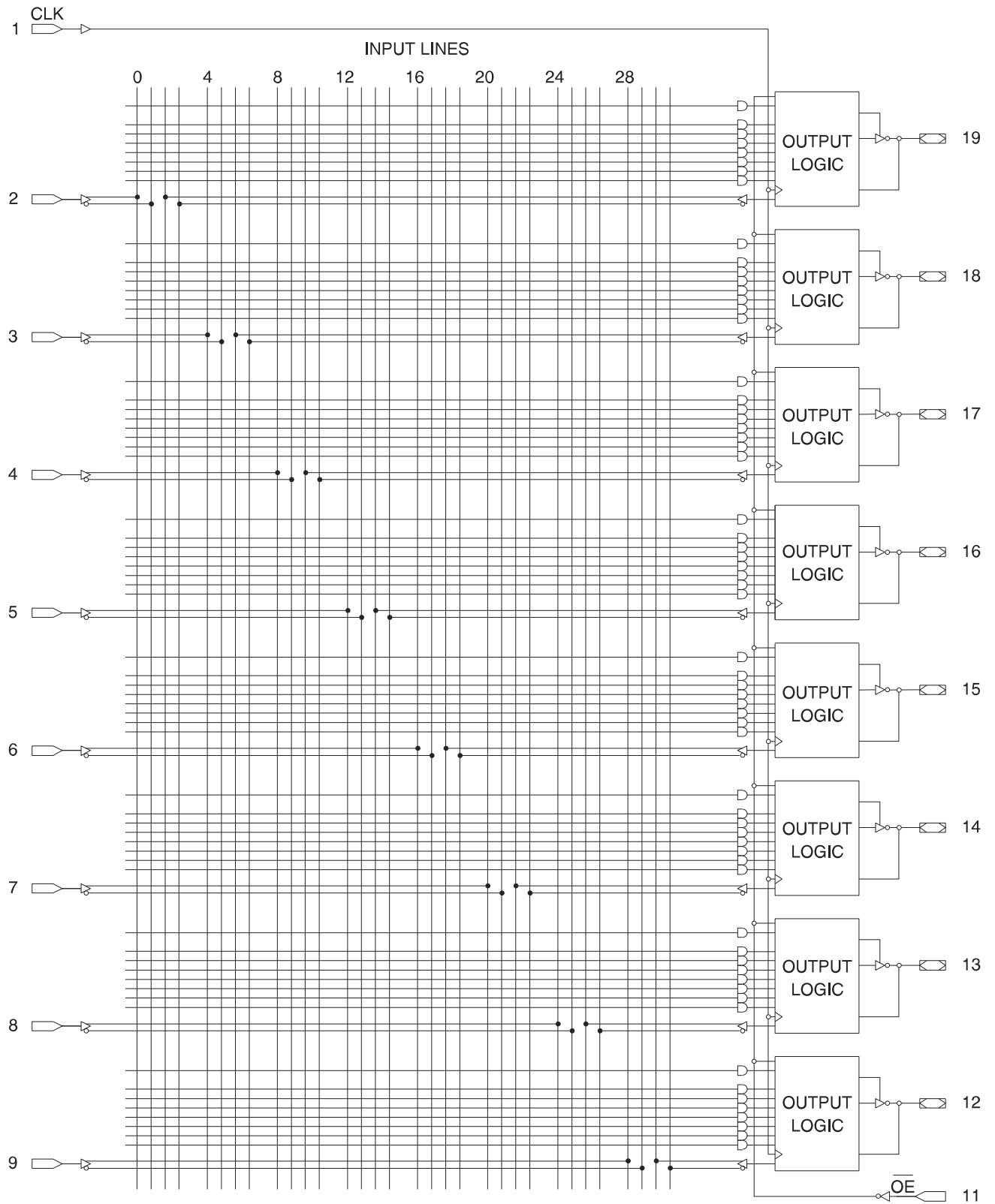
Figure 18. Combinatorial configuration for registered mode<sup>(1)(2)</sup>



- Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and  $\overline{OE}$ .
  2. The development software configures all the architecture control bits and checks for proper pin usage automatically.



Figure 19. Registered mode logic diagram



Note: \* Input not available if power-down mode is enabled

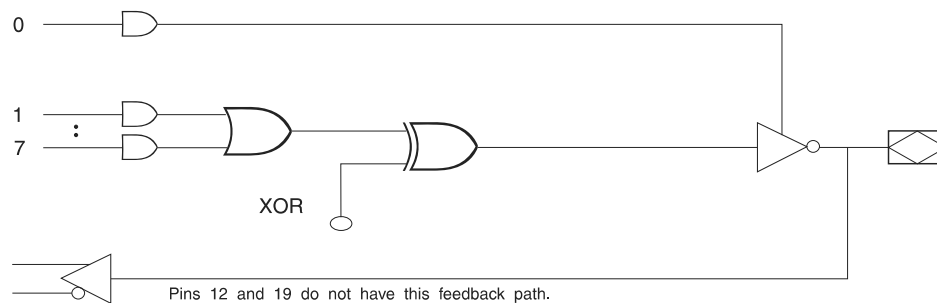
## 20. Atmel ATF16V8C complex mode

**PAL device emulation/PAL replacement.** In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an  $\overline{OE}$  requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8  
16H8  
16P8

Figure 21. Complex Mode Option



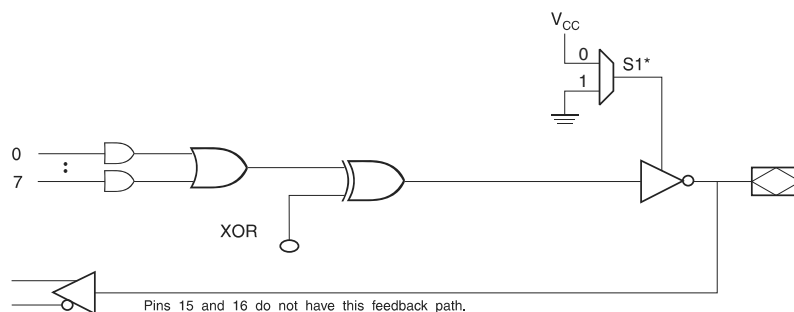
## 22. Atmel ATF16V8C simple mode

**PAL device emulation/PAL replacement.** In the simple mode, eight product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without  $\overline{OE}$  control. The following simple PALs can be emulated using this mode:

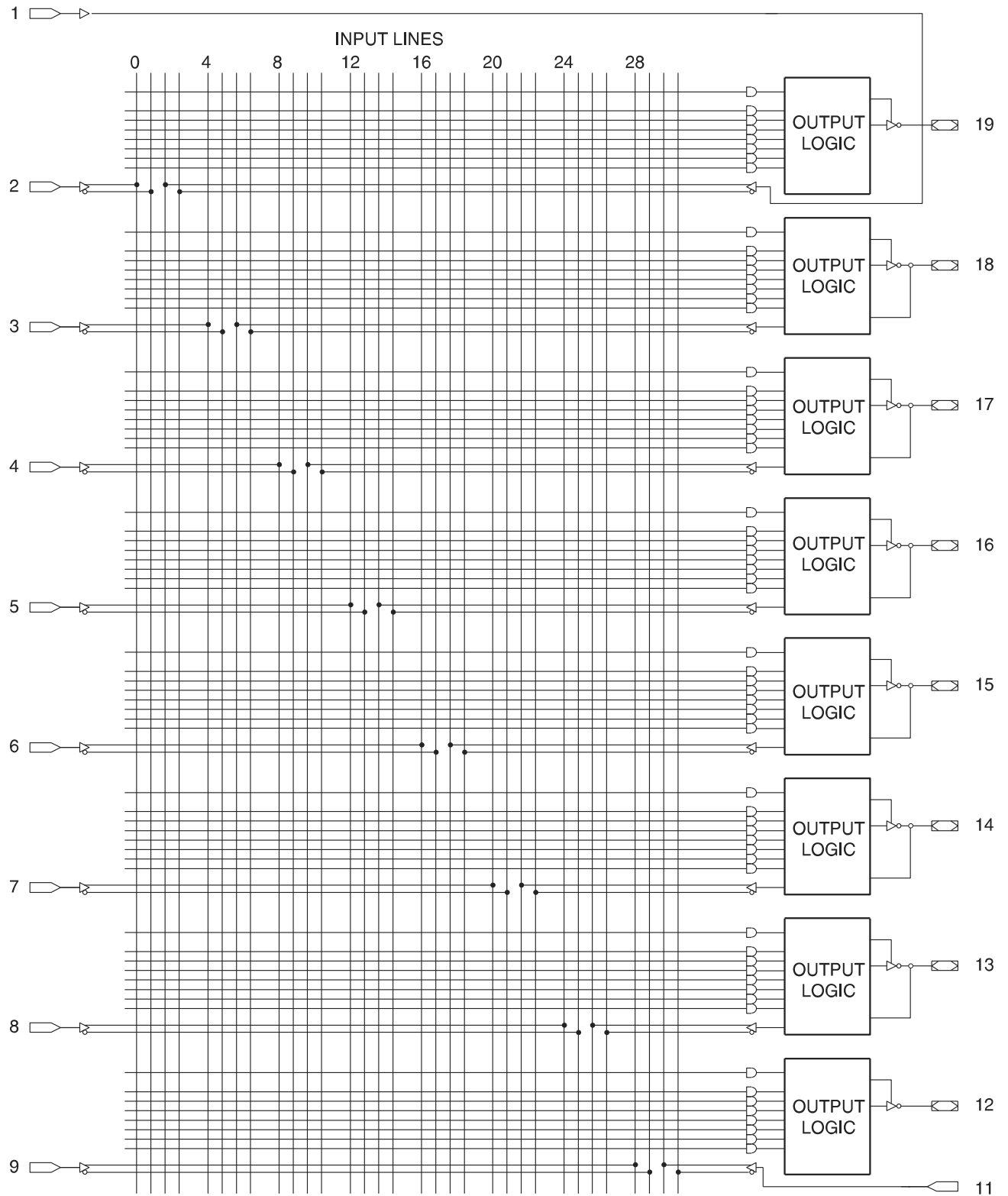
10L8 10H8 10P8  
12L6 12H6 12P6  
14L4 14H4 14P4  
16L2 16H2 16P2

Figure 23. Simple mode option



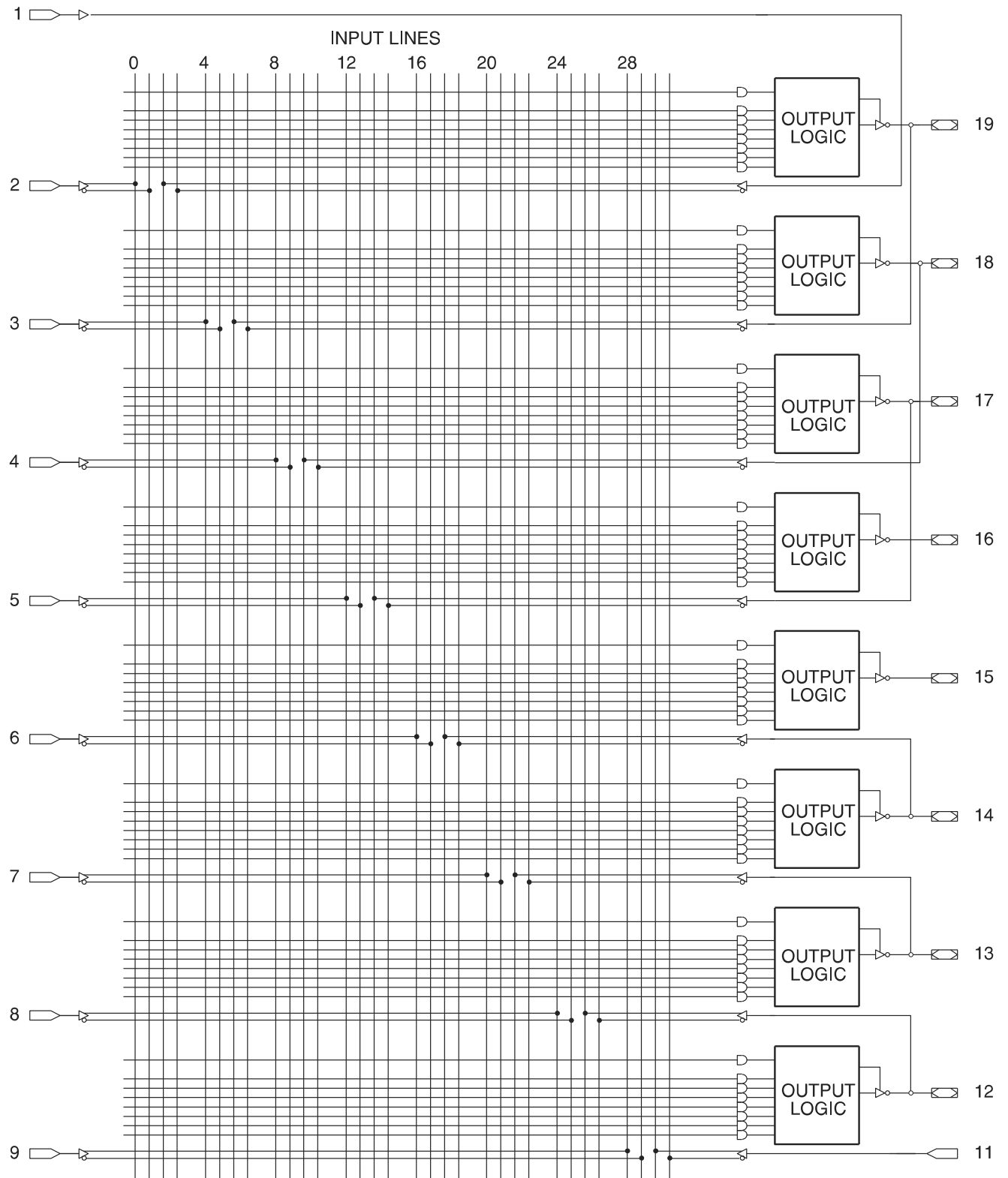
\* - Pins 15 and 16 are always enabled.

Figure 24. Complex mode logic diagram

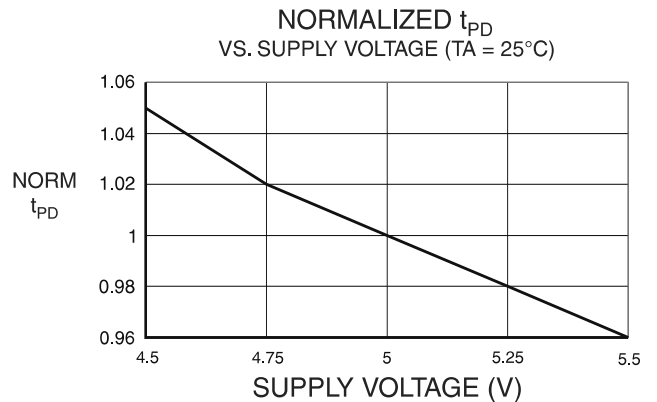
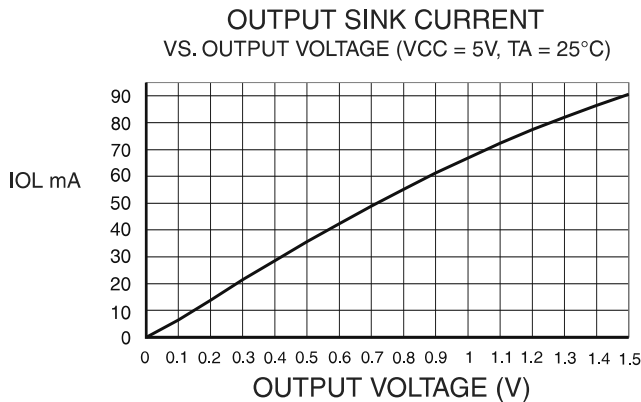
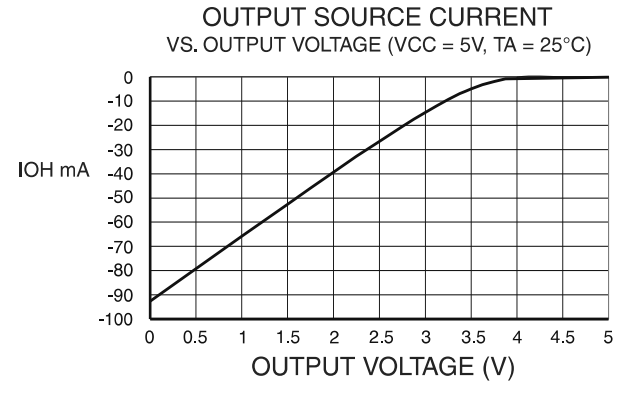
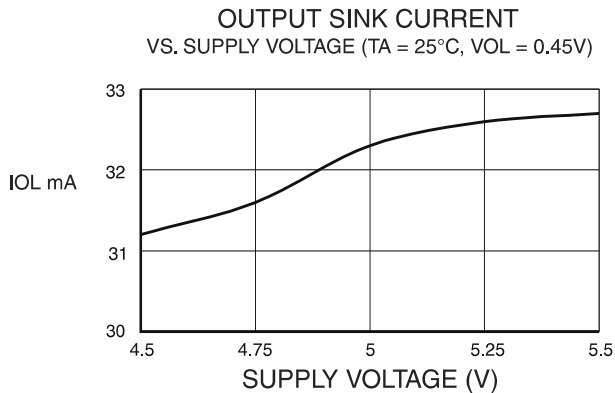
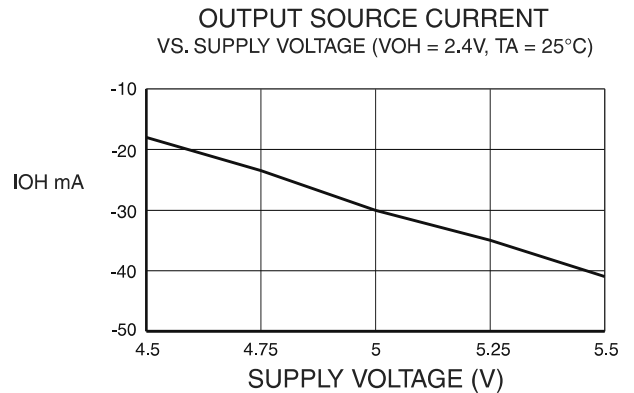
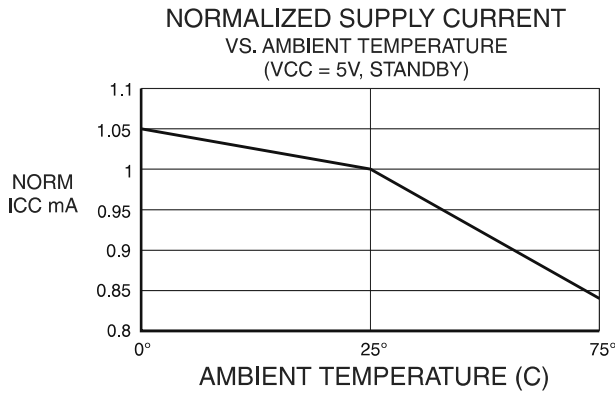
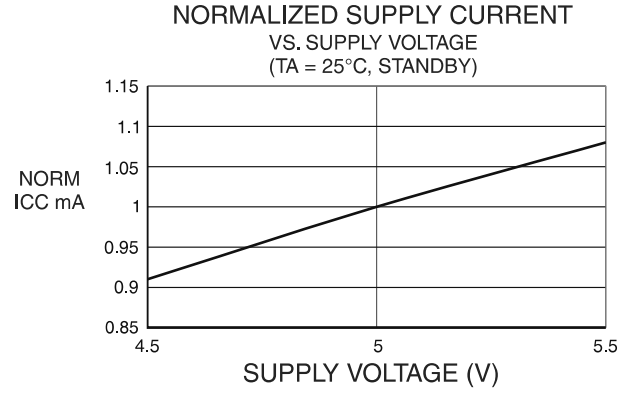
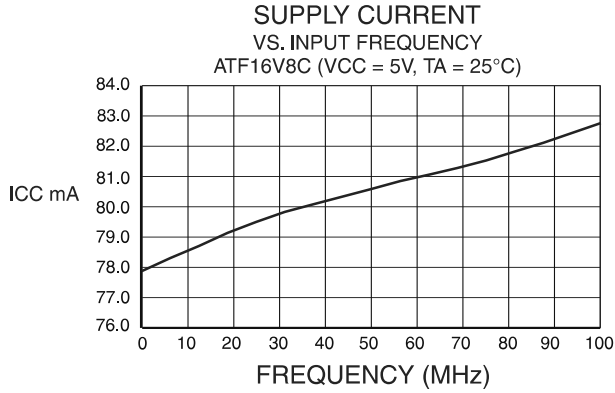


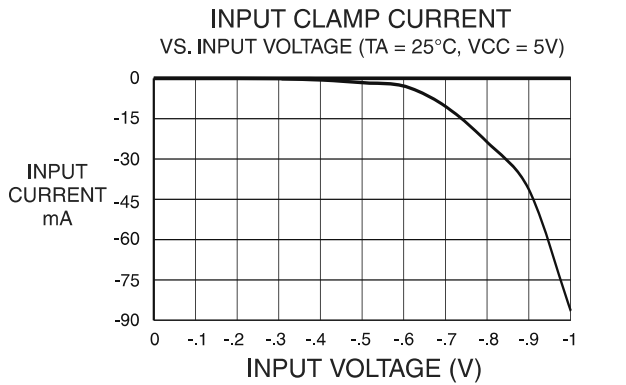
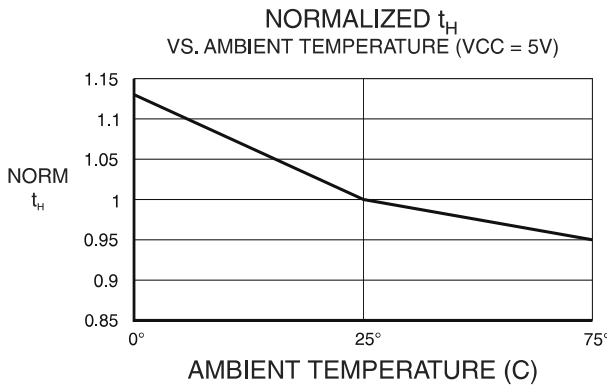
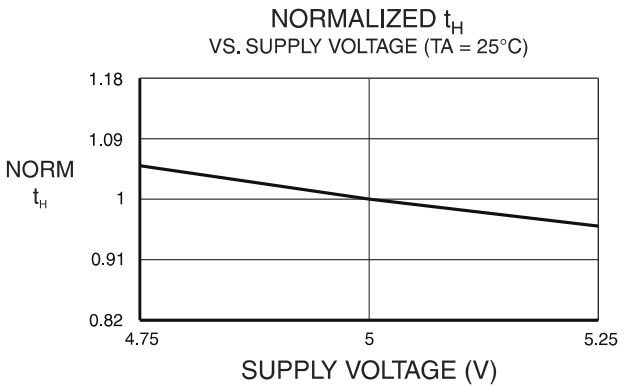
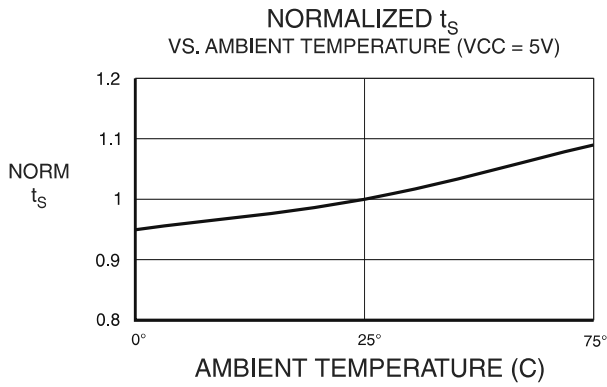
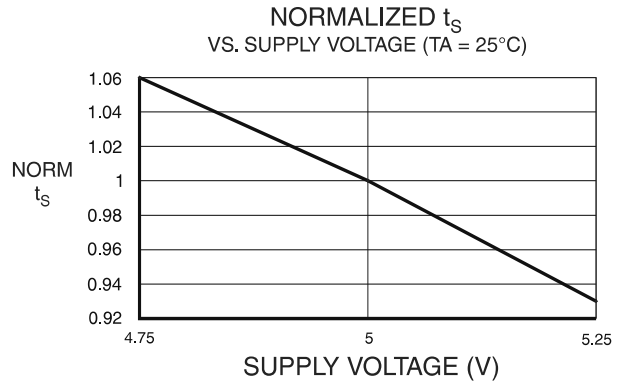
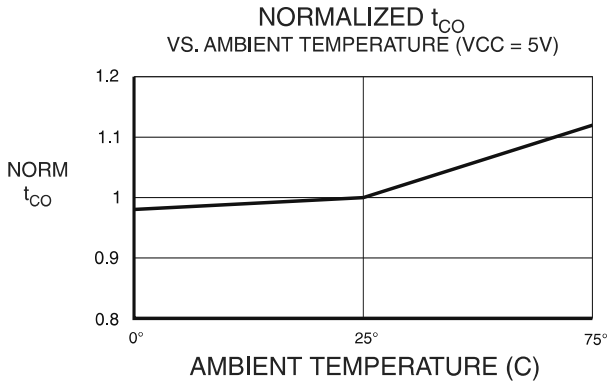
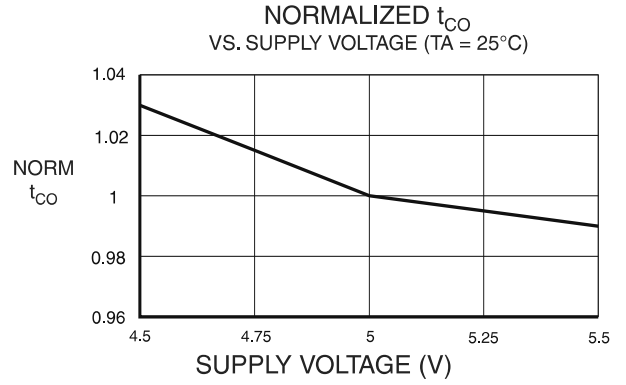
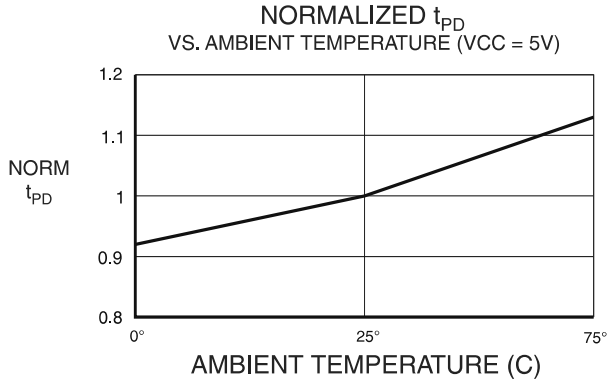
Note: \* Input not available if power-down mode is enabled

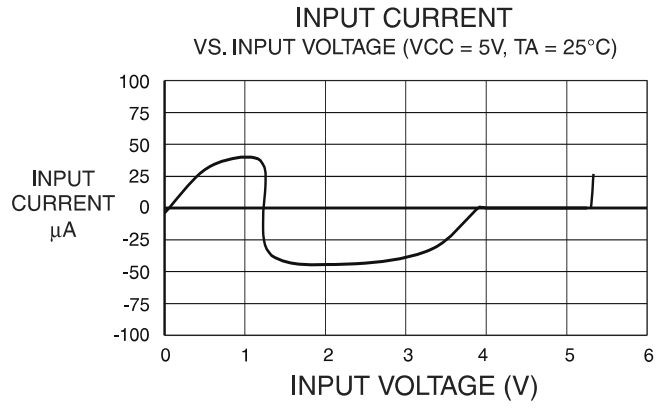
Note: Simple mode logic diagram



Note: \* Input not available if power-down mode is enabled







## 25. Ordering information

t <sub>PD</sub> (ns)	t <sub>S</sub> (ns)	t <sub>CO</sub> (ns)	Atmel ordering code*	Package	Operation range
5	3	4	ATF16V8C-5JX	20J	Commercial (0°C to 70°C)
7.5	5	5	ATF16V8C-7JU ATF16V8C-7PU ATF16V8C-7SU	20J 20P3 20S	Industrial (-40°C to 85°C)
5	3	4	ATF16V8C-5JC	20J	Commercial (0°C to 70°C)
7.5	5	5	ATF16V8C-7JC ATF16V8C-7PC ATF16V8C-7SC ATF16V8C-7XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
			ATF16V8C-7JI ATF16V8C-7PI ATF16V8C-7SI ATF16V8C-7XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)
10	7.5	7	ATF16V8C-10JI	20J	Industrial (-40°C to 85°C)

## Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7ns "C" = 10ns "I") and de-rate power by 30%.

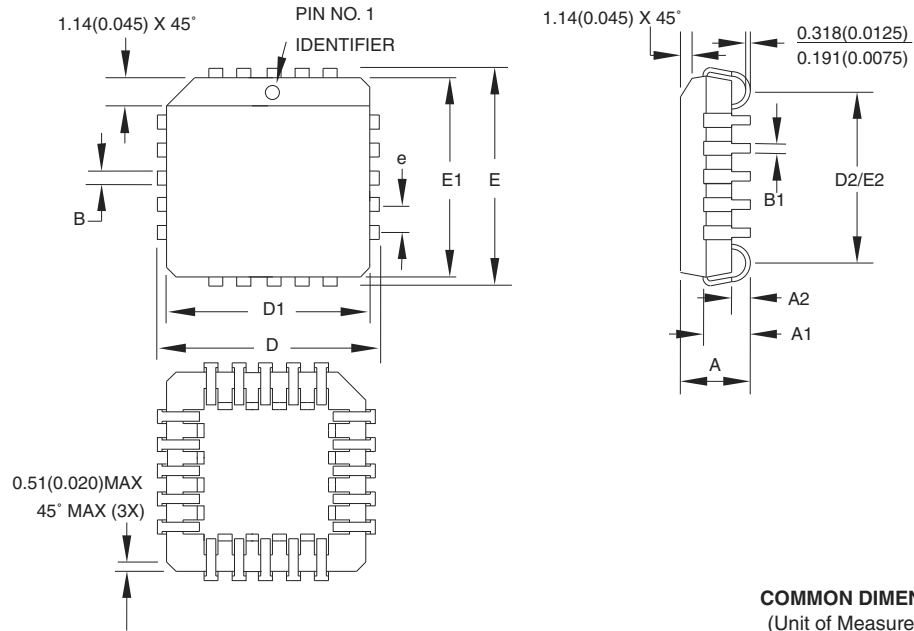
- Notes:
- \*Shaded parts are being obsoleted in 2011
  - The suffix, "U" and "X" as part of the ordering code, implies the package is ROHS compliant and lead free

Package type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-Wing Small Outline (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)



## 26. Package Drawings

### 20J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

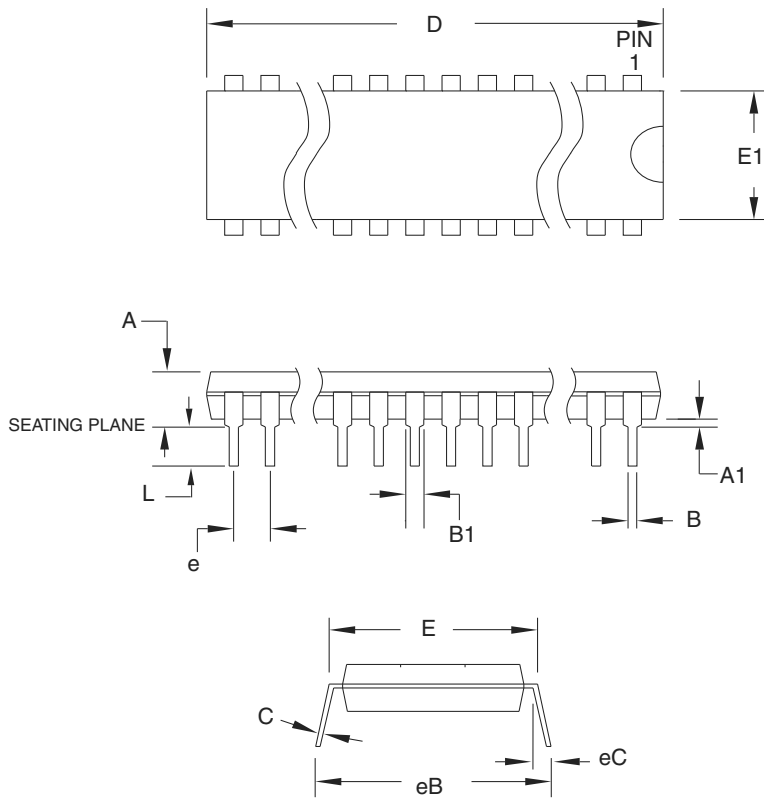
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
  2. Dimensions  $D1$  and  $E1$  do not include mold protrusion. Allowable protrusion is  $.010''(0.254 \text{ mm})$  per side. Dimension  $D1$  and  $E1$  include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is  $0.004''(0.102 \text{ mm})$  maximum.

10/04/01

2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)</b>	<b>DRAWING NO.</b> 20J	<b>REV.</b> B
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20P3 – PDIP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.  
 2. Dimensions D and E1 do not include mold Flash or Protrusion.  
 Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/23/04

2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b>	<b>DRAWING NO.</b> 20P3	<b>REV.</b> D
	20P3, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)		

# 20S – SOIC

Top View

End View

Side View

**COMMON DIMENSIONS**  
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

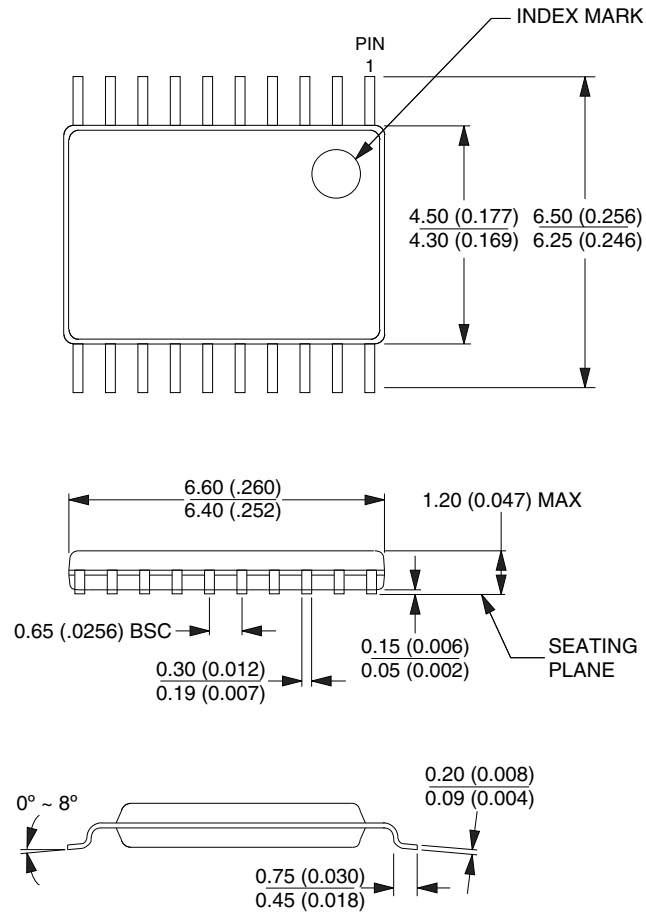
Notes.

1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>20S2</b> , 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	<b>DRAWING NO.</b> 20S2	<b>REV.</b> B
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20X – TSSOP

Dimensions in Millimeters and (Inches).  
 Controlling dimension: Millimeters.  
 JEDEC Standard MO-153 AC



10/23/03

2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>20X</b> , (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	<b>DRAWING NO.</b> 20X	<b>REV.</b> C
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