Welcome to E-XFL.COM

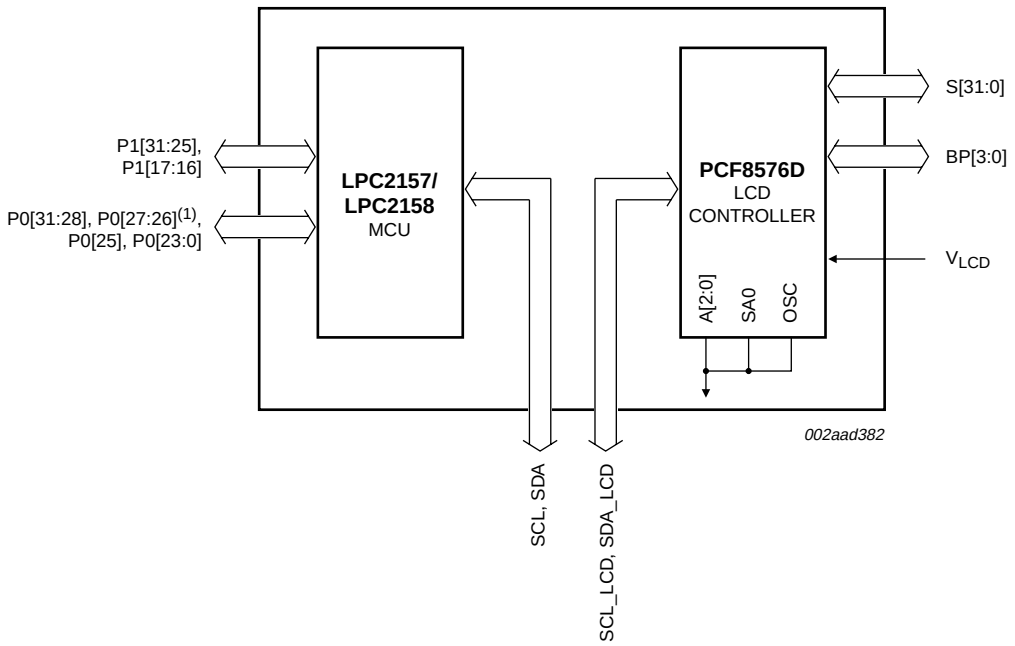
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 14x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2158fbd100-551

4. Block diagram



(1) LPC2157 only.

Fig 1. Block diagram of LPC2157/2158

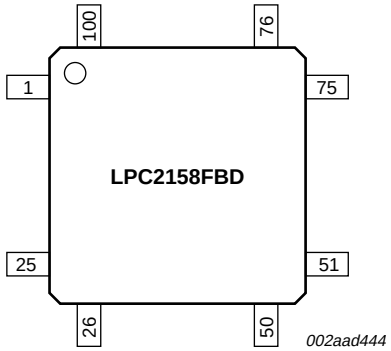


Fig 5. Pin configuration for LPC2158

5.2 Pin description

Table 2. Pin description LPC2157

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0[31] is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pin P0[24] is not available.
P0[0]/TXD0/ PWM1	7[1]	I/O	**P0[0] —** General purpose input/output digital pin (GPIO).
		O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	9[2]	I/O	**P0[1] —** General purpose input/output digital pin (GPIO).
		I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0[2]/SCL0/ CAP0[0]	10[3]	I/O	**P0[2] —** General purpose input/output digital pin (GPIO).
		I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA0/ MAT0[0]/EINT1	14[3]	I/O	**P0[3] —** General purpose input/output digital pin (GPIO).
		I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]/AD0[6]	15[4]	I/O	**P0[4] —** General purpose input/output digital pin (GPIO).
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		I	**AD0[6] —** ADC 0, input 6.
P0[5]/MISO0/ MAT0[1]/AD0[7]	17[4]	I/O	**P0[5] —** General purpose input/output digital pin (GPIO).
		I/O	**MISO0 —** Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
		I	**AD0[7] —** ADC 0, input 7.

Table 2. Pin description LPC2157 *…continued*

Symbol	Pin	Type	Description
P0[27]/AD0[0]/ CAP0[1]/MAT0[1]	99[7]	I/O	**P0[27] —** General purpose input/output digital pin (GPIO).
		I	**AD0[0] —** ADC 0, input 0. This analog input is always connected to its pin.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[28]/AD0[1]/ CAP0[2]/MAT0[2]	1[4]	I/O	**P0[28] —** General purpose input/output digital pin (GPIO).
		I	**AD0[1] —** ADC 0, input 1.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AD0[2]/ CAP0[3]MAT0[3]	2[4]	I/O	**P0[29] —** General purpose input/output digital pin (GPIO).
		I	**AD0[2] —** ADC 0, input 2.
		I	**CAP0[3] —** Capture input for Timer 0, channel 3.
		O	**MAT0[3] —** Match output for Timer 0, channel 3.
P0[30]/AD0[3]/ EINT3/CAP0[0]	3[4]	I/O	**P0[30] —** General purpose input/output digital pin (GPIO).
		I	**AD0[3] —** ADC 0, input 3.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[31]	5[6]	O	**P0[31] —** General purpose output only digital pin.
P1[0] to P1[31]		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 and 18 through 24 of port 1 are not available.
P1[16]	4[6]	I/O	**P1[16] —** General purpose input/output digital pin (GPIO).
P1[17]	100[6]	I/O	**P1[17] —** General purpose input/output digital pin (GPIO).
P1[25]/EXTIN0	16[6]	I/O	**P1[25] —** General purpose input/output digital pin (GPIO).
		I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	12[6]	I/O	**P1[26] —** General purpose input/output digital pin (GPIO).
		I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	90[6]	I/O	**P1[27] —** General purpose input/output digital pin (GPIO).
		O	**TDO —** Test Data out for JTAG interface.
P1[28]/TDI	86[6]	I/O	**P1[28] —** General purpose input/output digital pin (GPIO).
		I	**TDI —** Test Data in for JTAG interface.
P1[29]/TCK	82[6]	I/O	**P1[29] —** General purpose input/output digital pin (GPIO).
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	78[6]	I/O	**P1[30] —** General purpose input/output digital pin (GPIO).
		I	**TMS —** Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	8[6]	I/O	**P1[31] —** General purpose input/output digital pin (GPIO).
		I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2157/2158 incorporate a 512 kB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip bootloader, flash memory available for user's code on LPC2157/2158 is 500 kB respectively.

The LPC2157/2158 flash memory provides a minimum of 400000 erase/write cycles and 20 years of data-retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2157/2158 provide 32 kB and 40 kB of static RAM.

- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit ADC

The LPC2157/2158 contain two single 10-bit successive approximation ADCs. While ADC0 has eight channels (six channels for LPC2158), ADC1 has eight channels. Therefore, the total number of available ADC inputs for LPC2157 is 16 and for LPC2158 is 14.

6.8.1 Features

- 10-bit successive approximation ADC.
- Measurement range of 0 V to VREF (2.0 V ≤ VREF ≤ V_{DDA}).
- Each converter capable of performing more than 400000 10-bit samples per second.
- Every analog input has a dedicated result register to reduce interrupt overhead.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or timer match signal.
- Global Start command for both converters.

6.9 10-bit DAC

The DAC enables the LPC2157/2158 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

6.9.1 Features

- 10-bit DAC.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

6.10 USB 2.0 device controller (LPC2158 only)

The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.19 System control

6.19.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8 or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2157/2158: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.19.4 Brownout detector

The LPC2157/2158 include 2-stage monitoring of the voltage on the V_{DD} pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the VIC. This signal can be enabled for interrupt; if not, software can monitor the signal by reading dedicated register.

The second stage of low voltage detection asserts reset to inactivate the LPC2157/2158 when the voltage on the V_{DD} pins falls below 2.6 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset.

Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

6.19.5 Code security

This feature of the LPC2157/2158 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip bootloader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

6.19.6 External interrupt inputs

The LPC2157/2158 include up to nine edge or level sensitive external interrupt inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The external interrupt inputs can optionally be used to wake-up the processor from Power-down mode.

Additionally capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

6.19.7 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.19.8 Power control

The LPC2157/2158 supports two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings during active and Idle mode.

6.19.9 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.20 Emulation and debugging

The LPC2157/2158 supports emulation and debugging via a JTAG serial port. Debugging functions are multiplexed with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.20.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communications Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

6.21.4 Oscillator

6.21.4.1 Internal clock

An internal oscillator provides the clock signals for the internal logic of the LCD controller and its LCD drive signals. After power-up, pin SDA must be HIGH to guarantee that the clock starts.

6.21.5 Timing

The LCD controller timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock.

Frame frequency = $f_{osc(ctrl)LCD}/24$.

6.21.6 Display register

A display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs, and each column of the display RAM.

6.21.7 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31. The segment output signals are generated according to the multiplexed backplane signals and the display latch data. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

6.21.8 Backplane outputs

The LCD drive section has four backplane outputs BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit. In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.21.9 Display RAM

The display RAM is a static 32 $\times$ 4-bit RAM which stores LCD data. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 32 segments for backplane 0 (BP0). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

6.21.10 Data pointer

The Display RAM is addressed using the data pointer. Either a single byte or a series of display bytes may be loaded into any location of the display RAM.

6.21.11 Output bank selector

The LCD controller includes a RAM bank switching feature in the static and 1:2 drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This allows display information to be prepared in an alternative bank and then selected for display when it is assembled.

6.21.12 Input bank selector

The input bank selector loads display data into the display RAM based on the selected LCD drive configuration. The BANK SELECT command can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1:2 mode. The input bank selector functions are independent of the output bank selector.

6.21.13 Blinker

The LCD controller has a very versatile display blinking capability. The whole display can blink at a frequency selected by the BLINK command. Each blink frequency is a multiple integer value of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected, as shown in Table 5.

An additional feature allows an arbitrary selection of LCD segments to be blinked in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the BLINK command.

The entire display can be blinked at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 5. Blinking frequencies

Blink mode	Normal operating mode ratio	Normal blink frequency
Off	-	blinking off
2 Hz	$f_{osc(ctrl)LCD}/768$	2 Hz
1 Hz	$f_{osc(ctrl)LCD}/1536$	1 Hz
0.5 Hz	$f_{osc(ctrl)LCD}/3072$	0.5 Hz

Blink modes 0.5 Hz, 1 Hz and 2 Hz, and nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency ($f_{osc(ctrl)LCD}$) of 1536 Hz at pin CLK. The oscillator frequency range is 397 Hz to 3046 Hz.

6.21.13.1 I^2C-bus controller

The LCD controller acts as an I^2C-bus slave receiver. In the LPC2157/2158 the hardware subaddress inputs A0, A1 and A2 are tied to V_{SS} setting the hardware subaddress = 0.

6.21.14 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

Table 7. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1		0	-	1.8	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2		0	-	1.8	V
USB pins						
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	-	-	±10	µA
V_{BUS}	bus supply voltage		-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		0.8	-	2.0	V
V_{OL}	LOW-level output voltage	R_L of 1.5 kΩ to 3.6 V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L of 15 kΩ to GND	2.8	-	3.6	V
C_{trans}	transceiver capacitance	pin to GND	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	steady state drive [15]	29	-	44	Ω
R_{pu}	pull-up resistance	SoftConnect = ON	1.1	-	1.9	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and external rail.

[3] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[4] Including voltage on outputs in 3-state mode.

[5] V_{DD} supply voltages must be present.

[6] 3-state outputs go into 3-state mode when V_{DD} is grounded.

[7] Please also see the errata note mentioned in errata sheet.

[8] Accounts for 100 mV voltage drop in all supply lines.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[10] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[11] Applies to P1[16] to P1[31].

[12] On pin VBAT.

[13] Optimized for low battery consumption.

[14] To V_{SS}.

[15] Includes external resistors of 18 Ω ±1 % on D+ and D−.

Table 8. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[3]	-	-	±2	LSB
E_O	offset error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[4]	-	-	±3	LSB
E_G	gain error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[5]	-	-	±0.5	%
E_T	absolute error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[7]	-	-	40	kΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

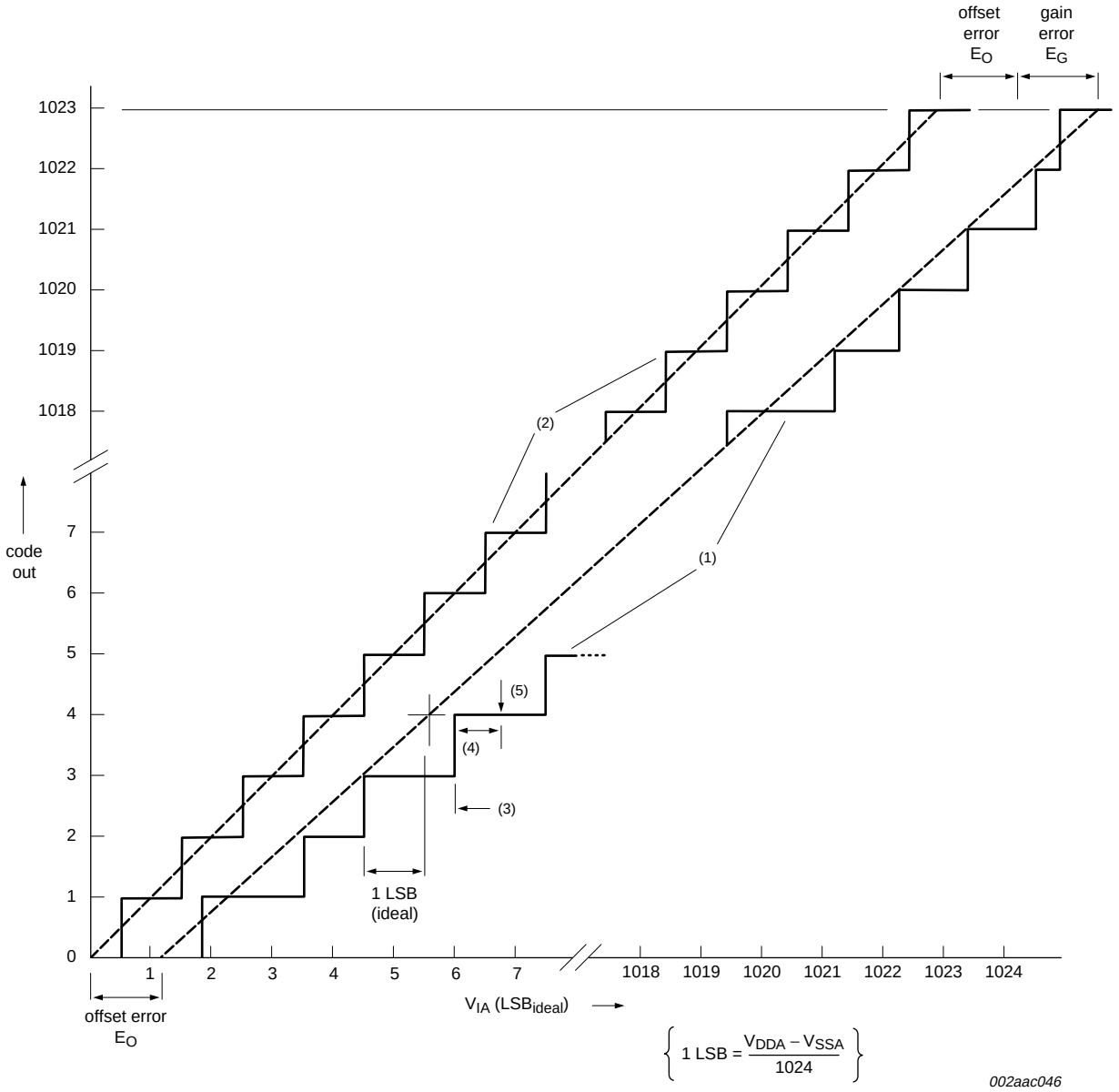
[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 7.

[7] See Figure 8.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics

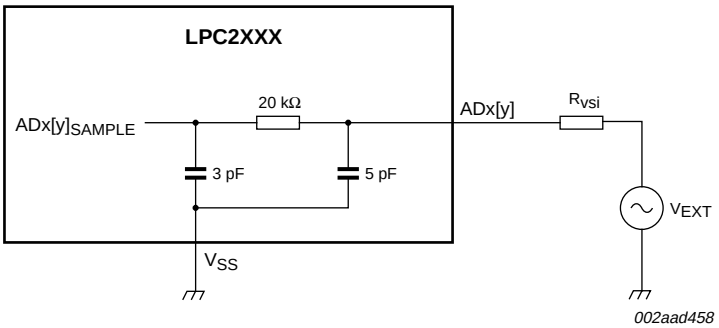


Fig 8. Suggested ADC interface - LPC2157/2158 ADx[y] pin

9. Dynamic characteristics

Table 9. Dynamic characteristics of USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	(t_r/t_f)	90	-	110	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 10	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 10	–2	-	+5	ns
t_{JR1}	receiver jitter to next transition		–18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	–9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 10	[1] 40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 10	[1] 82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 10. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (P0[2], P0[3], P0[11], and P0[14])						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0[2], P0[3], P0[11], and P0[14])						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

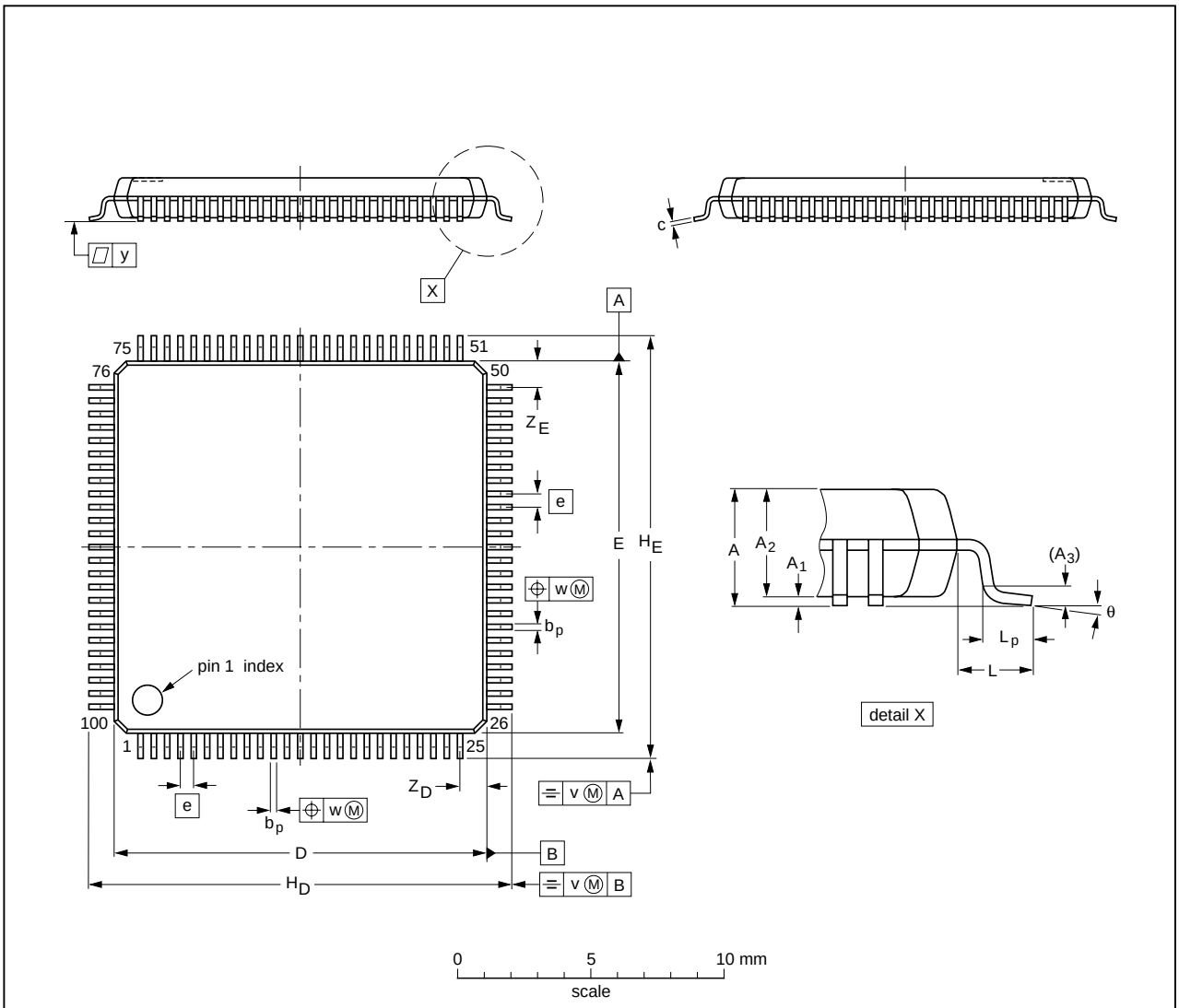
[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

11. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 13. Package outline SOT407-1 (LQFP100)

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2157_2158_2	20090209	Product data sheet	-	LPC2157_2158_1
Modifications:	• Section 2 “Features”: removed RC oscillator feature • Section 2 “Features”: added CPU operating voltage feature • Section 5.2 “Pin description”: description pin 82 P1[29]/TCK modified • Section 6.20.1 “EmbeddedICE”: added JTAG clock condition (last paragraph) • Table 7 “Static characteristics”: V_{hys}, 0.4 V moved from Typ to Min column • Table 7 “Static characteristics”: added table note [7]			
LPC2157_2158_1	20081015	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

14.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

GoodLink — is a trademark of ST-NXP Wireless.

SoftConnect — is a trademark of ST-NXP Wireless.

15. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

16. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 February 2009
Document identifier: LPC2157_2158_2