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Details

| Product Status | Active |
|----------------------------|---|
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 7x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 20-DIP (0.300", 7.62mm) |
| Supplier Device Package | 20-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f043aph020sg |

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Z8 Encore![®] F083A Series Product Specification

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Pin Description

The Z8 Encore! F083A Series products are available in variety of package styles and pin configurations. This chapter describes the signals and the pin configurations for each of the package styles. For information about the physical package specifications, see the <u>Packaging</u> chapter on page 198.

Available Packages

Table 3 lists the package styles that are available for each device in the Z8 Encore! F083A Series product line.

| Part Number | ADC | 20-pin QFN | 20-pin SOIC | 20-pin SSOP | 20-pin PDIP | 28-pin QFN | 28-pin SOIC | 28-pin SSOP |
|-------------|-----|---------------|----------------|----------------|----------------|---------------|----------------|----------------|
| Z8F083A | Yes | Х | Х | Х | Х | Х | Х | Х |
| Z8F043A | Yes | Х | Х | Х | Х | Х | Х | Х |

Table 3. Z8 Encore! F083A Series Package Options

Pin Configurations

Figures 2 through 5 display the pin configurations of all of the packages available in the Z8 Encore! F083A Series. For the description of the signals, see <u>Table 4</u> on page 11.

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.



Figure 2. Z8F083A Series in 20-Pin SOIC, SSOP, PDIP Package

| Address (He | ex) Register Description | Mnemonic | Reset (Hex) | Page # |
|--------------------|--------------------------|----------|-------------|--------|
| Interrupt Co | ntroller (cont'd.) | | | |
| FCF | Interrupt Control | IRQCTL | 00 | 68 |
| GPIO Port A | | | | |
| FD0 | Port A Address | PAADDR | 00 | 39 |
| FD1 | Port A Control | PACTL | 00 | 41 |
| FD2 | Port A Input Data | PAIN | XX | 41 |
| FD3 | Port A Output Data | PAOUT | 00 | 41 |
| GPIO Port B | | | | |
| FD4 | Port B Address | PBADDR | 00 | 39 |
| FD5 | Port B Control | PBCTL | 00 | 41 |
| FD6 | Port B Input Data | PBIN | XX | 41 |
| FD7 | Port B Output Data | PBOUT | 00 | 41 |
| GPIO Port C | | | | |
| FD8 | Port C Address | PCADDR | 00 | 39 |
| FD9 | Port C Control | PCCTL | 00 | 41 |
| FDA | Port C Input Data | PCIN | XX | 41 |
| FDB | Port C Output Data | PCOUT | 00 | 41 |
| GPIO Port D | | | | |
| FDC | Port D Address | PDADDR | 00 | 39 |
| FDD | Port D Control | PDCTL | 00 | 41 |
| FDE | Reserved | _ | XX | |
| FDF | Port D Output Data | PDOUT | 00 | 41 |
| FE0–FEF | Reserved | _ | XX | |
| Watchdog T | imer | | | |
| FF0 | Reset Status | RSTSTAT | XX | 95 |
| | WDT Control | WDTCTL | XX | 95 |
| FF1 | WDT Reload upper byte | WDTU | FF | 96 |
| FF2 | WDT Reload High Byte | WDTH | FF | 96 |
| FF3 | WDT Reload Low Byte | WDTL | FF | 97 |
| FF4–FF5 | Reserved | _ | XX | |

Table 8. Register File Address Map (Continued)

Note: XX = Undefined.

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Stop Mode Recovery Using the External RESET Pin

When the Z8 Encore! F083A Series device is in STOP Mode and the external $\overline{\text{RESET}}$ pin is driven low, a system reset occurs. Because of a glitch filter operating on the $\overline{\text{RESET}}$ pin, the low pulse must be greater than the minimum width specified about 12ns or it is ignored. The EXT bit in the Reset Status (RSTSTAT) Register is set.

Debug Pin Driven Low

Debug reset is initiated when the On-Chip Debugger detects any of the following error conditions on the DBG pin:

- Serial break (a minimum of nine continuous bits low)
- Framing error (received STOP bit is low)
- Transmit collision (OCD and host simultaneous transmission detected by the OCD)

When the Z8F083 is in STOP Mode, the debug reset will cause a system reset. The On-Chip Debugger block is not reset, but the remainder of the chip goes through a normal system reset. The POR bit in the reset (RSTSTAT) Register is set to 1.

Reset Register Definitions

The following sections define the Reset registers.

Reset Status Register

The Reset Status (RSTSTAT) Register detailed in Table 12 is a read-only register that indicates the source of the most recent Reset event, a Stop Mode Recovery event or a WDT time-out event. Reading this register resets the upper four bits to 0.

This register shares its address with the Watchdog Timer Control Register, which is writeonly.

Port A–D Alternate Function Set 2 Subregisters

The Port A–D Alternate Function Set 2 Subregister, shown in Table 28, is accessed through the Port A–D Control Register by writing 08H to the Port A–D Address Register. The Alternate Function Set 2 subregisters select the alternate function available at a port pin. Alternate functions selected by setting or clearing bits of this register are defined in the <u>Port Alternate Function Mapping</u> table on page 36.

Note: Alternate function selection on port pins must also be enabled, as described in the <u>Port A–</u> <u>D Alternate Function Subregisters</u> section on page 42.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|--------|--------|--------|--------|--------|--------|--------|
| Field | PAFS27 | PAFS26 | PAFS25 | PAFS24 | PAFS23 | PAFS22 | PAFS21 | PAFS20 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | If 08H in Port A–D Address Register, accessible through the Port A–D Control Register | | | | | | | |

Table 28. Port A–D Alternate Function Set 2 Subregisters (PxAFS2)

Bit Description

[7:0] Port Alternate Function Set 2

PAFS2x 0 = Port alternate function selected, as defined in <u>Table 16</u> on page 36.
 1 = Port alternate function selected, as defined in <u>Table 16</u> on page 36.

Note: x indicates the specific GPIO port pin number (7–0).

- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. Clear the timer PWM High and Low Byte registers to 0000H. This allows user software to determine if interrupts are generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt were generated by a reload.
- 5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and reload events. The user must configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL1 Register.
- 6. Configure the associated GPIO port pin for the timer input alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time between the timer start and the capture event is calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

COMPARE Mode

In COMPARE Mode, the timer counts up to the 16-bit maximum compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the compare value, the timer generates an interrupt and counting continues (the timer value is not reset to 0001H). Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) upon compare.

If the timer reaches FFFFH, the timer resets to 0000H and continues counting.

Observe the following steps to configure a timer for COMPARE Mode and to initiate the count.

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for COMPARE Mode
 - Set the prescale value
 - Set the initial logic level (High or Low) for the timer output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the compare value.

Timer 0–1 Control Registers

The Timer Control registers are 8-bit read/write registers that control the operation of their associated counter/timers.

Time 0–1 Control Register 0

The Timer Control Register 0 (TxCTL0) and the Timer Control Register 1 (TxCTL1) determine the timer operating mode. It also includes a programmable PWM deadband delay, two bits to configure timer interrupt definition and a status bit to identify, if the most recent timer interrupt is caused by an input capture event.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------------|----------|-----|----------|------|-----|-----|--------|
| Field | TMODEHI | TICONFIG | | Reserved | PWMD | | | INPCAP |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F06H, F0EH | | | | | | | |

| Table 56 | . Timer 0–1 | Control | Register | 0 (TxCTLC |)) |
|----------|-------------|---------|----------|-----------|----|
|----------|-------------|---------|----------|-----------|----|

| Bit | Description |
|-------------------|--|
| [7] TMODEHI | Timer Mode High Bit This bit, along with the TMODE field in the TxCTL1 Register, determines the operating mode of the timer; it is the most significant bit of the timer mode selection value. For more details, see <u>Timer 0–1 Control Register 1</u> on page 88. |
| [6:5] TICONFIG | Timer Interrupt ConfigurationThis field configures timer interrupt definition. $0x = Timer$ interrupt occurs on all of the defined reload, compare and input events. $10 = Timer$ interrupt occurs only on defined input Capture/Deassertion events. $11 = Timer$ interrupt occurs only on defined Reload/Compare events. |
| [4] | Reserved This bit is reserved and must be programmed to 0. |
| [3:1] PWMD | PWM Delay Value This field is a programmable delay to control the number of system clock cycles delay before the timer output and the timer output complement are forced to their active state. 000 = No delay. 001 = 2-cycle delay. 010 = 4-cycle delay. 011 = 8-cycle delay. 100 = 16-cycle delay. 101 = 32-cycle delay. 110 = 64-cycle delay. 111 = 128-cycle delay. |



Figure 11. Analog-to-Digital Converter Block Diagram

Operation

The ADC converts the analog input, ANA_X , to a 10-bit digital representation. The equation for calculating the digital value is represented by:

ADCOutput = $1024 \times (ANA_x \div V_{REF})$

Assuming zero gain and offset errors, any voltage outside the ADC input limits of AV_{SS} and V_{REF} returns all 0s or 1s, respectively. A new conversion is initiated by a software to the ADC Control Register's start bit.

Initiating a new conversion stops any conversion currently in progress and begins a new conversion. To avoid disrupting a conversion already in progress, the START bit is read to determine ADC operation status (i.e., busy or available).

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Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

Trim Bit Address Register

The Trim Bit Address Register, shown in Table 79, contains the target address to access the trim option bits. Trim bit addresses in the range (00H-1FH) map to the information area addresses (20H to 3FH) listed in Table 80.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|---------------------------------------|-----|-----|-----|-----|-----|-----|
| Field | | TRMADR: Trim Bit Address (00H to 1FH) | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF6H | | | | | | | |

Table 79. Trim Bit Address Register (TRMADR)

Table 80. Trim Bit Address Map

| Trim Bit Address | Information Area Address |
|---------------------|-----------------------------|
| 00H | 20H |
| 01H | 21H |
| 02H | 22H |
| 03H | 23H |
| : | : |
| 1FH | 3FH |

Trim Bit Data Register

The Trim Bit Data Register, shown in Table 81, contains the read or write data to access the trim option bits.

Byte Write

To write a byte to the NVDS array, the user code must first push the address, then the data byte onto the stack. The user code issues a CALL instruction to the address of the Byte Write routine ($0 \times 20B3$). At the return from the sub-routine, the write status byte resides in working register R0. The bit fields of this status byte are defined in Table 92. Additionally, user code should pop the address and data bytes off the stack.

The write routine uses 16 bytes of stack space in addition to the two bytes of address and data pushed by the user code. Sufficient memory must be available for this stack usage.

Because of the flash memory architecture, NVDS writes exhibit a nonuniform execution time. In general, a write takes 136 μ s (assuming a 20MHz system clock). For every 200 writes, however, a maintenance operation is necessary. In this rare occurrence, the write takes up to 58 ms to complete. Slower system clock speeds result in proportionally higher execution times.

NVDS byte writes to invalid addresses (those exceeding the NVDS array size) have no effect. Illegal write operations have a 7μ s execution time.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|---------------|---|----------|----|--------|----|---|---|
| Field | | | Reserved | FE | IGADDR | WE | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | D 1 41 | | | | | | | |

Table 92. Write Status Byte

| BIt | Description |
|---------------|--|
| [7:3] | Reserved These bits are reserved and must be programmed to 00000. |
| [2] FE | Flash Error If a Flash error is detected, this bit is set to 1. |
| [1] IGADDR | Illegal Address When NVDS byte writes to invalid addresses occur (those exceeding the NVDS array size), this bit is set to 1. |
| [0] WE | Write Error A failure occurs during writing data into Flash. When writing data into a certain address, a read back operation is performed. If the read back value is not the same as the value written, this bit is set to 1. |

On-Chip Debugger

Z8 Encore! devices contain an integrated On-Chip Debugger (OCD) that provides the following advanced debugging features:

- Reading and writing of the Register File
- Reading and writing of program and data memory
- Setting of breakpoints and watchpoints
- Executing eZ8 CPU instructions

Architecture

The On-Chip Debugger consists of four primary functional blocks: transmitter, receiver, autobaud detector/generator and debug controller. Figure 17 displays the architecture of the On-Chip Debugger.



Figure 17. On-Chip Debugger Block Diagram

eZ8 CPU Instruction Classes

eZ8 CPU instructions are divided functionally into the following groups:

- Arithmetic
- Bit manipulation
- Block transfer
- CPU control
- Load
- Logical
- Program control
- Rotate and shift

Tables 106 through 113 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instruction are considered as a subset of more than one category. Within these tables, the source operand is identified as 'src', the destination operand is 'dst' and a condition code is 'cc'.

| Mnemonic | Operands | Instruction |
|----------|----------|--|
| ADC | dst, src | Add with Carry |
| ADCX | dst, src | Add with Carry using extended addressing |
| ADD | dst, src | Add |
| ADDX | dst, src | Add using extended addressing |
| СР | dst, src | Compare |
| CPC | dst, src | Compare with Carry |
| CPCX | dst, src | Compare with Carry using extended addressing |
| СРХ | dst, src | Compare using extended addressing |
| DA | dst | Decimal Adjust |
| DEC | dst | Decrement |
| DECW | dst | Decrement Word |
| INC | dst | Increment |
| INCW | dst | Increment Word |

Table 106. Arithmetic Instructions

| Mnemonic | Operands | Instruction |
|----------|----------|--|
| AND | dst, src | Logical AND |
| ANDX | dst, src | Logical AND using extended addressing |
| СОМ | dst | Complement |
| OR | dst, src | Logical OR |
| ORX | dst, src | Logical OR using extended addressing |
| XOR | dst, src | Logical Exclusive OR |
| XORX | dst, src | Logical Exclusive OR using extended addressing |

Table 112. Program Control Instructions

| Mnemonic | Operands | Instruction |
|----------|-----------------|-------------------------------|
| BRK | _ | On-Chip Debugger Break |
| BTJ | p, bit, src, DA | Bit Test and Jump |
| BTJNZ | bit, src, DA | Bit Test and Jump if Non-Zero |
| BTJZ | bit, src, DA | Bit Test and Jump if Zero |
| CALL | dst | Call Procedure |
| DJNZ | dst, src, RA | Decrement and Jump Non-Zero |
| IRET | — | Interrupt Return |
| JP | dst | Jump |
| JP cc | dst | Jump Conditional |
| JR | DA | Jump Relative |
| JR cc | DA | Jump Relative Conditional |
| RET | — | Return |
| TRAP | vector | Software Trap |

| Assombly | | Address Mode Op Code(s) | | | | Flags | | | | Fotob | Instr | |
|-----------------|-------------------------------------|-------------------------------|-------|-------|---|-------|---|---|---|-------|--------|--------|
| Mnemonic | Symbolic Operation | dst | src | (Hex) | С | Ζ | S | ۷ | D | н | Cycles | Cycles |
| LDX dst, src | dst ← src | r | ER | 84 | - | _ | _ | _ | _ | _ | 3 | 2 |
| | | lr | ER | 85 | _ | | | | | | 3 | 3 |
| | | R | IRR | 86 | _ | | | | | | 3 | 4 |
| | | IR | IRR | 87 | _ | | | | | | 3 | 5 |
| | | r | X(rr) | 88 | _ | | | | | | 3 | 4 |
| | | X(rr) | r | 89 | _ | | | | | | 3 | 4 |
| | | ER | r | 94 | _ | | | | | | 3 | 2 |
| | | ER | lr | 95 | _ | | | | | | 3 | 3 |
| | | IRR | R | 96 | _ | | | | | | 3 | 4 |
| | | IRR | IR | 97 | _ | | | | | | 3 | 5 |
| | | ER | ER | E8 | _ | | | | | | 4 | 2 |
| | | ER | IM | E9 | _ | | | | | | 4 | 2 |
| LEA dst, X(src) | $dst \gets src + X$ | r | X(r) | 98 | _ | _ | _ | _ | _ | _ | 3 | 3 |
| | | rr | X(rr) | 99 | | | | | | | 3 | 5 |
| MULT dst | dst[15:0] ← dst[15:8] * dst[7:0] | RR | | F4 | _ | _ | _ | - | _ | _ | 2 | 8 |
| NOP | No operation | | | 0F | _ | _ | _ | _ | - | _ | 1 | 2 |
| OR dst, src | dst ← dst OR src | r | r | 42 | - | * | * | 0 | - | _ | 2 | 3 |
| | | r | lr | 43 | | | | | | | 2 | 4 |
| | | R | R | 44 | | | | | | | 3 | 3 |
| | | R | IR | 45 | _ | | | | | | 3 | 4 |
| | | R | IM | 46 | - | | | | | | 3 | 3 |
| | | IR | IM | 47 | _ | | | | | | 3 | 4 |

Table 114. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation: * = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 =Set to 1.

On-Chip Debugger Timing

Figure 32 and Table 127 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4ns maximum rise and fall time.



| Figure 32. | On-Chip | Debugger | Timing |
|------------|----------------|----------|--------|
|------------|----------------|----------|--------|

| Table | 127. | On-Chip | Debugger | Timing |
|-------|------|----------------|----------|--------|
|-------|------|----------------|----------|--------|

| | | Delay (ns) | | | | |
|----------------|--|------------|---------|--|--|--|
| Parameter | Abbreviation | Minimum | Maximum | | | |
| DBG | | | | | | |
| T ₁ | X _{IN} Rise to DBG Valid Delay | - | 15 | | | |
| T ₂ | X _{IN} Rise to DBG Output Hold Time | 2 | - | | | |
| T ₃ | DBG to XIN Rise Input Setup Time | 5 | - | | | |
| T ₄ | DBG to XIN Rise Input Hold Time | 5 | - | | | |

Appendix A. Register Tables

For the reader's convenience, this appendix lists all F083A Series registers numerically by hexadecimal address.

General Purpose RAM

In the F083A Series, the 000-EFF hexadecimal address range is partitioned for generalpurpose random access memory, as follows.

Hex Addresses: 000–0FF

This address range is reserved for general-purpose register file RAM. For more details, see the <u>Register File</u> section on page 14.

Hex Addresses: 100-EFF

This address range is reserved.

Timer 0

For more information about these Timer Control registers, see the <u>Timer Control Register</u> <u>Definitions</u> section on page 83.

Hex Address: F00

| Table 131 | . Timer | 0 High | Byte | Register | (T0H) |
|-----------|---------|--------|------|----------|-------|
|-----------|---------|--------|------|----------|-------|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---------|-----|------|-----|-----|-----|-----|-----|-----|--|--|
| Field | | TH | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Address | | F00H | | | | | | | | |

Hex Address: F09

Table 140. Timer 1 Low Byte Register (T1L)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---------|-----|------|-----|-----|-----|-----|-----|-----|--|--|
| Field | | TL | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Address | | F09H | | | | | | | | |

Hex Address: F0A

Table 141. Timer 1 Reload High Byte Register (T1RH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---------|------|-----|-----|-----|-----|-----|-----|-----|--|--|
| Field | | TRH | | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Address | F0AH | | | | | | | | | |

Hex Address: F0B

Table 142. Timer 1 Reload Low Byte Register (T1RL)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---------|-----|------|-----|-----|-----|-----|-----|-----|--|--|
| Field | | | | TF | RL | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Address | | F0BH | | | | | | | | |

Hex Address: F0C

Table 143. Timer 1 PWM High Byte Register (T1PWMH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|------|------|-----|-----|-----|-----|-----|-----|--|
| Field | | PWMH | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Address | F0CH | | | | | | | | |

Hex Addresses: FC9–FCC

This address range is reserved.

Hex Address: FCD

Table 168. Interrupt Edge Select Register (IRQES)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Field | IES7 | IES6 | IES5 | IES4 | IES3 | IES2 | IES1 | IES0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FCDH | | | | | | | |

Hex Address: FCE

Table 169. Shared Interrupt Select Register (IRQSS)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|----------|-------|-----|----------|-----|-----|-----|-----|--|
| Field | Reserved | PA6CS | | Reserved | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Address | FCEH | | | | | | | | |

Hex Address: FCF

Table 170. Interrupt Control Register (IRQCTL)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|------|---|----------|---|---|---|---|---|--|
| Field | IRQE | | Reserved | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R/W | R/W | R | R | R | R | R | R | R | |
| Address | FCFH | | | | | | | | |

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