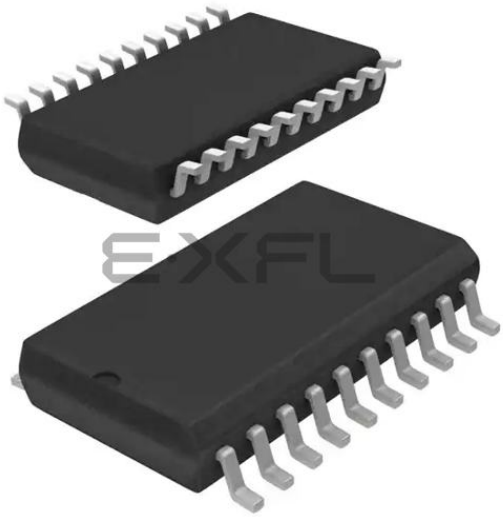


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f043ash020eg

List of Figures

Figure 1. Z8 Encore! F083A Series Block Diagram 3
Figure 2. Z8F083A Series in 20-Pin SOIC, SSOP, PDIP Package 7
Figure 3. Z8F083A Series in 28-Pin SOIC and SSOP Packages 8
Figure 4. Z8F083A Series in 20-Pin QFN Package 9
Figure 5. Z8F083A Series in 28-Pin QFN Package 10
Figure 6. Power-On Reset Operation 24
Figure 7. Voltage Brown-Out Reset Operation 25
Figure 8. GPIO Port Pin Block Diagram 34
Figure 9. Interrupt Controller Block Diagram 56
Figure 10. Timer Block Diagram 70
Figure 11. Analog-to-Digital Converter Block Diagram 99
Figure 12. ADC Timing Diagram 100
Figure 13. ADC Convert Timing 100
Figure 14. 4K Flash with NVDS 111
Figure 15. 8K Flash with NVDS 112
Figure 16. Flash Controller Operation Flow Chart 114
Figure 17. On-Chip Debugger Block Diagram 139
Figure 18. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, # 1 of 2 140
Figure 19. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #2 of 2 141
Figure 20. OCD Data Format 142
Figure 21. Oscillator Control Clock Switching Flow Chart 156
Figure 22. Recommended 20 MHz Crystal Oscillator Configuration 158
Figure 23. Connecting the On-Chip Oscillator to an External RC Network 159
Figure 24. Typical RC Oscillator Frequency as a Function of the External Capacitance with a 45K Resistor 160
Figure 25. Op Code Map Cell Description 181
Figure 26. First Op Code Map 182

Register Map

Table 8 provides an address map for the Z8 Encore! F083A Series register file. Consider registers for unimplemented peripherals to be reserved.

Table 8. Register File Address Map

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page #
General Purpose RAM				
000–0FF	General Purpose Register File RAM	—	XX	
100–EFF	Reserved	—	XX	
Timer 0				
F00	Timer 0 High Byte	T0H	00	84
F01	Timer 0 Low Byte	T0L	01	84
F02	Timer 0 Reload High Byte	T0RH	FF	85
F03	Timer 0 Reload Low Byte	T0RL	FF	85
F04	Timer 0 PWM High Byte	T0PWMH	00	86
F05	Timer 0 PWM Low Byte	T0PWML	00	86
F06	Timer 0 Control 0	T0CTL0	00	87
F07	Timer 0 Control 1	T0CTL1	00	88
Timer 1				
F08	Timer 1 High Byte	T1H	00	84
F09	Timer 1 Low Byte	T1L	01	84
F0A	Timer 1 Reload High Byte	T1RH	FF	85
F0B	Timer 1 Reload Low Byte	T1RL	FF	85
F0C	Timer 1 PWM High Byte	T1PWMH	00	86
F0D	Timer 1 PWM Low Byte	T1PWML	00	86
F0E	Timer 1 Control 0	T1CTL0	00	87
F0F	Timer 1 Control 1	T1CTL1	00	84
F10–F6F	Reserved	—	XX	
Analog-to-Digital Converter				
F70	ADC Control 0	ADCCTL0	00	102
F71	Reserved	—	XX	
F72	ADC Data High Byte	ADCD_H	XX	103
F73	ADC Data Low Bits	ADCD_L	XX	104

Note: XX = Undefined.

Bit	Description (Continued)
[6] TPOL	**Timer Input/Output Polarity** Operation of this bit is a function of the current operating mode of the timer. **ONE-SHOT Mode** When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled, the timer output signal is complemented on timer reload. **CONTINUOUS Mode** When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled and reloaded, the timer output signal is complemented. **COUNTER Mode** If the timer is disabled, the timer output signal is set to the value of this bit. If the timer is enabled the timer output signal is complemented after timer reload. 0 = Count occurs on the rising edge of the timer input signal. 1 = Count occurs on the falling edge of the timer input signal. **PWM SINGLE OUTPUT Mode** 0 = Timer output is forced low (0), when the timer is disabled. The timer output is forced high (1), when the timer is enabled and the PWM count matches and the timer output is forced low (0), when the timer is enabled and reloaded. 1 = Timer output is forced high (1), when the timer is disabled. The timer output is forced low(0), when the timer is enabled and the PWM count matches and forced high (1) when the timer is enabled and reloaded. **CAPTURE Mode** 0 = Count is captured on the rising edge of the timer input signal. 1 = Count is captured on the falling edge of the timer input signal. **COMPARE Mode** When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled and reloaded, the timer output signal is complemented. **GATED Mode** 0 = Timer counts when the timer input signal is high (1) and interrupts are generated on the falling edge of the timer input. 1 = Timer counts when the timer input signal is low (0) and interrupts are generated on the rising edge of the timer input. **CAPTURE/COMPARE Mode** 0 = Counting is started on the first rising edge of the timer input signal. The current count is captured on subsequent rising edges of the timer input signal. 1 = Counting is started on the first falling edge of the timer input signal. The current count is captured on subsequent falling edges of the timer input signal.

Sample Settling Time Register

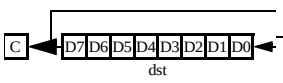
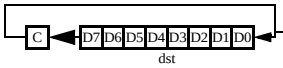
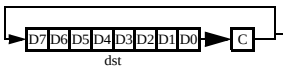
The Sample Settling Time Register, shown in Table 66, is used to program the delay after the SAMPLE/HOLD signal is asserted and before the START signal is asserted; the conversion then begins. The number of clock cycles required for settling will vary from system to system depending on the system clock period used. The system designer must program this register to contain the number of clocks required to meet a 0.5µs minimum settling time.

Table 66. Sample Settling Time (ADCSST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				SST			
RESET	0				1	1	1	1
R/W	R				R/W			
Address	F74H							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3:0] SST	0h–Fh: Sample settling time in number of system clock periods to meet 0.5µs minimum.

Table 114. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Flags Z	Flags S	Flags V	Flags D	Flags H	Fetch Cycles	Instr. Cycles
ORX dst, src	dst 8 dst OR src	ER	ER	48	–	*	*	0	–	–	4	3
		ER	IM	49							4	3
POP dst	dst 8 @SP SP 8 SP + 1	R		50	–	–	–	–	–	–	2	2
		IR		51							2	3
POPX dst	dst 8 @SP SP 8 SP + 1	ER		D8	–	–	–	–	–	–	3	2
PUSH src	SP 8 SP – 1 @SP 8 src	R		70	–	–	–	–	–	–	2	2
		IR		71							2	3
		IM		IF70							3	2
PUSHX src	SP 8 SP – 1 @SP 8 src	ER		C8	–	–	–	–	–	–	3	2
RCF	C m0			CF	0	–	–	–	–	–	1	2
RET	PC 8 @SP SP 8 SP + 2			AF	–	–	–	–	–	–	1	4
RL dst		R		90	*	*	*	*	–	–	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	–	–	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	–	–	2	2
		IR		E1							2	3
RRC dst		R		C0	*	*	*	*	–	–	2	2
		IR		C1							2	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 114. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Flags Z	Flags S	Flags V	Flags D	Flags H	Fetch Cycles	Instr. Cycles
SWAP dst	dst[7:4] < dst[3:0]	R		F0	X	*	*	X	–	–	2	2
		IR		F1							2	3
TCM dst, src	(NOT dst) AND src	r	r	62	–	*	*	0	–	–	2	3
		r	Ir	63							2	4
		R	R	64							3	3
		R	IR	65							3	4
		R	IM	66							3	3
		IR	IM	67							3	4
TCMX dst, src	(NOT dst) AND src	ER	ER	68	–	*	*	0	–	–	4	3
		ER	IM	69							4	3
TM dst, src	dst AND src	r	r	72	–	*	*	0	–	–	2	3
		r	Ir	73							2	4
		R	R	74							3	3
		R	IR	75							3	4
		R	IM	76							3	3
		IR	IM	77							3	4
TMX dst, src	dst AND src	ER	ER	78	–	*	*	0	–	–	4	3
		ER	IM	79							4	3
TRAP Vector	SP 8 SP – 2 @SP 8 PC SP 8 SP – 1 @SP 8 FLAGS PC 8 @Vector		Vector	F2	–	–	–	–	–	–	2	6
WDT				5F	–	–	–	–	–	–	1	2

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 123. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V_{DD} = 2.7V to 3.6V T_A = 0°C to +70°C			V_{DD} = 2.7V to 3.6V T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
I_{DD2}ADC	ADC Quiescent Current						1	µA	
Z_{IN}	Input Impedance				10			M	
V_{IN}	Input Voltage Range				0		2.0	V	Internal reference.
					0		0.9*V_{DD}		External reference.
T_{CONV}	Conversion Time				2.8			µs	10MHz (ADC Clock)
GBW_{IN}	Input Bandwidth					350		kHz	
T_{WAKE}	Wake Up Time					0.02		ms	Internal reference.
						10		ms	External reference.
	Input Clock Duty				45	50	55	%	
f_{ADC_CLK}	Maximum Frequency of ADC_CLK						10	MHz	

Note:
1. When the input voltage is lower than 20mV, the conversion error is out of specification tolerance.

Table 124. Comparator Electrical Characteristics

		V_{DD} = 2.7V to 3.6V T_A = 0°C to +70°C			V_{DD} = 2.7V to 3.6V T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{OS}	Input DC Offset					5		mV	
V_{CREF}	Programmable Internal Reference Voltage Range				0		1.8	V	User-programmable in 200 mV step
V_{CREF}	Programmable internal reference voltage				0.92	1.0	1.08	V	Default (CMP0[REFLVL]=5H)
T_{PROP}	Propagation delay					100		ns	
V_{HYS}	Input hysteresis					8		mV	

Hex Address: FFA

Table 197. Flash Frequency High Byte Register (FFREQH)

Bit	7	6	5	4	3	2	1	0
Field	FFREQH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FFAH							

Hex Address: FFB

Table 198. Flash Frequency Low Byte Register (FFREQL)

Bit	7	6	5	4	3	2	1	0
Field	FFREQL							
RESET	0							
R/W	R/W							
Address	FFBH							

Hex Address: FC5

Table 164. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC5H							

Hex Address: FC6

Table 165. Interrupt Request 2 Register (IRQ2)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC6H							

Hex Address: FC7

Table 166. IRQ2 Enable High Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC7H							

Hex Address: FC8

Table 167. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC8H							