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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f043asj020eg

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- 0°C to +70°C standard temperature range and –40°C to +105°C extended temperature operating ranges

Part Selection Guide

Table 1 lists the basic features available for each device within the Z8 Encore! F083A Series product line. For details, see the [Ordering Information](#) chapter on page 199.

Table 1. Z8 Encore! F083A Series Family Part Selection Guide

Part Number	Flash (KB)	RAM (B)	NVDS (100B)	ADC	I/O Pins
Z8F083A	8	256	Yes	Yes	17/23
Z8F043A	4	256	Yes	Yes	17/23

Nonvolatile Data Storage

The nonvolatile data storage (NVDS) uses a hybrid hardware/software scheme to implement a byte programmable data memory and is capable of storing about 100,000 write cycles.

Internal Precision Oscillator

The internal precision oscillator (IPO) with accuracy of $\pm 4\%$ full voltage/temperature range is a trimable clock source that requires no external components.

External Crystal Oscillator

The external crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

10-Bit Analog-to-Digital Converter

The analog-to-digital converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from eight different analog input pins. It has a fast 2.8 μ s conversion speed.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable reference voltage or with a signal at the second input pin. The comparator output is used either to drive a logic output pin or to generate an interrupt.

Timers

Two enhanced 16-bit reloadable timers are used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, CAPTURE RESTART, COMPARE, CAPTURE and COMPARE, PWM SINGLE OUTPUT and PWM DUAL OUTPUT modes.

Interrupt Controller

The Z8 Encore! F083A Series products support seventeen interrupt sources with sixteen interrupt vectors: up to five internal peripheral interrupts and up to twelve GPIO interrupts. These interrupts have three levels of programmable interrupt priority.

Low-Power Modes

The Z8 Encore! F083A Series products contain power saving features. The highest level of power reduction is provided by the STOP Mode. The next level of power reduction is provided by the HALT Mode.

Further power savings are implemented by disabling the individual peripheral blocks while in NORMAL Mode.

! Caution: The user must not enable the pull-up register bits for unused GPIO pins, because these ports output by default to V_{SS} . Unused GPIO pins include those missing on 20-pin packages and ADC-enabled 28-pin packages.

STOP Mode

Executing the eZ8 CPU's STOP instruction places the device into STOP Mode. In STOP Mode, the operating characteristics are:

- Primary crystal oscillator and internal precision oscillator are stopped; XIN and XOUT (if previously enabled) are disabled and PA0/PA1 revert to the states programmed by the GPIO registers
- System clock is stopped
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- WDT's internal RC oscillator continues to operate if enabled by the Oscillator Control Register
- If enabled, the WDT logic continues to operate
- If enabled for operation in STOP Mode by the associated Flash option bit, the VBO protection circuit continues to operate
- All other on-chip peripherals are idle

To minimize the current in STOP Mode, all GPIO pins that are configured as digital inputs must be driven to V_{DD} when the pull-up register bit is enabled or to one of power rail (V_{DD} or GND) when the pull-up register bit is disabled. The device is brought out of STOP Mode using Stop Mode Recovery. For more information about Stop Mode Recovery, see the [Reset and Stop Mode Recovery](#) chapter on page 21.

Table 16. Port Alternate Function Mapping (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port B	PB0	Reserved		AFS1[0]: 0
		ANA0	ADC analog input	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1	ADC analog input	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2	ADC analog input	AFS1[2]: 1
	PB3	CLKIN	External input clock	AFS1[3]: 0
		ANA3	ADC analog input	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		ANA7	ADC analog input	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		VREF	ADC reference voltage	AFS1[5]: 1
	PB6	Reserved		AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PB7	Reserved		AFS1[7]: 0
		Reserved		AFS1[7]: 1

Note: Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) automatically enables the associated alternate function.

Table 34. Trap and Interrupt Vectors in Order of Priority

Priority	Program Memory Vector Address	Interrupt or Trap Source
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see Watchdog Timer chapter)
	003AH	Primary oscillator fail trap (not an interrupt)
	003CH	Watchdog oscillator fail trap (not an interrupt)
	0006H	Illegal instruction trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	Reserved
	0010H	Reserved
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A7, selectable rising or falling input edge
	001AH	Port A6, selectable rising or falling input edge or Comparator Output
	001CH	Port A5, selectable rising or falling input edge
	001EH	Port A4, selectable rising or falling input edge
	0020H	Port A3, selectable rising or falling input edge
	0022H	Port A2, selectable rising or falling input edge
	0024H	Port A1, selectable rising or falling input edge
	0026H	Port A0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C3, both input edges
	0032H	Port C2, both input edges
	0034H	Port C1, both input edges
	0036H	Port C0, both input edges
Lowest	0038H	Reserved

Sample Settling Time Register

The Sample Settling Time Register, shown in Table 66, is used to program the delay after the $\overline{\text{SAMPLE/HOLD}}$ signal is asserted and before the START signal is asserted; the conversion then begins. The number of clock cycles required for settling will vary from system to system depending on the system clock period used. The system designer must program this register to contain the number of clocks required to meet a 0.5 μs minimum settling time.

Table 66. Sample Settling Time (ADCSST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				SST			
RESET	0				1	1	1	1
R/W	R				R/W			
Address	F74H							

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3:0] SST	0h–Fh: Sample settling time in number of system clock periods to meet 0.5 μs minimum.

► **Note:** The bit values used in Table 88 are set at the factory; no calibration is required.

Table 89. VBO Trim Definition

VBO_TRIM	Trigger Voltage Level
000	1.7
001	1.6
101	2.2
110	2.0
100	2.4
111	1.8

The F083A Series' on-chip Flash memory only guarantees write operations with a voltage supply over 2.7V. Write operations below 2.7V may cause unpredictable results.

Trim Bit Address 0006H

Table 90. Trim Option Bits at 0006H (TCLKFLT)

Bit	7	6	5	4	3	2	1	0
Field	DivBy4	Reserved	DlyCtl1	DlyCtl2	DlyCtl3	Reserved	FilterSel1	FilterSel0
RESET	0	1	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0026H							

Note: U = Unchanged by Reset; R/W = Read/Write.

Bit	Description
[7] DivBy4	Output Frequency Selection 0 = Output frequency is input frequency. 1 = Output frequency is 1/4 of the input frequency.
[6]	Reserved This bit is reserved and must be programmed to 1.
[5:3] DlyCtlx	Delay Control Filtered 3-bit pulse width selection. For 3.3V operation, see Table 91.

Notes: x indicates bit values 3–1; y indicates bit values 1–0.

Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a CALL instruction to the address of the byte-read routine (0x2000). At the return from the sub-routine, the read byte resides in working register R0 and the read status byte resides in working register R1. The bit fields of this status byte are defined in Table 93. Additionally, the user code should pop the address byte off the stack.

The read routine uses 16 bytes of stack space in addition to the one byte of address pushed by the user code. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS reads exhibit a nonuniform execution time. A read operation takes between 71 μ s and 258 μ s (assuming a 20MHz system clock). Slower system clock speeds result in proportionally higher execution times.

NVDS byte reads from invalid addresses (those exceeding the NVDS array size) return 0xff. Illegal read operations have a 6 μ s execution time.

The status byte returned by the NVDS read routine is zero for successful read. If the status byte is nonzero, there is a corrupted value in the NVDS array at the location being read. In this case, the value returned in R0 is the byte most recently written to the array that does not have an error.

Table 93. Read Status Byte

Bit	7	6	5	4	3	2	1	0
Field	Reserved			DE	Reserved	FE	IGADDR	Reserved
Default Value	0	0	0	0	0	0	0	0

Bit	Description
[7:5]	Reserved These bits are reserved and must be programmed to 000.
[4] DE	Data Error When reading a NVDS address, if an error is found in the latest data corresponding to this NVDS address, this bit is set to 1. NVDS source code steps forward until finding a valid data at this address.
[3]	Reserved This bit is reserved and must be programmed to 0.
[2] FE	Flash Error If a Flash error is detected, this bit is set to 1.

Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a nonstandard frequency or use the automatic factory trimmed version to achieve a 20MHz frequency with $\pm 4\%$ accuracy and 45%–55% duty cycle over the operating temperature and supply voltage of the device. Maximum startup time of IPO is 25 μ s. IPO features include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 20MHz or 119kHz (contains both a FAST and a SLOW mode)
- Trimming possible through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

Operation

The internal oscillator is an RC relaxation oscillator with minimized sensitivity to power supply variation. By using ratio tracking thresholds, the effect of power supply voltage is cancelled out. The dominant source of oscillator error is the absolute variance of chip level fabricated components, such as capacitors. An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming was performed during manufacturing and is not necessary for the user to repeat unless a frequency other than 20MHz (FAST Mode) or 119kHz (SLOW Mode) is required.

Power-down this block for minimum system power.

By default, the oscillator is configured through the Flash option bits. However, the user code overrides these trim values as described in the Trim Bit Address Space section on page 129.

Select one of two frequencies for the oscillator: 20MHz and 119kHz, using the OSCSEL bits in the Oscillator Control chapter on page 151.

eZ8 CPU Instruction Classes

eZ8 CPU instructions are divided functionally into the following groups:

- Arithmetic
- Bit manipulation
- Block transfer
- CPU control
- Load
- Logical
- Program control
- Rotate and shift

Tables 106 through 113 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instructions are considered as a subset of more than one category. Within these tables, the source operand is identified as 'src', the destination operand is 'dst' and a condition code is 'cc'.

Table 106. Arithmetic Instructions

Mnemonic	Operands	Instruction
ADC	dst, src	Add with Carry
ADCX	dst, src	Add with Carry using extended addressing
ADD	dst, src	Add
ADDX	dst, src	Add using extended addressing
CP	dst, src	Compare
CPC	dst, src	Compare with Carry
CPCX	dst, src	Compare with Carry using extended addressing
CPX	dst, src	Compare using extended addressing
DA	dst	Decimal Adjust
DEC	dst	Decrement
DECW	dst	Decrement Word
INC	dst	Increment
INCW	dst	Increment Word

Table 114. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
JR dst	$PC \leftarrow PC + X$	DA		8B	–	–	–	–	–	–	2	2
JR cc, dst	if cc is true $PC \leftarrow PC + X$	DA		0B-FB	–	–	–	–	–	–	2	2
LD dst, rc	$dst \leftarrow src$	r	IM	0C-FC	–	–	–	–	–	–	2	2
		r	X(r)	C7							3	3
		X(r)	r	D7							3	4
		r	lr	E3							2	3
		R	R	E4							3	2
		R	IR	E5							3	4
		R	IM	E6							3	2
		IR	IM	E7							3	3
		lr	r	F3							2	3
		IR	R	F5							3	3
LDC dst, src	$dst \leftarrow src$	r	lrr	C2	–	–	–	–	–	–	2	5
		lr	lrr	C5							2	9
		lrr	r	D2							2	5
LDCI dst, src	$dst \leftarrow src$ $r \leftarrow r + 1$ $rr \leftarrow rr + 1$	lr	lrr	C3	–	–	–	–	–	–	2	9
		lrr	lr	D3							2	9
LDE dst, src	$dst \leftarrow src$	r	lrr	82	–	–	–	–	–	–	2	5
		lrr	r	92							2	5
LDEI dst, src	$dst \leftarrow src$ $r \leftarrow r + 1$ $rr \leftarrow rr + 1$	lr	lrr	83	–	–	–	–	–	–	2	9
		lrr	lr	93							2	9
LDWX dst, src	$dst \leftarrow src$	ER	ER	1FE8	–	–	–	–	–	–	5	4

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Figures 26 and 27 provide operation code mapping information about each of the eZ8 CPU instructions.

		Lower Nibble (Hex)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Upper Nibble (Hex)	0	1.1 BRK	2.2 SRP	2.3 ADD	2.4 ADD	3.3 ADD	3.4 ADD	3.3 ADD	3.4 ADD	4.3 ADDX	4.3 ADDX	2.3 DJNZ	2.2 JR	2.2 LD	3.2 JP	1.2 INC	1.2 NOP	
	1	2.2 RLC	2.3 RLC	2.3 ADC	2.4 ADC	3.3 ADC	3.4 ADC	3.3 ADC	3.4 ADC	4.3 ADCX	4.3 ADCX							See 2nd Op Code Map
	2	2.2 INC	2.3 INC	2.3 SUB	2.4 SUB	3.3 SUB	3.4 SUB	3.3 SUB	3.4 SUB	4.3 SUBX	4.3 SUBX							
	3	2.2 DEC	2.3 DEC	2.3 SBC	2.4 SBC	3.3 SBC	3.4 SBC	3.3 SBC	3.4 SBC	4.3 SBCX	4.3 SBCX							
	4	2.2 DA	2.3 DA	2.3 OR	2.4 OR	3.3 OR	3.4 OR	3.3 OR	3.4 OR	4.3 ORX	4.3 ORX							
	5	2.2 POP	2.3 POP	2.3 AND	2.4 AND	3.3 AND	3.4 AND	3.3 AND	3.4 AND	4.3 ANDX	4.3 ANDX							1.2 WDT
	6	2.2 COM	2.3 COM	2.3 TCM	2.4 TCM	3.3 TCM	3.4 TCM	3.3 TCM	3.4 TCM	4.3 TCMX	4.3 TCMX							1.2 STOP
	7	2.2 PUSH	2.3 PUSH	2.3 TM	2.4 TM	3.3 TM	3.4 TM	3.3 TM	3.4 TM	4.3 TMX	4.3 TMX							1.2 HALT
	8	2.5 DECW	2.6 DECW	2.5 LDE	2.9 LDEI	3.2 LDX	3.3 LDX	3.4 LDX	3.5 LDX	3.4 LDX	3.4 LDX							1.2 DI
	9	2.2 RL	2.3 RL	2.5 LDE	2.9 LDEI	3.2 LDX	3.3 LDX	3.4 LDX	3.5 LDX	3.3 LEA	3.5 LEA							1.2 EI
	A	2.5 INCW	2.6 INCW	2.3 CP	2.4 CP	3.3 CP	3.4 CP	3.3 CP	3.4 CP	4.3 CPX	4.3 CPX							1.4 RET
	B	2.2 CLR	2.3 CLR	2.3 XOR	2.4 XOR	3.3 XOR	3.4 XOR	3.3 XOR	3.4 XOR	4.3 XORX	4.3 XORX							1.5 IRET
	C	2.2 RRC	2.3 RRC	2.5 LDC	2.9 LDCI	2.3 JP	2.9 LDC		3.4 LD	3.2 PUSHX								1.2 RCF
	D	2.2 SRA	2.3 SRA	2.5 LDC	2.9 LDCI	2.6 CALL	2.2 BSWAP	3.3 CALL	3.4 LD	3.2 POPX								1.2 SCF
	E	2.2 RR	2.3 RR	2.2 BIT	2.3 LD	3.2 LD	3.3 LD	3.2 LD	3.3 LD	4.2 LDX	4.2 LDX							1.2 CCF
	F	2.2 SWAP	2.3 SWAP	2.6 TRAP	2.3 LD	2.8 MULT	3.3 LD	3.3 BTJ	3.4 BTJ									

Figure 26. First Op Code Map

Figure 28 displays the typical current consumption while operating at 25°C and 3.3 V versus the system clock frequency in HALT Mode.

Figure 28. I_{CC} versus System Clock Frequency (HALT Mode)

Figure 29 displays the typical current consumption versus the system clock frequency in NORMAL Mode.

Figure 29. I_{CC} versus System Clock Frequency (NORMAL Mode)

Hex Addresses: F77–F7F

This address range is reserved.

Low Power Control

For more information about the Power Control Register, see the [Power Control Register Definitions](#) section on page 31.

Hex Address: F80**Table 153. Power Control Register 0 (PWRCTL0)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved			VBO	Reserved	Reserved	COMP	Reserved
RESET	1	0	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F80H							

Hex Address: F81

This address is reserved.

LED Controller

For more information about the LED Drive registers, see the [GPIO Control Register Definitions](#) section on page 39.

Hex Address: F82**Table 154. LED Drive Enable (LEDEN)**

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							

GPIO Port A

For more information about the GPIO registers, see the [GPIO Control Register Definitions](#) section on page 39.

Hex Address: FD0

Table 171. Port A GPIO Address Register (PAADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD0H							

Hex Address: FD1

Table 172. Port A Control Registers (PACTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD1H							

Hex Address: FD2

Table 173. Port A Input Data Registers (PAIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FD2H							

Hex Address: FDB**Table 182. Port C Output Data Register (PCOUT)**

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDBH							

Hex Address: FDC**Table 183. Port D GPIO Address Register (PDADDR)**

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDCH							

Hex Address: FDD**Table 184. Port D Control Registers (PDCTL)**

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDDH							

Hex Address: FDE

This address is reserved.