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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f083aqj020eg

Nonvolatile Data Storage

The nonvolatile data storage (NVDS) uses a hybrid hardware/software scheme to implement a byte programmable data memory and is capable of storing about 100,000 write cycles.

Internal Precision Oscillator

The internal precision oscillator (IPO) with accuracy of ±4% full voltage/temperature range is a trimable clock source that requires no external components.

External Crystal Oscillator

The external crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

10-Bit Analog-to-Digital Converter

The analog-to-digital converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from eight different analog input pins. It has a fast 2.8 µs conversion speed.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable reference voltage or with a signal at the second input pin. The comparator output is used either to drive a logic output pin or to generate an interrupt.

Timers

Two enhanced 16-bit reloadable timers are used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, CAPTURE RESTART, COMPARE, CAPTURE and COMPARE, PWM SINGLE OUTPUT and PWM DUAL OUTPUT modes.

Interrupt Controller

The Z8 Encore! F083A Series products support seventeen interrupt sources with sixteen interrupt vectors: up to five internal peripheral interrupts and up to twelve GPIO interrupts. These interrupts have three levels of programmable interrupt priority.

address. Following Stop Mode Recovery, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1. Table 11 lists the Stop Mode Recovery sources and resulting actions. The following sections provide more detailed information about each of the Stop Mode Recovery sources.

Table 11. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP Mode	WDT time-out when configured for Reset.	Stop Mode Recovery.
	WDT time-out when configured for interrupt.	Stop Mode Recovery followed by interrupt (if interrupts are enabled).
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source.	Stop Mode Recovery.
	Assertion of external $\overline{\text{RESET}}$ pin.	System reset.
	Debug pin driven Low.	System reset.

Stop Mode Recovery using Watchdog Timer Time-Out

If the WDT times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status (RSTSTAT) Register, the WDT and STOP bits are set to 1. If the WDT is configured to generate an interrupt upon time-out and the Z8 Encore! F083A Series device is configured to respond to interrupts, the eZ8 CPU services the WDT interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery using GPIO Port Pin Transition

Each of the GPIO port pins can be configured as a Stop Mode Recovery input source. If any GPIO pin is enabled as a Stop Mode Recovery source, a change in the input pin value (from high to low or from low to high) initiates Stop Mode Recovery. In the Reset Status (RSTSTAT) Register, the STOP bit is set to 1.

! **Caution:** In STOP Mode, the GPIO port input data registers (PxIN) are disabled. The port input data registers record the port transition only if the signal stays on the port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the port pin initiates Stop Mode Recovery without being written to the port Input Data Register or without initiating an interrupt (if enabled for that pin).

Port A–D Output Data Register

The Port A–D Output Data Register, shown in Table 30, controls the output data to the pins.

Table 30. Port A–D Output Data Register (P*x*OUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD3H, FD7H, FDBH, FDFH							

Bit	Description
[7:0] PxOUT	**Port Output Data** These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation. 0 = Drive a logical 0 (Low). 1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding port output Control Register bit to 1.

Note: x indicates the specific GPIO port pin number (7–0).

LED Drive Enable Register

The LED Drive Enable Register, shown in Table 31, activates the controlled current drive. The Alternate Function Register has no control over the LED function; therefore, setting the Alternate Function Register to select the LED function is not required. LEDEN bits [7:0] correspond to Port C bits [7:0], respectively.

Table 31. LED Drive Enable (LEDEN)

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							

Bit	Description
[7:0] LEDEN	**LED Drive Enable** These bits determine, which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin. 1 = Connect controlled current sink to the Port C pin.

LED Drive Level Low Register

The LED Drive Level Low Register, shown in Table 33, contains two control bits for each Port C pin. These two bits selects one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

Table 33. LED Drive Level Low Register (LEDLVLL)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F84H							

Bit	Description
[7:0] LEDLVLL	**LED Level Low Bits** {LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA. 01 = 7mA. 10 = 13mA. 11 = 20mA.

Caution: The frequency of the comparator output signal must not exceed one-fourth the system clock frequency.

After reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps to configure a timer for COMPARATOR COUNTER Mode and to initiate the count.

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for COMPARATOR COUNTER Mode
   - Select either the rising edge or falling edge of the comparator output signal for the count. This also sets the initial logic level (High or Low) for the timer output alternate function. However, the timer output function is not required to be enabled
2. Write to the Timer High and Low Byte registers to set the starting count value. This write only affects the first pass in COMPARATOR COUNTER Mode. After the first timer reload in COMPARATOR COUNTER Mode, counting always begins at the reset value 0001H. Generally, in COMPARATOR COUNTER Mode, the Timer High and Low Byte registers must be written with the value 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the timer output function, configure the associated GPIO port pin for the timer output alternate function.
6. Write to the Timer Control Register to enable the timer.

In COMPARATOR COUNTER Mode, the number of comparator output transitions is given by the following equation:

Comparator Output Transitions = Current Count Value – Start Value

Timer 0–1 PWM High and Low Byte Registers

The Timer 0–1 PWM High and Low Byte (TxPWMH and TxPWML) registers, shown in Tables 54 and 55, control PWM operations. These registers also store the capture values for the CAPTURE and CAPTURE/COMPARE modes.

Table 54. Timer 0–1 PWM High Byte Register (TxPWMH)

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F04H, F0CH							

Table 55. Timer 0–1 PWM Low Byte Register (TxPWML)

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H, F0DH							

Bit	Description
[7:0] PWMH, PWML	**Pulse width modulator High and Low Bytes** These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control Register (TxCTL1). The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in capture or CAPTURE/COMPARE modes.

Sample Time Register

The sample time register, shown in Table 67, is used to program the length of active time for the sample after a conversion has begun by setting the START bit in the ADC Control Register. The number of system clock cycles required for the sample time varies from system to system, depending on the clock period used. The system designer must program this register to contain the number of system clocks required to meet a 1µs minimum sample time.

Table 67. Sample Time (ADCST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		ST					
RESET	0		1	1	1	1	1	1
R/W	R/W		R/W					
Address	F75H							

Bit	Description
[7:6]	**Reserved** These bits are reserved and must be programmed to 00.
[5:0] ST	**Sample/Hold Time** Measured in number of system clock periods to meet 1µs minimum.

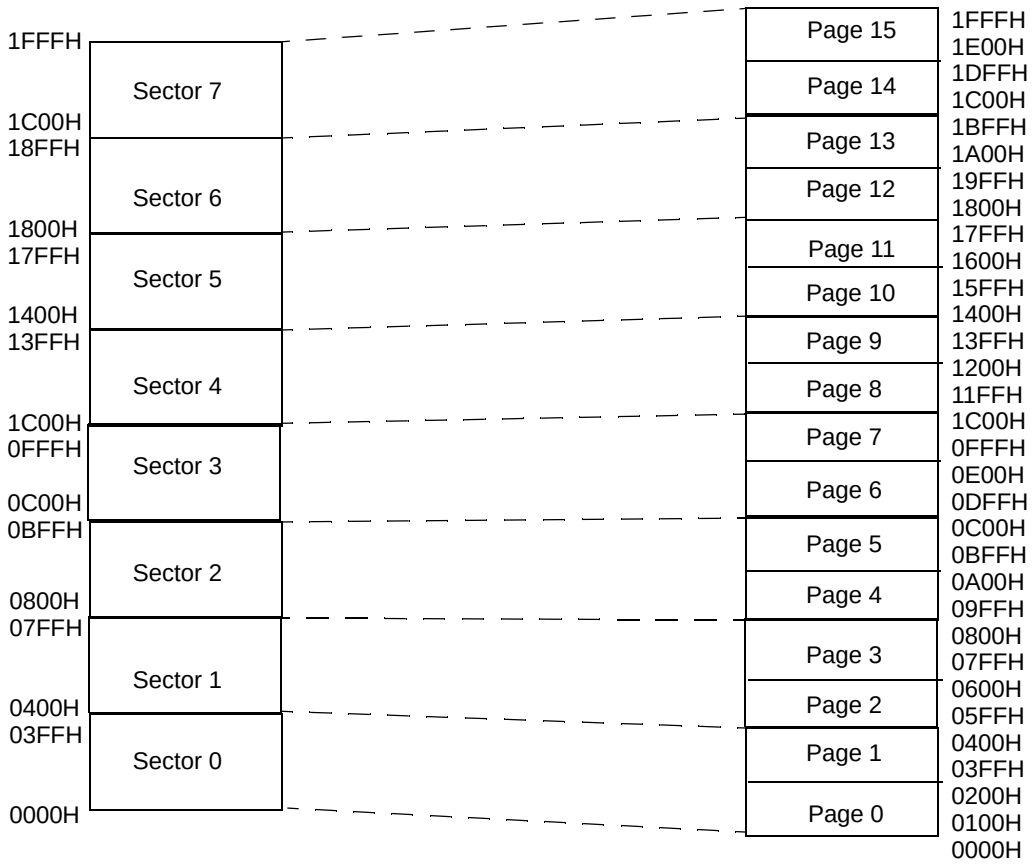

Figure 15. 8K Flash with NVDS

Data Memory Address Space

The Flash information area, including the Zilog Flash option bits, is located in the data memory address space. The Z8 Encore! F083A Series devices are configured by the Zilog Flash option bits to prevent the user from writing to the eZ8 CPU data memory address space.

Flash Information Area

The Flash information area is physically separate from program memory and is mapped to the address range FE00H to FE7FH. Not all of these addresses are user-accessible. Factory trim values for the VBO and internal precision oscillator, and factory calibration data for the ADC, are stored here.

Flash Operation Timing Using the Flash Frequency Registers

Before performing either a Program or Erase operation on Flash memory, the user must first configure the Flash frequency High and Low Byte registers. The Flash frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 10kHz to 20MHz.

The Flash frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control the timing for Flash Program and Erase operations. The 16-bit binary Flash frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

$$\text{FFREQ}[15:0] = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

Caution: Flash programming and erasure are not supported for system clock frequencies below 10kHz or above 20MHz. The Flash frequency High and Low Byte registers must be loaded with the correct value to ensure operation of the Z8 Encore! F083A Series devices.

Flash Code Protection Against External Access

The user code contained within Flash memory is protected against external access by using the On-Chip Debugger. Programming the FRP Flash option bit prevents reading of the user code using the On-Chip Debugger. For more details, see the Flash Option Bits chapter on page 124 and the On-Chip Debugger chapter on page 139.

Flash Code Protection Against Accidental Program and Erasure

Z8 Encore! F083A Series devices provide several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

Flash Code Protection using the Flash Option Bits

The FHSWP and FWP Flash option bits combine to provide three levels of Flash program memory protection as listed in Table 72. For more details, see the Flash Option Bits chapter on page 124.

Table 72. Flash Code Protection Using Flash Option Bits

FHSWP	FWP	Flash Code Protection Description
0	0	Programming and erasing disabled for all Flash program memory. In user code programming, page erase and mass erase are all disabled. Mass erase is available through the On-Chip Debugger.
0 or 1	1	Programming, page erase and mass erase are enabled for all of the Flash program memory.

At reset, the Flash Controller is locked to prevent accidental program or erasure of Flash memory. To program or erase Flash memory, first write the target page to the Page Select Register. Unlock the Flash Controller by making two consecutive writes to the Flash Control Register with the values 73H and 8CH, sequentially. The Page Select Register must be rewritten with the same page previously stored there. If the two page select writes do not match, the controller reverts to a Locked state. If the two writes match, the selected page becomes active. For details, see Figure 16 on page 114.

After unlocking a specific page, the user must enable either page program or erase. Writing the value 95H causes a page erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control Register locks the Flash Controller. Mass erase is not allowed in the user code, but is allowed through the debug port.

After unlocking a specific page, the user must also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register causes the active page to revert to a Locked state.

Sector-Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore! devices are divided into maximum number of eight sectors. A sector is one-eighth of the total size of Flash memory, unless this value is smaller than the page size, in which case the sector and page sizes are equal. On the Z8 Encore! F083A Series devices, the sector size is varied; see Table 70 and Figures 14 and 15.

The Flash Sector Protect Register can be configured to prevent sectors from being programmed or erased. After a sector is protected, it cannot be unprotected by user code. The Flash Sector Protect Register is cleared after reset and any previously written protection values is lost. User code must write this register in their initialization routine if they want to enable sector protection.

The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register is accessed by writing the Flash Control Register with 5EH. After the Flash Sector Protect Register is selected, it can be accessed at the Page Select Register address. When user code writes the Flash Sector Protect Register, bits can only be set to 1. Thus, sectors can be protected, but not unprotected, via register

- The Flash Sector Protect Register is ignored for programming and Erase operations.
- Programming operations are not limited to the page selected in the Page Select Register.
- Bits in the Flash Sector Protect Register are written to one or zero.
- The second write of the Page Select Register to unlock the flash controller is not necessary.
- The Page Select Register is written when the Flash Controller is unlocked.
- The mass erase command is enabled through the Flash Control Register

Caution: For security reasons, Flash Controller allows only a single page to be opened for write/erase. When writing multiple Flash pages, the Flash Controller must go through the unlock sequence again to select another page.

NVDS Operational Requirements

The device uses a 12KB Flash memory, despite the maximum specified Flash of 8KB size (except 12KB mode with non-NVDS). User code accesses the lower 8KB of flash, leaving the upper 4 K for Zilog memory. The NVDS is implemented by using Zilog memory for special purpose routines and for the data required by the routines. These routines are factory programmed and cannot be altered by the user. The NVDS operation is described in detail. See the Nonvolatile Data Storage chapter on page 134.

The NVDS routines are triggered by a user code: CALL into Zilog memory. Code executing from Zilog memory must be able to read and write other locations within Zilog memory. User code must not be able to read or write Zilog memory.

Flash Control Register Definitions

This section defines the features of the following Flash Control registers.

Flash Control Register: see page 120

Flash Status Register: see page 121

Flash Page Select Register: see page 121

Flash Sector Protect Register: see page 122

Flash Frequency High and Low Byte Registers: see page 123

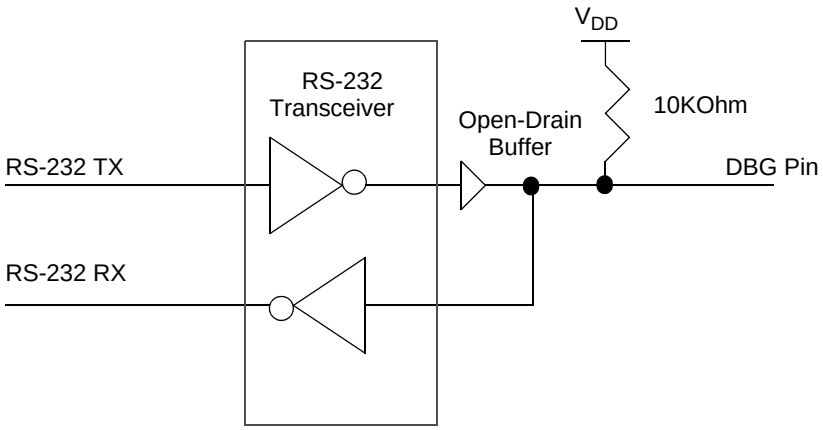

Figure 19. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #2 of 2

DEBUG Mode

F083A Series devices, when in DEBUG Mode, feature the following operating characteristics:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates, unless the device is in STOP Mode
- All enabled on-chip peripherals operate, unless the device is in STOP Mode
- Automatically exits HALT Mode
- Constantly refreshes the Watchdog Timer, if enabled

Entering DEBUG Mode

- The device enters DEBUG Mode after the eZ8 CPU executes a Breakpoint (BRK) instruction
- If the DBG pin is held Low during the most recent system reset clock cycle, the device enters DEBUG Mode upon exiting system reset

Exiting DEBUG Mode

The device exits DEBUG Mode upon any of the following operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0
- Power-On Reset
- Voltage Brown-Out reset

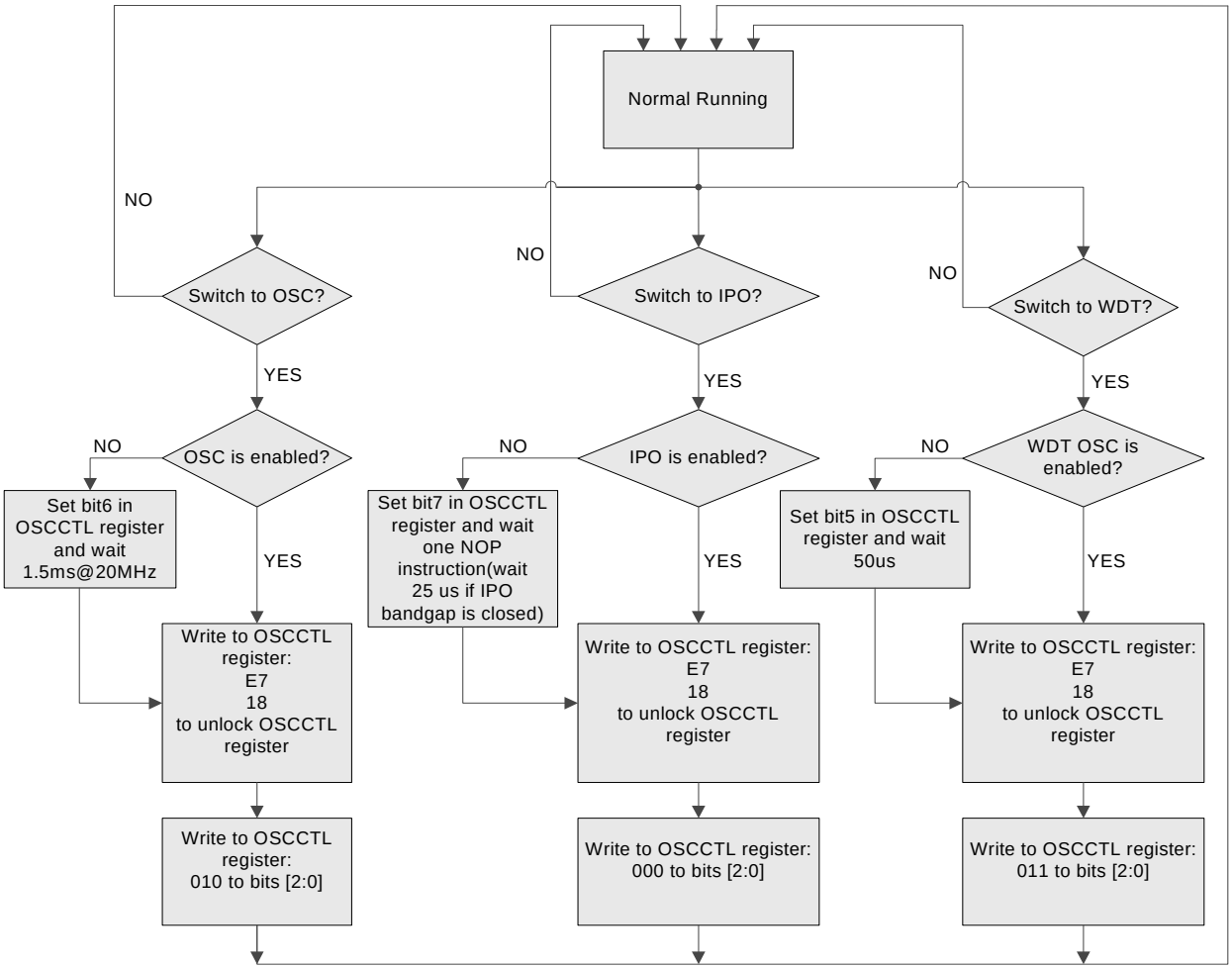

Figure 21. Oscillator Control Clock Switching Flow Chart

Table 103. Assembly Language Syntax Example 2

Assembly Language Code	ADD	43H,	R8	(ADD dst, src)
Object Code	04	E8	43	(OPC src, dst)

The Register File size varies, depending on the device type. See the device-specific Z8 Encore! product specification to determine the exact Register File range available.

eZ8 CPU Instruction Notation

In the eZ8 CPU instruction summary and description sections, the operands, condition codes, status flags and address modes are represented by a notational shorthand that is described in Table 104.

Table 104. Notational Shorthand

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
cc	Condition Code	—	See the condition codes overview in the eZ8 CPU Core User Manual (UM0128).
DA	Direct Address	Addrs	*Addrs* represents a number in the range of 0000H to FFFFH.
ER	Extended addressing Register	Reg	*Reg* represents a number in the range of 000H to FFFH.
IM	Immediate Data	#Data	Data is a number between 00H to FFH/
Ir	Indirect Working Register	@Rn	n = 0–15.
IR	Indirect Register	@Reg	*Reg* represents a number in the range of 00H to FFH/
Irr	Indirect Working Register Pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12 or 14.
IRR	Indirect Register Pair	@Reg	*Reg* represents an even number in the range 00H to FEH.
p	Polarity	p	Polarity is a single bit binary value of either 0B or 1B.
r	Working Register	Rn	n = 0–15.
R	Register	Reg	Reg. represents a number in the range of 00H to FFH.

eZ8 CPU Instruction Summary

Table 114 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags register, the number of CPU clock cycles required for the instruction fetch and the number of CPU clock cycles required for the instruction execution.

Table 114. eZ8 CPU Instruction Summary

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
ADC dst, src	dst ← dst + src + C	r	r	12	*	*	*	*	0	*	2	3
		r	Ir	13							2	4
		R	R	14							3	3
		R	IR	15							3	4
		R	IM	16							3	3
		IR	IM	17							3	4
ADCX dst, src	dst ← dst + src + C	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19							4	3
ADD dst, src	dst ← dst + src	r	r	02	*	*	*	*	0	*	2	3
		r	Ir	03							2	4
		R	R	04							3	3
		R	IR	05							3	4
		R	IM	06							3	3
		IR	IM	07							3	4
ADDX dst, src	dst ← dst + src	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09							4	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Hex Address: F09

Table 140. Timer 1 Low Byte Register (T1L)

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F09H							

Hex Address: F0A

Table 141. Timer 1 Reload High Byte Register (T1RH)

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0AH							

Hex Address: F0B

Table 142. Timer 1 Reload Low Byte Register (T1RL)

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0BH							

Hex Address: F0C

Table 143. Timer 1 PWM High Byte Register (T1PWMH)

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0CH							

Hex Address: F83

Table 155. LED Drive Level High Register (LEDLVLH)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F83H							

Hex Address: F84

Table 156. LED Drive Level Low Register (LEDLVLL)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F84H							

Hex Address: F85

This address is reserved.

Oscillator Control

For more information about the Oscillator Control registers, see the Oscillator Control Register Definitions section on page 154.

Hex Address: F86

Table 157. Oscillator Control Register (OSCCTL)

Bit	7	6	5	4	3	2	1	0
Field	INTEN	XTLEN	WDTEN	POFEN	WDFEN	SCKSEL		
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F86H							

G

H

I