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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc811m001jdh16j

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC810M021FN8	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT097-2
LPC811M001JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JD20	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC812M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC812M101JTB16	XSON16	plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 × 3.2 × 0.5 mm	SOT1341-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/kB	SRAM/kB	USART	I^2C-bus	SPI	Comparator	GPIO	Package
LPC810M021FN8	4	1	2	1	1	1	6	DIP8
LPC811M001JDH16	8	2	2	1	1	1	14	TSSOP16
LPC812M101JDH16	16	4	3	1	2	1	14	TSSOP16
LPC812M101JD20	16	4	2	1	1	1	18	SO20
LPC812M101JDH20	16	4	3	1	2	1	18	TSSOP20
LPC812M101JTB16	16	4	3	1	2	1	14	XSON16

6. Block diagram

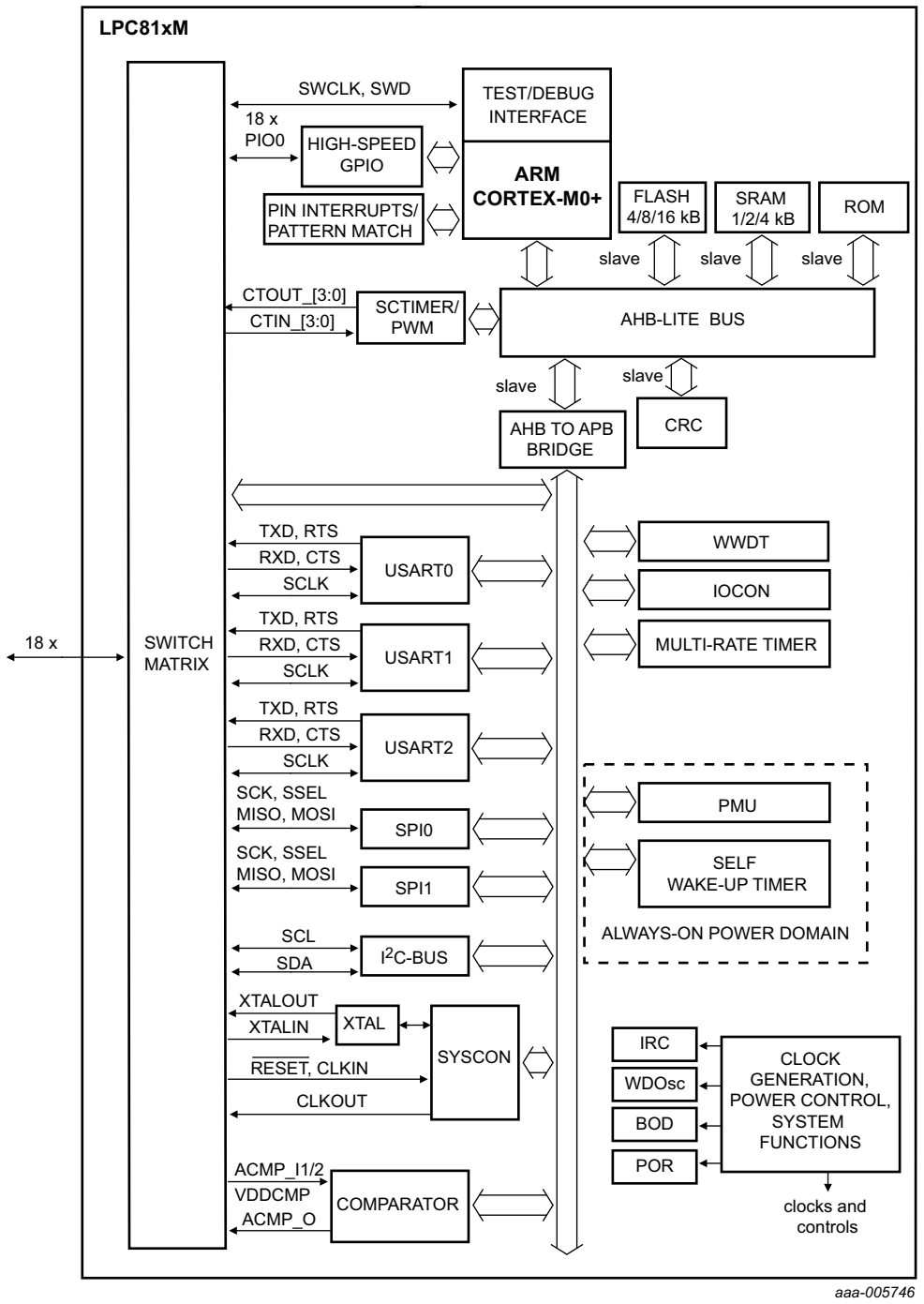


Fig 1. LPC81xM block diagram

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC81xM contain a total of up to 4 kB on-chip static RAM data memory.

8.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I^2C-bus driver API routines

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Relocatable interrupt vector table using vector table offset register.

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight pins, regardless of the selected function, can be programmed to generate an interrupt on a level, a rising or falling edge, or both. The interrupt generating pins can be selected from all digital or mixed digital/analog pins. The pin interrupt/pattern match block controls the edge or level detection mechanism.

8.6 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.7 Memory map

The LPC81xM incorporates several distinct memory regions. Figure 7 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 10 “LPC81xM clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

8.8.1 Standard I/O pad configuration

Figure 8 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

– The pattern match engine does not facilitate wake-up.

8.12 USART0/1/2

Remark: USART0 and USART1 are available on all LPC800 parts. USART2 is available on parts LPC812M101JTB16, LPC812M101JDH16, and LPC812M101JDH20 only.

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.12.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except PIO0_10 and PIO0_11.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Supported by on-chip ROM API.

8.13 SPI0/1

Remark: SPI0 is available on all LPC800 parts. SPI1 is available on parts LPC812M101JDH16 and LPC812M101JDH20 only.

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.13.1 Features

- Maximum data rates of 30 Mbit/s in master mode and 25 Mbit/s in slave mode for SPI functions connected to all digital pins except PIO0_10 and PIO0_11.

All inputs and outputs of the SCTimer/PWM are movable functions and are assigned to pins through the switch matrix.

8.15.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state, and the count direction.
- Events control outputs, interrupts, and the SCT states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - 4 inputs
  - 4 outputs
  - 5 match/capture registers
  - 6 events
  - 2 states

8.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.16.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC81xM will operate from the IRC until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 10 for an overview of the LPC81xM clock generation.

8.20.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC81xM use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.20.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.20.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is $\pm$ 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz ($\pm$ 40% accuracy) oscillator serves a the clock input to the WKT. This oscillator can be configured to run in all low power modes.

8.20.2 Clock input

An external clock source can be supplied on the selected CLKIN pin. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 9 “Static characteristics” and Table 16 “Dynamic characteristics: I/O pins[1]”.

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal ((see Section 14.2).

The maximum frequency for both clock signals is 25 MHz.

8.20.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output

8.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

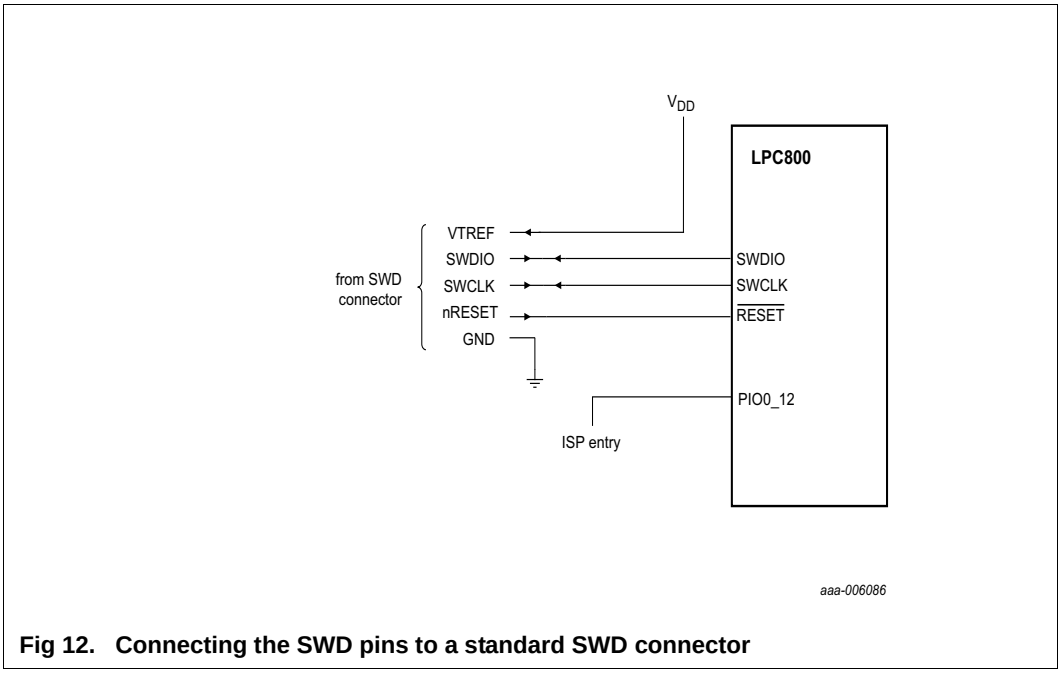


Fig 12. Connecting the SWD pins to a standard SWD connector

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Oscillator input pins (PIO0_8 and PIO0_9)							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[3] IRC enabled; system oscillator disabled; system PLL disabled.

[4] BOD disabled.

[5] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[6] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[7] IRC enabled; system oscillator disabled; system PLL enabled.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[10] WAKEUP pin pulled HIGH externally.

[11] Including voltage on outputs in tri-state mode.

[12] 3-state outputs go into tri-state mode in Deep power-down mode.

[13] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[14] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 8.

[15] To V_{SS}.

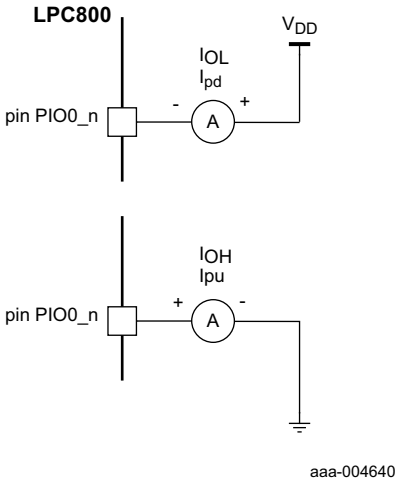


Fig 13. Pin input/output current measurement

12. Dynamic characteristics

12.1 Power-up ramp conditions

Table 11. Power-up characteristics

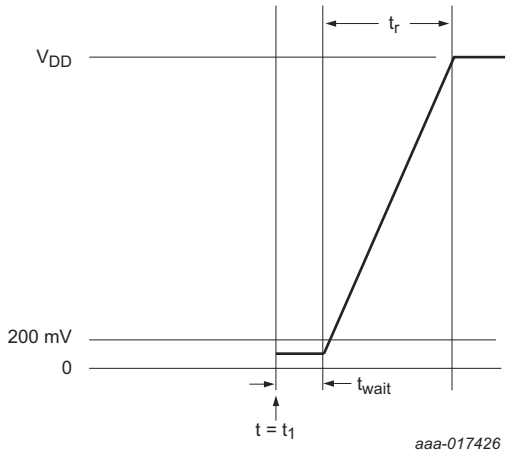
T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 200 mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2][3]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	200	mV

[1] See Figure 28.

[2] The wait time specifies the time the power supply must be at levels below 200 mV before ramping up. See the LPC81x errata sheet.

[3] Based on characterization, not tested in production.



Condition: 0 < V_I ≤ 200 mV at start of power-up (t = t_1)

Fig 28. Power-up ramp

12.2 Flash memory

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

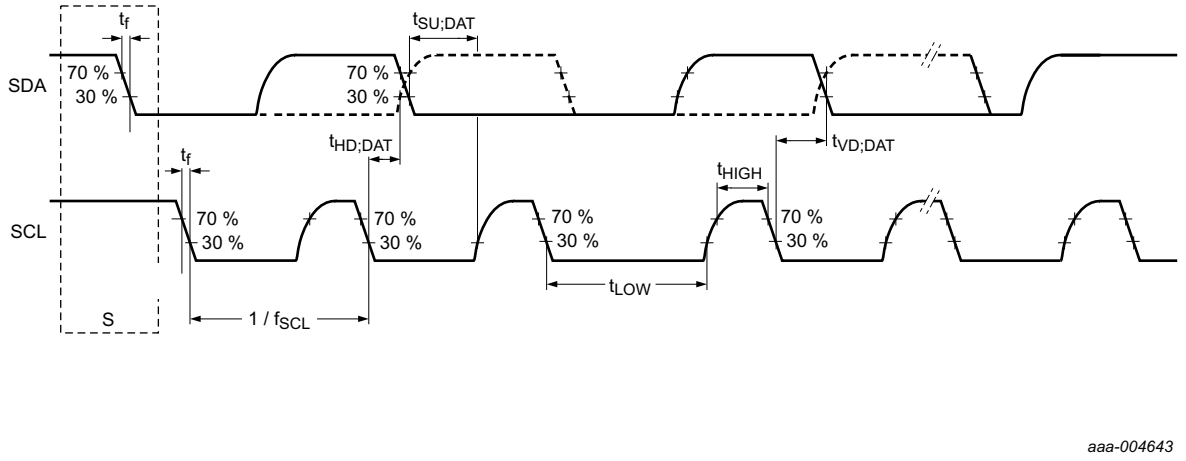


Fig 31. I^2C-bus pins clock timing

12.7 SPI interfaces

The maximum data bit rate is 30 Mbit/s in master mode and 25 Mbit/s in slave mode.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

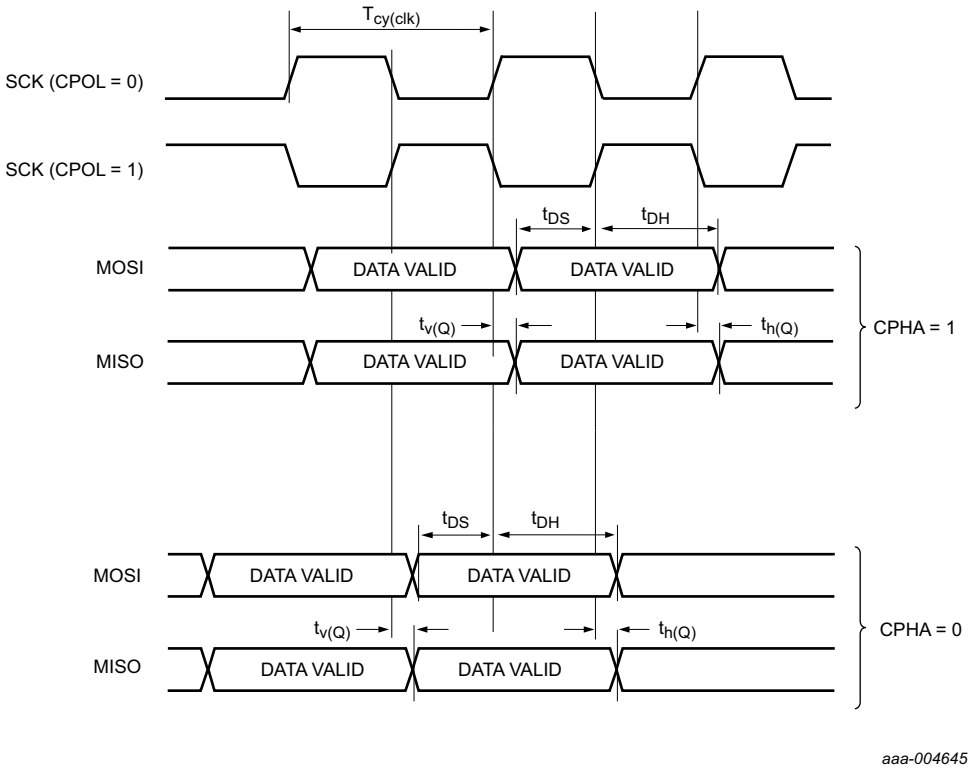
Table 18. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V. Simulated parameters sampled at the 50 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master[1]						
$T_{cy(clk)}$	clock cycle time		[2]	33	-	ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	0.5	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		0.5	-	ns
SPI slave						
$T_{cy(clk)}$				40		ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	10	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		10	-	ns

[1] Capacitance on pin SPIn_SCK C_{SCK} < 5 pF.

[2] $T_{cy(clk)}$ = DIVVAL/CCLK with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the *LPC800 User manual UM10601*.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 33. SPI slave timing

[3] Typical values are derived from nominal simulation (V_{DD} = 3.3 V; T_{amb} = 27 °C; nominal process models). Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 105 °C; slow process models).

[4] Maximum and minimum values are measured on samples from the corners of the process matrix lot.

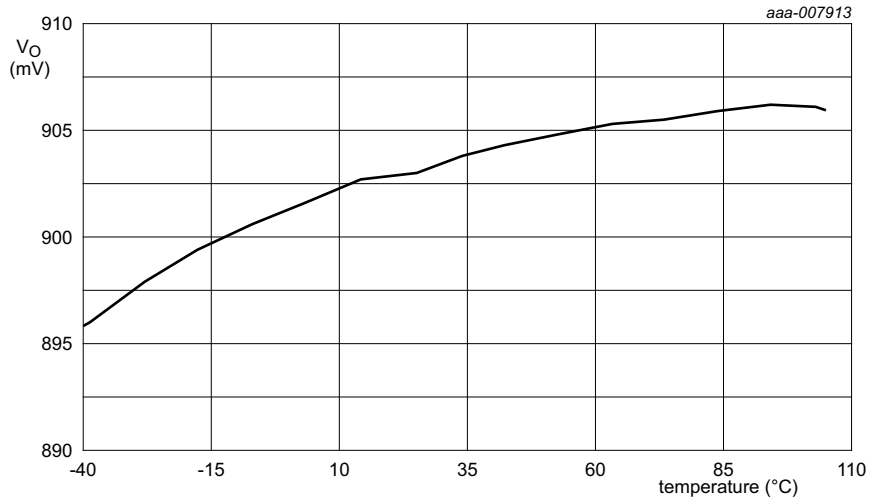


Fig 35. Typical internal voltage reference output voltage

13.3 Comparator

Table 22. Comparator characteristics

V_{DD} = 3.0 V and T_{amb} = 27 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin PIO0_6/VDDCMP configured for function VDDCMP		1.5	-	3.6	V
I_{DD}	supply current			-	55	-	µA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	1.9	-	mV
		V_{IC} = 1.5 V		-	2.1	-	mV
		V_{IC} = 2.8 V		-	2.0		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	µs

14.3 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14.4 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC812M101FDH20.

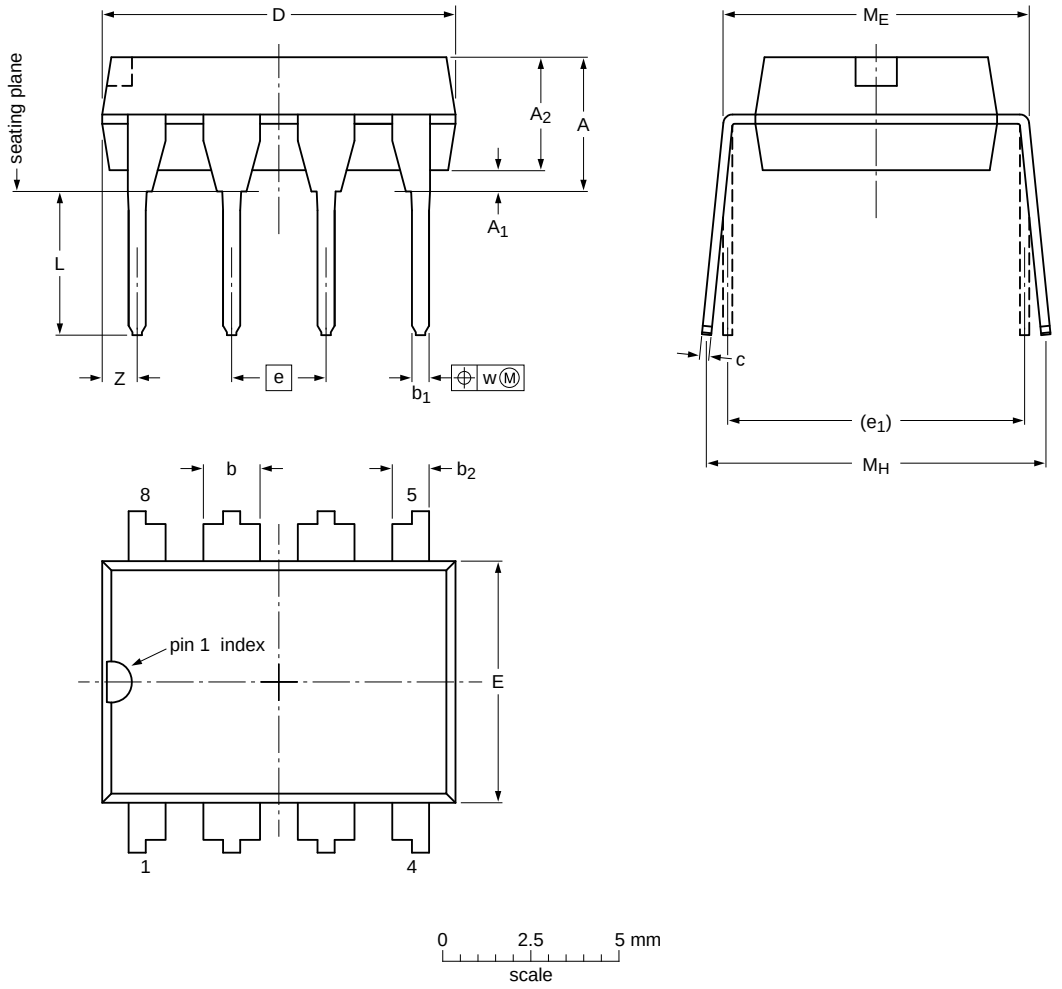
Table 28. ElectroMagnetic Compatibility (EMC) for part LPC812M101 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	30 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	1 MHz to 30 MHz	–6	–5	–5	dBμV
	30 MHz to 150 MHz	-2	-1	-2	dBμV
	150 MHz to 1 GHz	–1	-1	-1	dBμV
IEC level[1]	-	O	O	O	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	1 MHz to 30 MHz	–5	–6	–6	dBμV
	30 MHz to 150 MHz	–2	-1	-2	dBμV
	150 MHz to 1 GHz	–1	-2	-1	dBμV
IEC level[1]	-	O	O	N	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

15. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-2**



Dimensions (inch dimensions are derived from the original dimensions)

Unit[1]		A	A_1	A_2	b	b_1	b_2	c	D[1]	E[1]	e	e_1	L	M_E	M_H	w	Z[1]
mm	max	4.2		3.43	1.73	0.53	1.07	0.38	9.8	6.48			3.60	7.88	9.40		1.15
	nom										2.54	7.62				0.254	
	min		0.51		1.14	0.38	0.89	0.20	9.2	6.20			3.05	7.62	7.88		
inches	max	0.17		0.14	0.068	0.021	0.042	0.015	0.39	0.26			0.14	0.31	0.37		0.045
	nom										0.1					0.01	
	min		0.02		0.045	0.015	0.035	0.008	0.36	0.24		0.3	0.12	0.30	0.31		

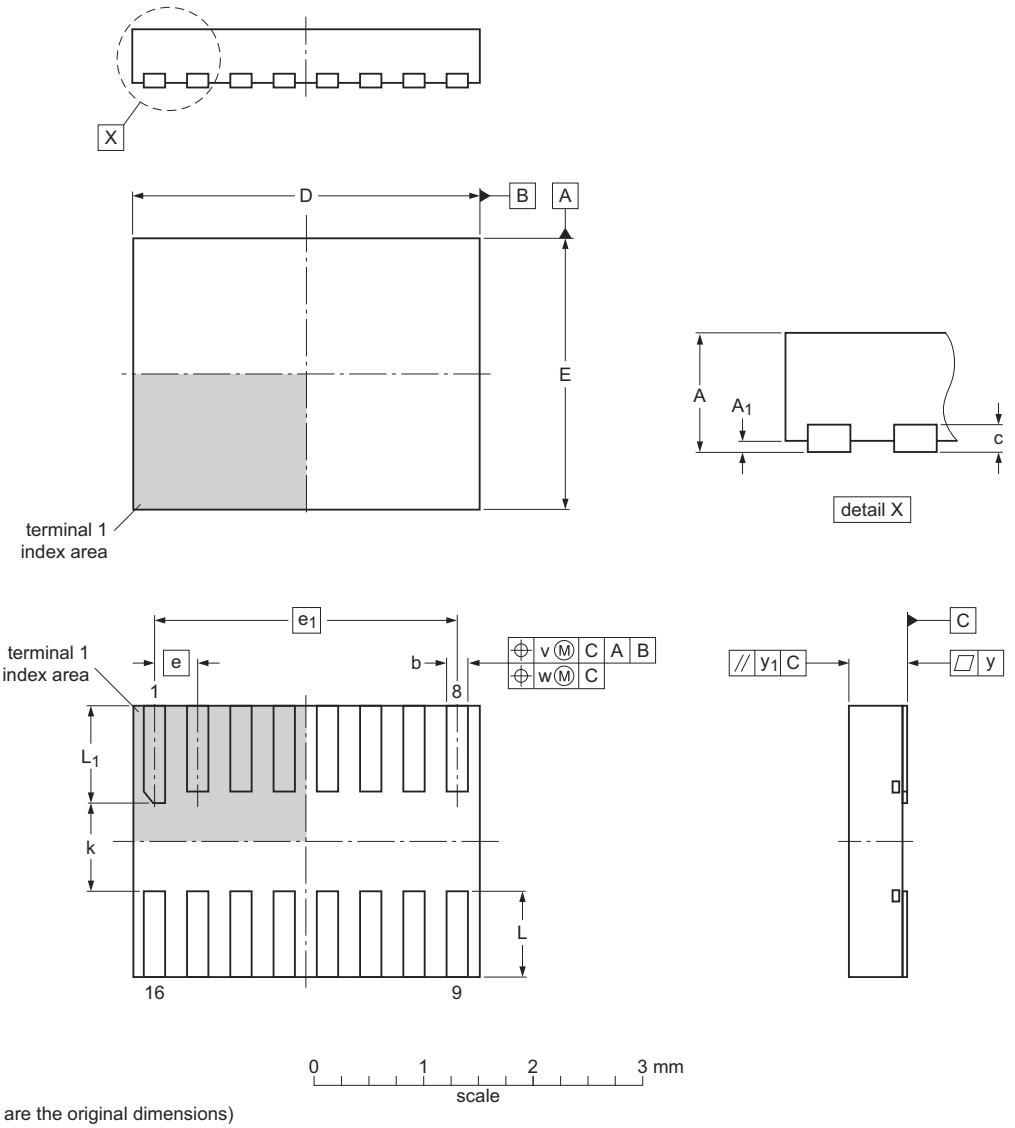
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included

sot097-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT97-2	- - -	MO-001	- - -			~~10-10-15~~ 10-10-18

Fig 38. Package outline SOT097-2 (DIP8)

XSON16: plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 x 3.2 x 0.5 mm **SOT1341-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	c	D	E	e	e_1	k	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	0.152	3.3	2.6				0.9	1.0				
	nom			0.20		3.2	2.5	0.4	2.8		0.8	0.9	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.050	3.1	2.4			0.2	0.7	0.8				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

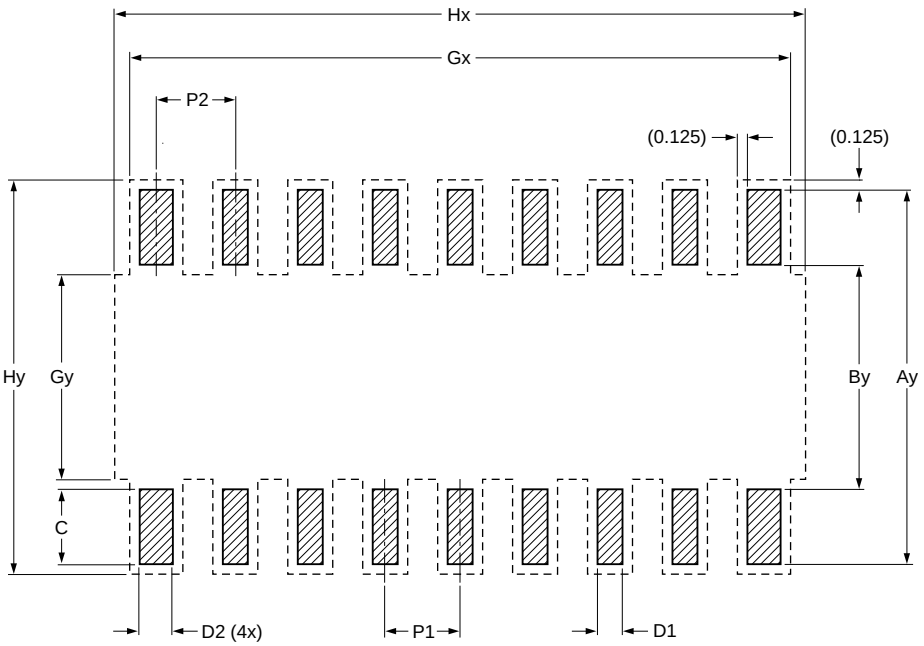
sot1341-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1341-1	- - -	MO-252	- - -			~~12-09-05~~ 13-02-13

Fig 42. Package outline SOT1341-1 (XSON16)

16. Soldering

Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 43. Reflow soldering of the TSSOP16 package