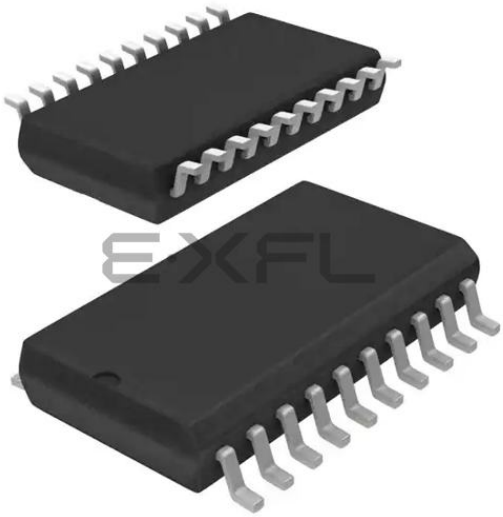

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101jd20fp

- State Configurable Timer/PWM (SCTimer/PWM) with input and output functions (including capture and match) assigned to pins through the switch matrix.
- Multiple-channel multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Self Wake-up Timer (WKT) clocked from either the IRC or a low-power, low-frequency internal oscillator.
- CRC engine.
- Windowed Watchdog timer (WWDT).

- Analog peripherals:
  - Comparator with internal and external voltage references with pin functions assigned or enabled through the switch matrix.
- Serial interfaces:
  - Three USART interfaces with pin functions assigned through the switch matrix.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - One I^2C-bus interface with pin functions assigned through the switch matrix.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1.5 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - 10 kHz low-power oscillator for the WKT.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input CLKIN, or the internal RC oscillator.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from Deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect.
- Unique device serial number for identification.
- Single power supply.
- Operating temperature range −40 °C to 105 °C except for the DIP8 package, which is available for a temperature range of −40 °C to 85 °C.
- Available as DIP8, TSSOP16, SO20, TSSOP20, and XSON16 package.

3. Applications

- 8/16-bit applications
- Consumer
- Climate control
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC810M021FN8	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT097-2
LPC811M001JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JD20	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC812M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC812M101JTB16	XSON16	plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 × 3.2 × 0.5 mm	SOT1341-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/kB	SRAM/kB	USART	I^2C-bus	SPI	Comparator	GPIO	Package
LPC810M021FN8	4	1	2	1	1	1	6	DIP8
LPC811M001JDH16	8	2	2	1	1	1	14	TSSOP16
LPC812M101JDH16	16	4	3	1	2	1	14	TSSOP16
LPC812M101JD20	16	4	2	1	1	1	18	SO20
LPC812M101JDH20	16	4	3	1	2	1	18	TSSOP20
LPC812M101JTB16	16	4	3	1	2	1	14	XSON16

7. Pinning information

7.1 Pinning

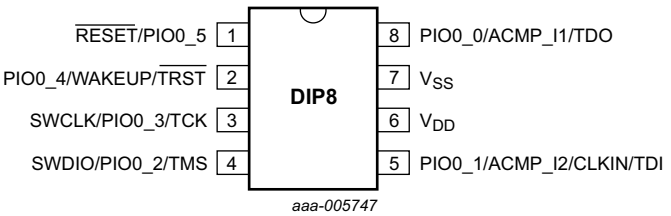


Fig 2. Pin configuration DIP8 package (LPC810M021JN8)

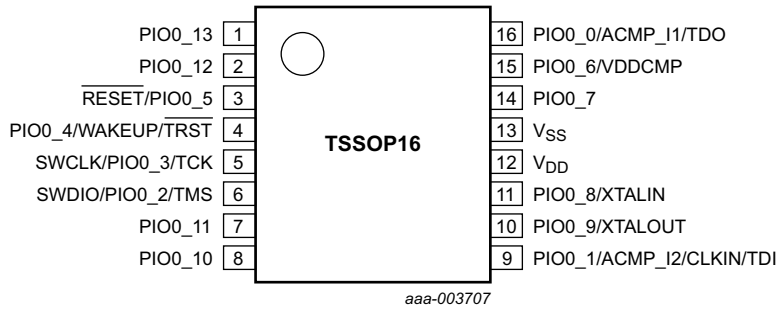


Fig 3. Pin configuration TSSOP16 package (LPC811M001JDH16 and LPC812M101JDH16)

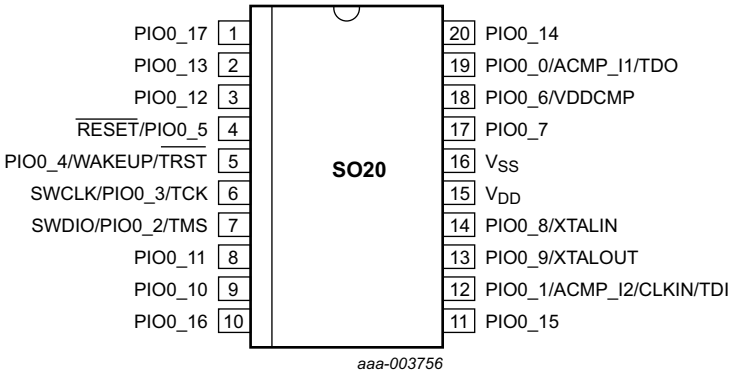


Fig 4. Pin configuration SO20 package (LPC812M101JD20)

- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK)is generated by a the dedicated watchdog oscillator (WDOSC).

8.18 Self Wake-up Timer (WKT)

The self wake-up timer is a 32-bit, loadable down-counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur just prior to entering a reduced power mode.

8.18.1 Features

- 32-bit loadable down-counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports two clock sources: the low-power oscillator and the IRC. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in Deep power-down mode.
- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 23.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled or disabled on pins PIO0_0 and PIO0_1 through the switch matrix.

8.20 Clocking and power control

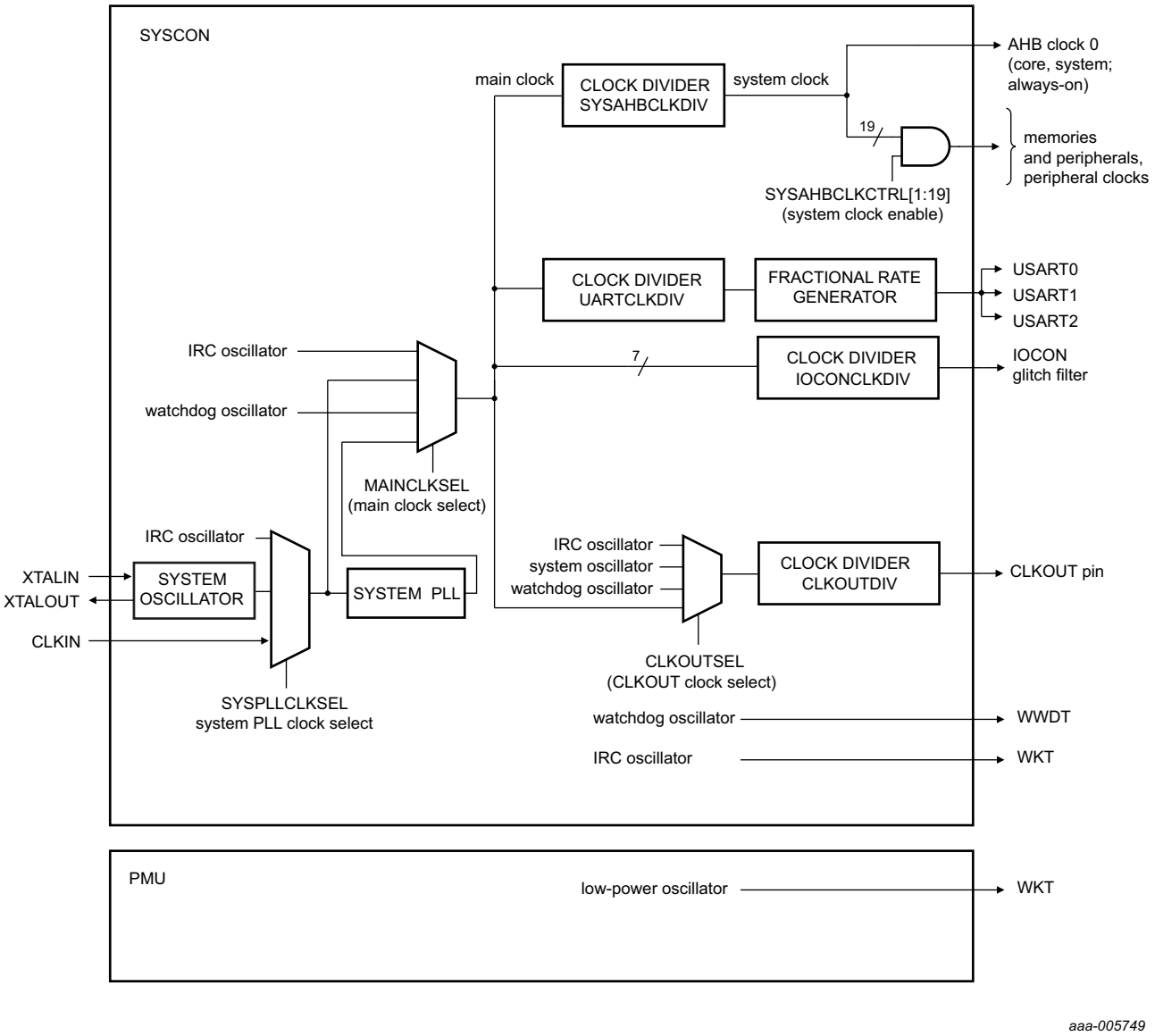


Fig 10. LPC81xM clock generation

8.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

8.21.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC800 user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC800 user manual*.

8.21.4 APB interface

The APB peripherals are located on one APB bus.

8.21.5 AHBLite

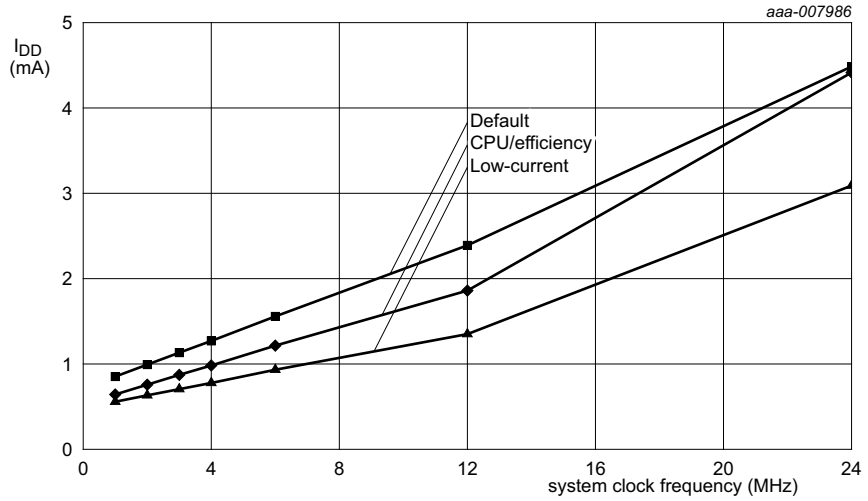
The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, and the ROM.

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

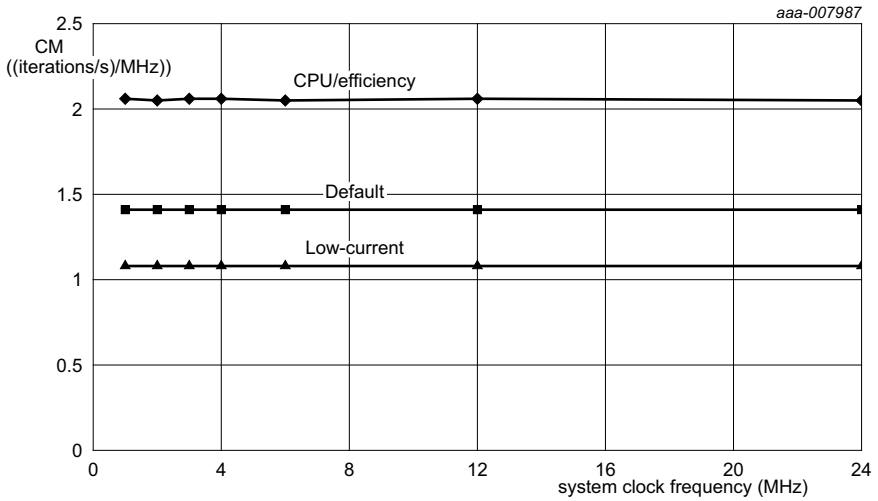
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_I	input voltage	$V_{DD} \geq 1.8$ V	[11] [12]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = 20 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = 12 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[14]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V	[14]	15	50	85	μA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
I^2C-bus pins (PIO0_10 and PIO0_11); see Figure 13							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.5 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[15]	-	2	4	μA
		V_I = 5 V		-	10	22	μA

11.2 CoreMark data



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; system clock derived from the IRC; system oscillator disabled; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.7.

Fig 20. Active mode: CoreMark power consumption I_{DD}



Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.7.

Fig 21. CoreMark score

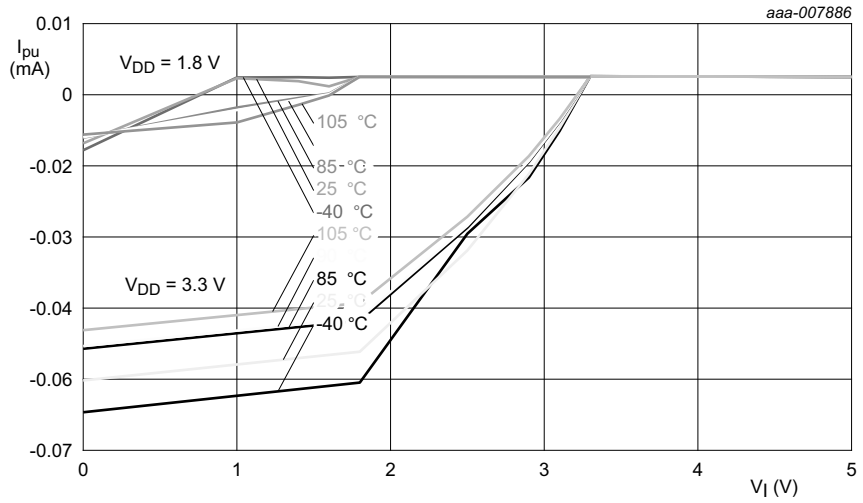
11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 30 MHz.

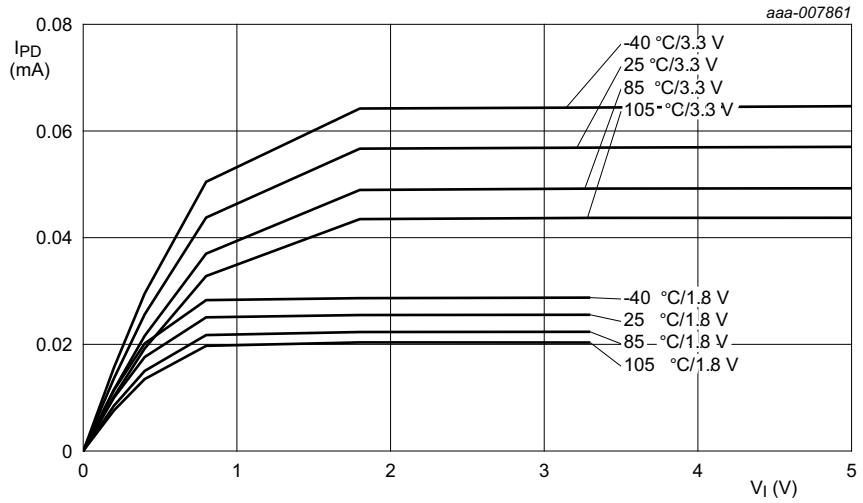
Table 10. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	30 MHz	
IRC	0.21	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.002	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
Main PLL	-	0.31	-	-
CLKOUT	-	0.06	0.09	Main clock divided by 4 in the CLKOUTDIV register.
ROM	-	0.08	0.19	-
I2C	-	0.06	0.15	-
GPIO + pin interrupt/pattern match	-	0.09	0.23	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	0.03	0.07	-
SCT	-	0.17	0.42	-
WKT	-	0.01	0.03	-
MRT	-	0.09	0.21	-
SPI0	-	0.05	0.13	-
SPI1	-	0.06	0.14	-
CRC	-	0.03	0.07	-
USART0	-	0.04	0.10	-
USART1	-	0.04	0.11	-
USART2	-	0.04	0.10	-
WWDT	-	0.04	0.10	Main clock selected as clock source for the WDT.
IOCON	-	0.03	0.08	-
Comparator	-	0.04	0.09	-



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 26. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 27. Typical pull-down current I_{pd} versus input voltage V_I

12.5 I/O pins

Table 16. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.6 I²C-bus

Table 17. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

12.7 SPI interfaces

The maximum data bit rate is 30 Mbit/s in master mode and 25 Mbit/s in slave mode.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

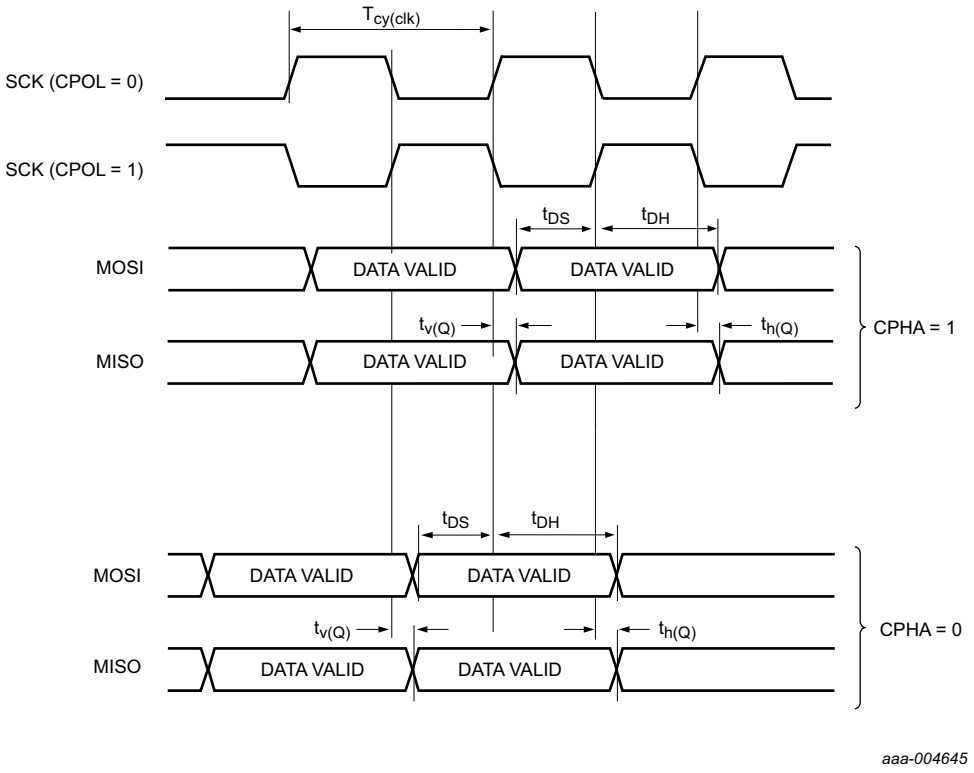
Table 18. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V. Simulated parameters sampled at the 50 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master[1]						
$T_{cy(clk)}$	clock cycle time		[2]	33	-	ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	0.5	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		0.5	-	ns
SPI slave						
$T_{cy(clk)}$				40		ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	10	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		10	-	ns

[1] Capacitance on pin SPIn_SCK C_{SCK} < 5 pF.

[2] $T_{cy(clk)}$ = DIVVAL/CCLK with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the *LPC800 User manual UM10601*.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 33. SPI slave timing

Table 22. Comparator characteristics *…continued*

V_{DD} = 3.0 V and T_{amb} = 27 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	109	121	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	155	164	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	95	105	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	101	108	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	122	129	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	74	82	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	246	260	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	57	59	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	218		ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	146	155	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	184	206	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	250	286	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2]	-	6, 11, 21	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2][2]	-	4, 9, 19	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = −40 °C to +105 °C. Typical data are for T_{amb} = 27 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable to three levels.

Table 23. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

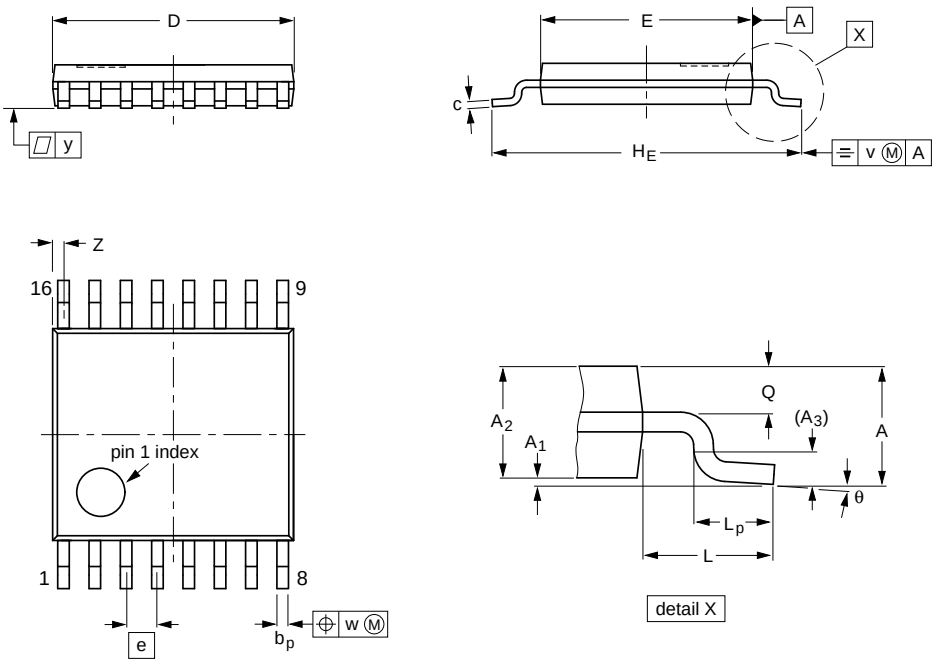
[1] Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 105 °C; slow process models).

[2] Settling time applies to switching between comparator channels.

14.3 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 39. Package outline SOT403-1 (TSSOP16)

17. Abbreviations

Table 29. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] I2C-bus specification *UM10204*.

19. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC81XM v.4.6	20180404	Product data sheet	201804004I	LPC81XM v.4.5
Modifications:	• Updated table note 2 of Section 12.1 “Power-up ramp conditions”.			
LPC81XM v.4.5	20160603	Product data sheet	-	LPC81XM v.4.4
Modifications:	• Added Section 12.1 “Power-up ramp conditions”. • Updated Figure 4 “Pin configuration SO20 package (LPC812M101JD20)”: Corrected function of pin 12 to ACMP_I2. • Updated the remark in Section 8.12 “USART0/1/2” to: USART2 is available on parts LPC812M101JTB16, LPC812M101JDH16, and LPC812M101JDH20 only.			
LPC81XM v.4.4	20150619	Product data sheet	-	LPC81XM v.4.3
Modifications:	• Section 14.4 “ElectroMagnetic Compatibility (EMC)” added.			
LPC81XM v.4.3	20140422	Product data sheet	-	LPC81XM v.4.2
Modifications:	• Section 8.20.2 “Clock input” updated for clarity. • CLKIN signal removed from Table 13 “Dynamic characteristic: external clock (XTALIN inputs)”. • Name “SCT” changed to “SCTimer/PWM” for clarity. • Remove slew rate control from GPIO features for clarity. • MRT bus stall mode added. • WWDT clock source corrected in Section 8.17.1. • Pin description table updated for clarification (I2C-bus pins, WAKEUP, $\overline{\text{RESET}}$). • Added reflow solder diagram and thermal resistance numbers for XSON16 (SOT1341-1). • Table 22: Added $V_{ref(cmp)}$ spec for PIO0_6/VDDCMP..			
LPC81XM v.4.2	20131210	Product data sheet	-	LPC81XM v.4.1
Modifications:	Corrected vertical axis marker in Figure 21 “CoreMark score”.			
LPC81XM v.4.1	20131112	Product data sheet	-	LPC81XM v.4
Modifications:	• Corrected XSON16 pin information in Figure 6 and Table 4.			
LPC81XM v.4	20131025	Product data sheet	-	LPC81XM v.3.1
Modifications:	• Added Section 14.1 “Typical wake-up times”. • Added LPC812M101JTB16 and XSON16 package.			
LPC81XM v.3.1	20130916	Product data sheet	-	LPC81XM v.3
Modifications:	• Correct the pin interrupt features: Pin interrupts can wake up the part from Sleep mode, Deep-sleep mode, and Power-down mode. See Section 8.11.1. • Table 9 “Static characteristics”: Updated power numbers for Deep-sleep, Power-down, and Deep power-down. • Added 30 MHz data to Figure 13 “Active mode: Typical supply current IDD versus supply voltage VDD”, Figure 14 “Active mode: Typical supply current IDD versus temperature”, and Figure 15 “Sleep mode: Typical supply current IDD versus temperature for different system clock frequencies”.			
LPC81XM v.3	20130729	Product data sheet	-	LPC81XM v.2.1

Table 30. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Operating temperature range changed to −40 °C to 105 °C. • Type numbers updated to reflect the new operating temperature range. See Table 1 “Ordering information” and Table 2 “Ordering options”. • ISP entry pin moved from PIO0_1 to PIO0_12 for TSSOP, and SSOP packages. See Table 4 and Table 6. • Propagation delay values updated in Table 21 “Comparator characteristics”. • SPI characteristics updated. See Section 12.6. • IRC characteristics updated. See Section 12.3. • CoreMark data updated. See Figure 19 and Figure 20. • IRC frequency changed to 12 MHz +/- 1.5 %. See Table 13. • Data sheet status updated to Product data sheet.			
LPC81XM v.2.1	20130325	Preliminary data sheet	-	LPC81XM v.2
	• Editorial updates (temperature sensor removed). • CoreMark data added. See Figure 19 “Active mode: CoreMark power consumption IDD” and Figure 20 “CoreMark score”. • I_{DD} in Deep power-down mode added for condition Low-power oscillator on/WKT wake-up enabled. See Table 10. • Table note 3 updated for Table 4 “Pin description table (fixed pins)”. • Conditions for t_{er} and t_{prog} updated in Table 12 “Flash characteristics”. • Section 13.3 “Internal voltage reference” added. • Typical timing data added for SPI. See Section 12.6. • Typical timing data added for USART in synchronous mode. See Section 12.7. • BOD characterization added. See Section 13.1. • IRC characterization added. See Section 12.3. • Internal voltage reference characteristics added. See Section 13.3. • Data sheet status changed to Preliminary data sheet.			
LPC81XM v.2	20130128	Objective data sheet	-	LPC81XM v.1
Modifications:	• MTB memory space changed to 1 kB in Figure 6. • Electrical pin characteristics added in Table 10. • Figure 11 “Connecting the SWD pins to a standard SWD connector” added. • Peripheral power consumption added in Table 11. • Table 7 updated. • MRT implementation changed to 31-bit timer. • Power consumption data in active and sleep mode with IRC added. See Figure 13 to Figure 15. • Power consumption (parameter I_{DD}) in active and sleep mode for low-power mode at 12 MHz corrected in Table 10. • Power consumption (parameter I_{DD}) in active and sleep mode at 24 MHz added in Table 10. • Maximum USART speed in synchronous mode changed to 10 Mbit/s. • Section 5 “Marking” added.			
LPC81XM v.1	20121112	Objective data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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