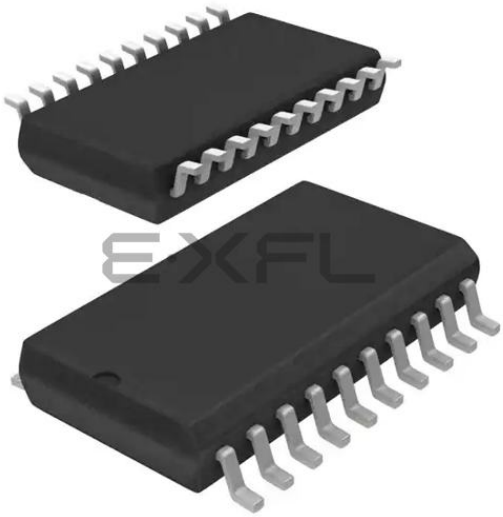

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101jd20j

- State Configurable Timer/PWM (SCTimer/PWM) with input and output functions (including capture and match) assigned to pins through the switch matrix.
- Multiple-channel multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Self Wake-up Timer (WKT) clocked from either the IRC or a low-power, low-frequency internal oscillator.
- CRC engine.
- Windowed Watchdog timer (WWDT).

- Analog peripherals:
  - Comparator with internal and external voltage references with pin functions assigned or enabled through the switch matrix.
- Serial interfaces:
  - Three USART interfaces with pin functions assigned through the switch matrix.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - One I^2C-bus interface with pin functions assigned through the switch matrix.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1.5 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - 10 kHz low-power oscillator for the WKT.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input CLKIN, or the internal RC oscillator.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from Deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect.
- Unique device serial number for identification.
- Single power supply.
- Operating temperature range −40 °C to 105 °C except for the DIP8 package, which is available for a temperature range of −40 °C to 85 °C.
- Available as DIP8, TSSOP16, SO20, TSSOP20, and XSON16 package.

3. Applications

- 8/16-bit applications
- Consumer
- Climate control
- Lighting
- Motor control
- Fire and security applications

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_12	3	2	2	-	[2]	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin. ISP entry pin on the SO20/TSSOP20/TSSOP16/XSON16 packages starting with chip version 4C (see Table 6). A LOW level on this pin during reset starts the ISP command handler. See pin PIO0_1 for the DIP8 package and chip versions 1A and 2A.
PIO0_13	2	1	1	-	[2]	I/O	I; PU	**PIO0_13 —** General purpose digital input/output pin.
PIO0_14	20	-	-	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin.
PIO0_15	11	-	-	-	[7]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin.
PIO0_16	10	-	-	-	[7]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin.
PIO0_17	1	-	-	-	[7]	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin.
V_{DD}	15	12	12	6		-	-	3.3 V supply voltage.
V_{SS}	16	13	13	7		-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[3] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

Remark: If this pin is not available on the package, prevent it from internally floating as follows: Set bits 10 and 11 in the GPIO DIR0 register to 1 to enable the output driver and write 1 to bits 10 and 11 in the GPIO CLR0 register to drive the outputs LOW internally.

[4] See Figure 11 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[5] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. In Deep power-down mode, pulling this pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low power oscillator is enabled for waking up the part from Deep power-down mode.

[7] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured as an analog I/O, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

Table 5. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.

Table 5. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
$\overline{\text{U1\_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U1\_CTS}}$	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
$\overline{\text{U2\_RTS}}$	O	Request To Send output for USART2.
$\overline{\text{U2\_CTS}}$	I	Clear To Send input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART2 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL	I/O	Slave select for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL	I/O	Slave select for SPI1.
CTIN_0	I	SCT input 0.
CTIN_1	I	SCT input 1.
CTIN_2	I	SCT input 2.
CTIN_3	I	SCT input 3.
CTOUT_0	O	SCT output 0.
CTOUT_1	O	SCT output 1.
CTOUT_2	O	SCT output 2.
CTOUT_3	O	SCT output 3.
I2C0_SCL	I/O	I^2C-bus clock input/output (open-drain if assigned to pin PIO0_10). High-current sink only if assigned to PIO0_10 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
I2C0_SDA	I/O	I^2C-bus data input/output (open-drain if assigned to pin PIO0_11). High-current sink only if assigned to pin PIO0_11 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
ACMP_O	O	Analog comparator digital output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

Table 6. Pin location in ISP mode

ISP entry pin	USART RXD	USART TXD	Marking	Boot loader version	Package
PIO0_1	PIO0_0	PIO0_4	1A	v 13.1	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	2A	v 13.2	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	4C and later	v 13.4 and later	DIP8
PIO0_12	PIO0_0	PIO0_4	4C and later	v 13.4 and later	TSSOP20; SO20; TSSOP16; XSON16

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC81xM contain a total of up to 4 kB on-chip static RAM data memory.

8.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I^2C-bus driver API routines

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Relocatable interrupt vector table using vector table offset register.

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight pins, regardless of the selected function, can be programmed to generate an interrupt on a level, a rising or falling edge, or both. The interrupt generating pins can be selected from all digital or mixed digital/analog pins. The pin interrupt/pattern match block controls the edge or level detection mechanism.

8.6 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.7 Memory map

The LPC81xM incorporates several distinct memory regions. Figure 7 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

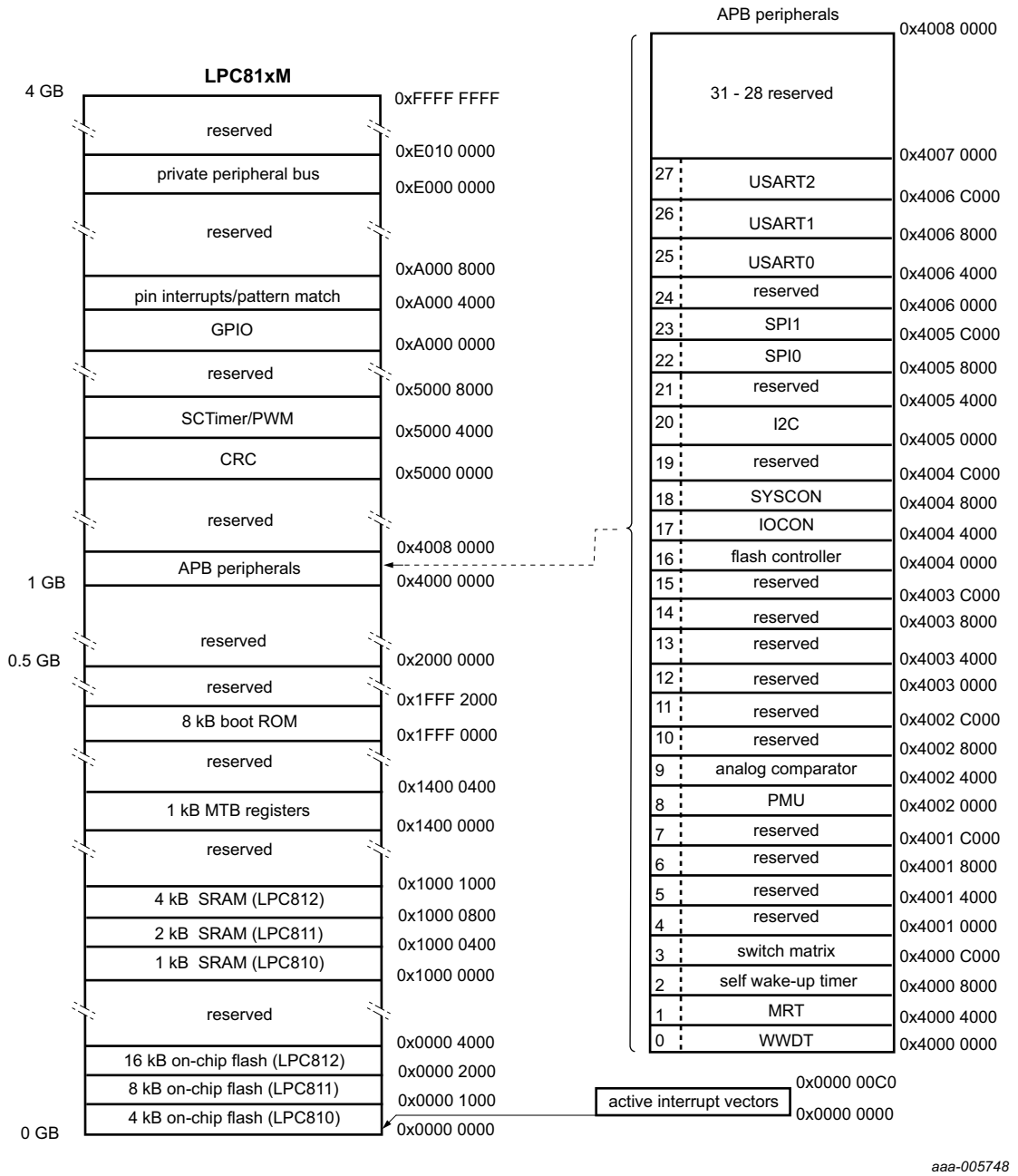


Fig 7. LPC81xM Memory map

8.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. This pin is not 5 V tolerant when V_{DD} = 0.

- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 10 “LPC81xM clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

8.8.1 Standard I/O pad configuration

Figure 8 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 8).
-

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.

8.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

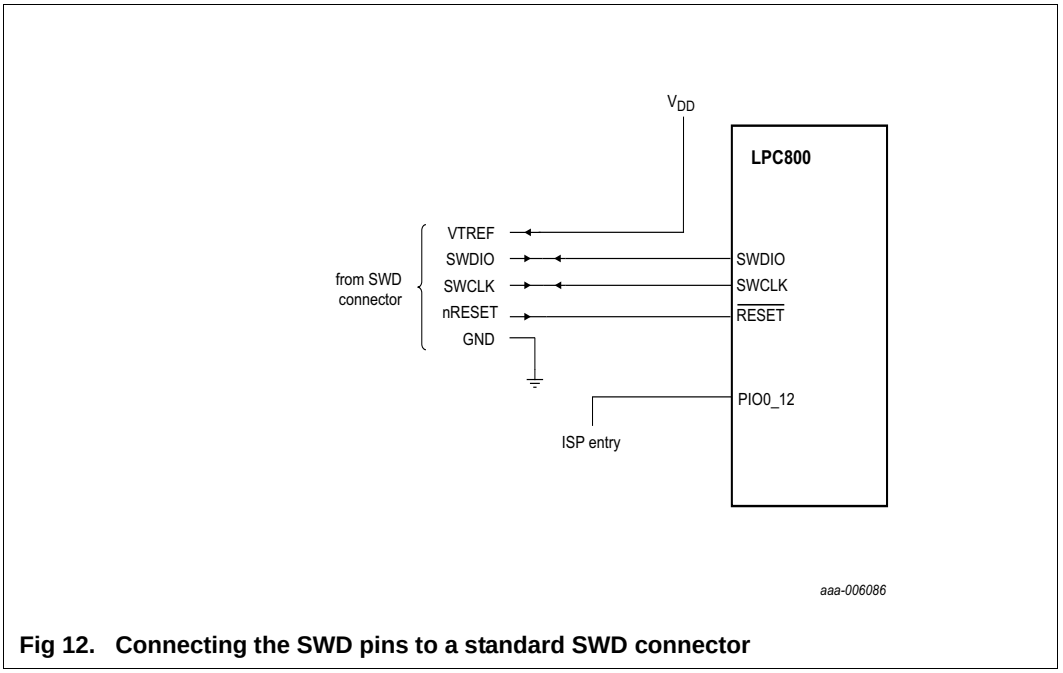


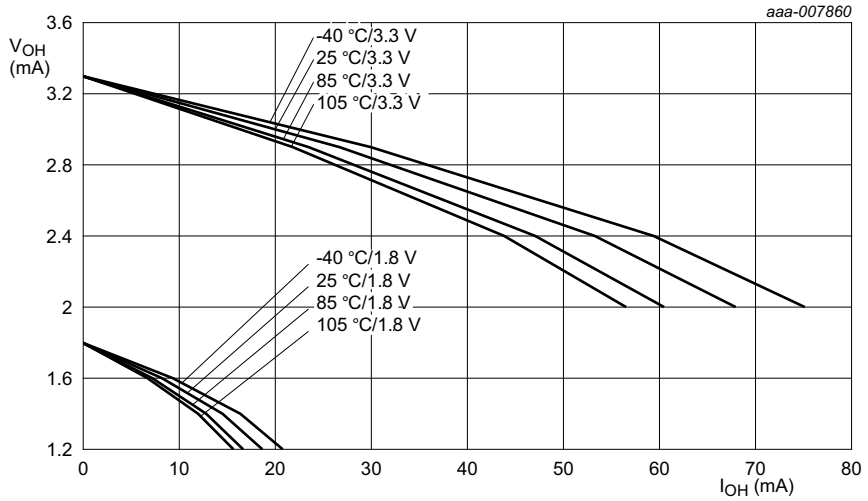
Fig 12. Connecting the SWD pins to a standard SWD connector

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

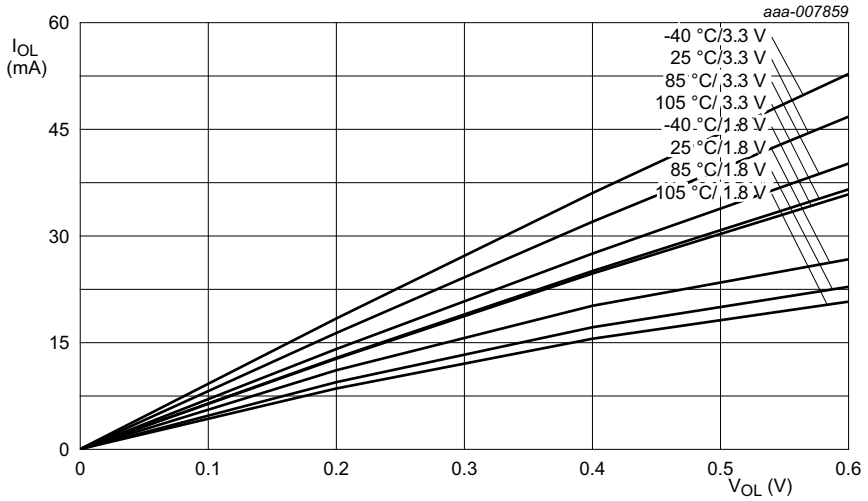
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_I	input voltage	$V_{DD} \geq 1.8$ V	[11] [12]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = 20 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = 12 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[14]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V	[14]	15	50	85	μA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
I^2C-bus pins (PIO0_10 and PIO0_11); see Figure 13							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.5 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[15]	-	2	4	μA
		V_I = 5 V		-	10	22	μA

11.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; on pins PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13.

Fig 22. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; on pins PIO0_10 and PIO0_11.

Fig 23. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

Table 22. Comparator characteristics *…continued*

V_{DD} = 3.0 V and T_{amb} = 27 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	109	121	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	155	164	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	95	105	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	101	108	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	122	129	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	74	82	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	246	260	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	57	59	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	218		ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	146	155	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	184	206	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	250	286	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2]	-	6, 11, 21	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2][2]	-	4, 9, 19	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = −40 °C to +105 °C. Typical data are for T_{amb} = 27 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable to three levels.

Table 23. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 105 °C; slow process models).

[2] Settling time applies to switching between comparator channels.

14.3 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14.4 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC812M101FDH20.

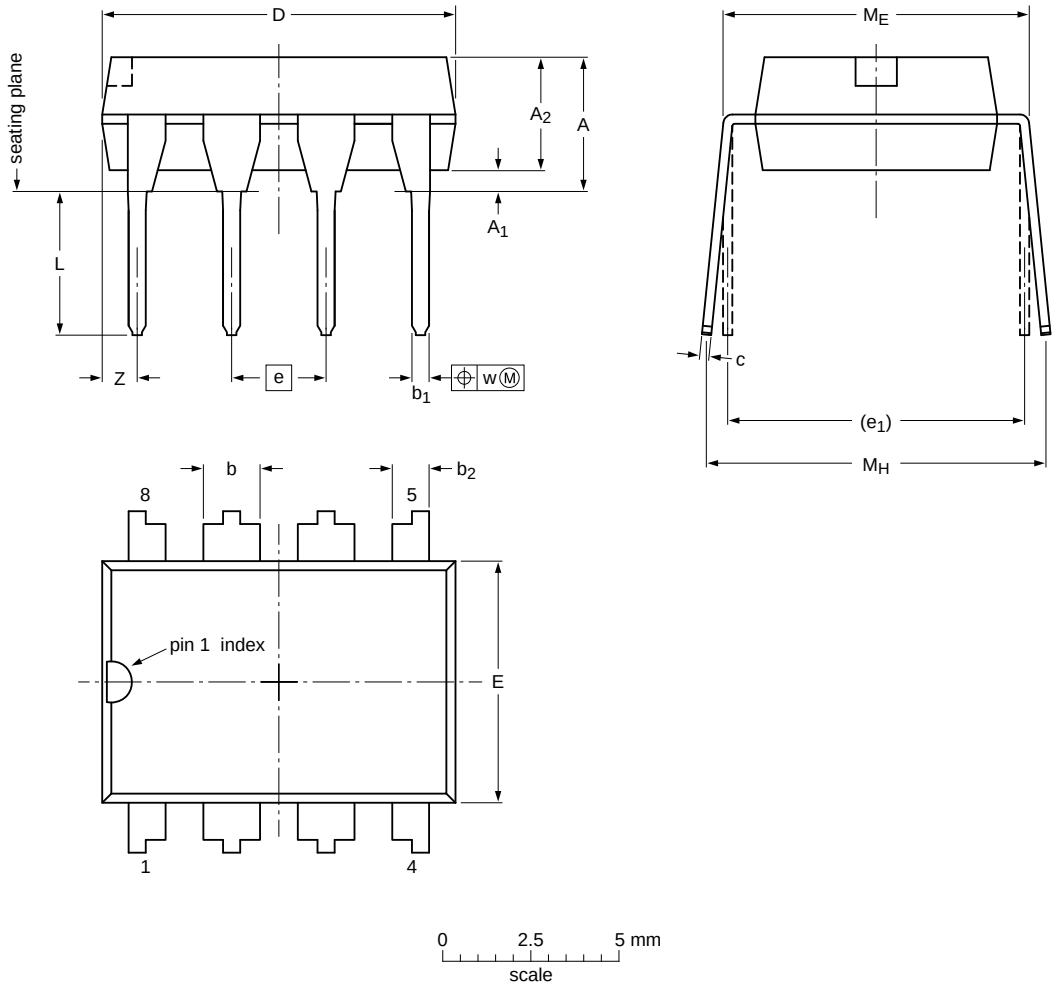
Table 28. ElectroMagnetic Compatibility (EMC) for part LPC812M101 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	30 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	1 MHz to 30 MHz	–6	–5	–5	dBμV
	30 MHz to 150 MHz	-2	-1	-2	dBμV
	150 MHz to 1 GHz	–1	-1	-1	dBμV
IEC level[1]	-	O	O	O	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	1 MHz to 30 MHz	–5	–6	–6	dBμV
	30 MHz to 150 MHz	–2	-1	-2	dBμV
	150 MHz to 1 GHz	–1	-2	-1	dBμV
IEC level[1]	-	O	O	N	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

15. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-2**



Dimensions (inch dimensions are derived from the original dimensions)

Unit[1]		A	A_1	A_2	b	b_1	b_2	c	D[1]	E[1]	e	e_1	L	M_E	M_H	w	Z[1]
mm	max	4.2		3.43	1.73	0.53	1.07	0.38	9.8	6.48			3.60	7.88	9.40		1.15
	nom										2.54	7.62				0.254	
	min		0.51		1.14	0.38	0.89	0.20	9.2	6.20			3.05	7.62	7.88		
inches	max	0.17		0.14	0.068	0.021	0.042	0.015	0.39	0.26			0.14	0.31	0.37		0.045
	nom										0.1					0.01	
	min		0.02		0.045	0.015	0.035	0.008	0.36	0.24		0.3	0.12	0.30	0.31		

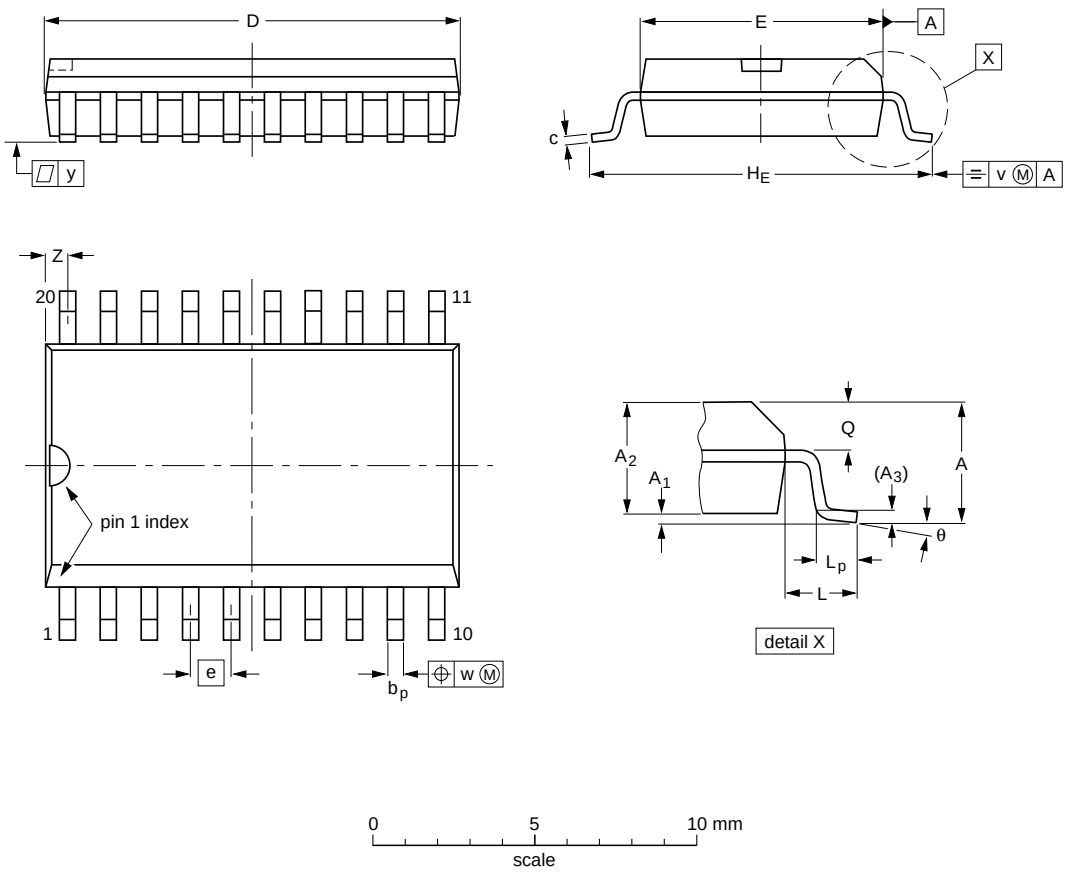
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included

sot097-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT97-2	- - -	MO-001	- - -			~~10-10-15~~ 10-10-18

Fig 38. Package outline SOT097-2 (DIP8)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

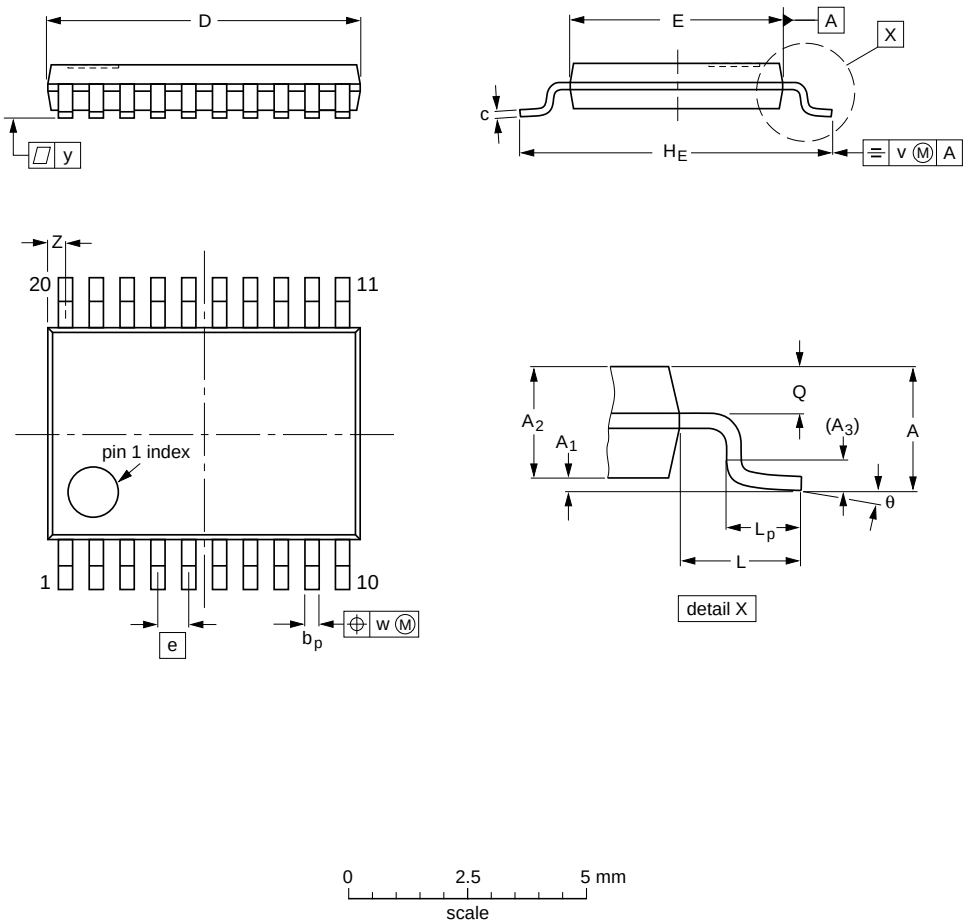
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 40. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

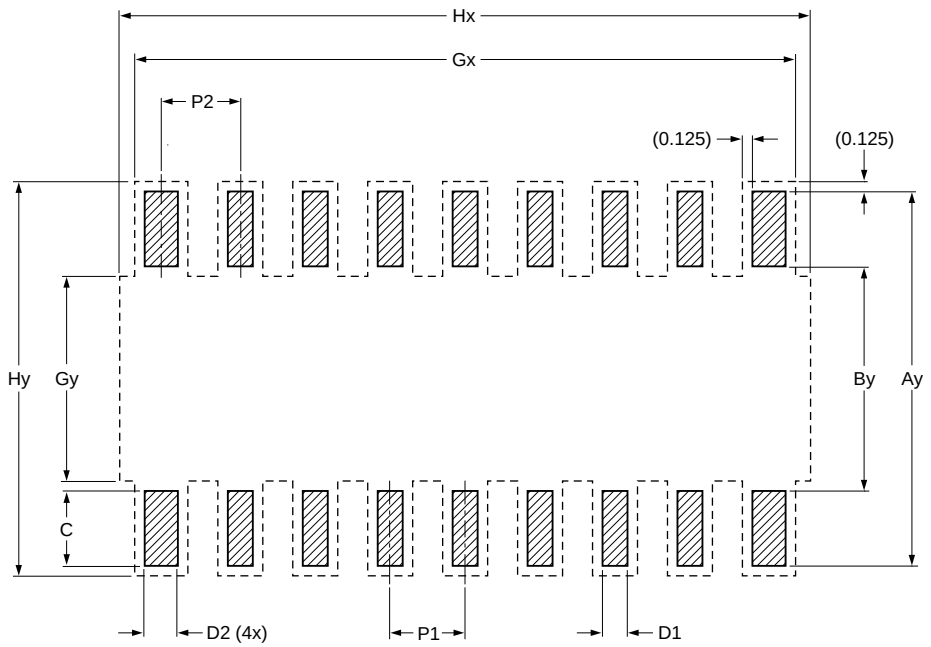
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 41. Package outline SOT360-1 (TSSOP20)

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 45. Reflow soldering of the TSSOP20 package

Footprint information for reflow soldering of XSON16 package **SOT1341-1**

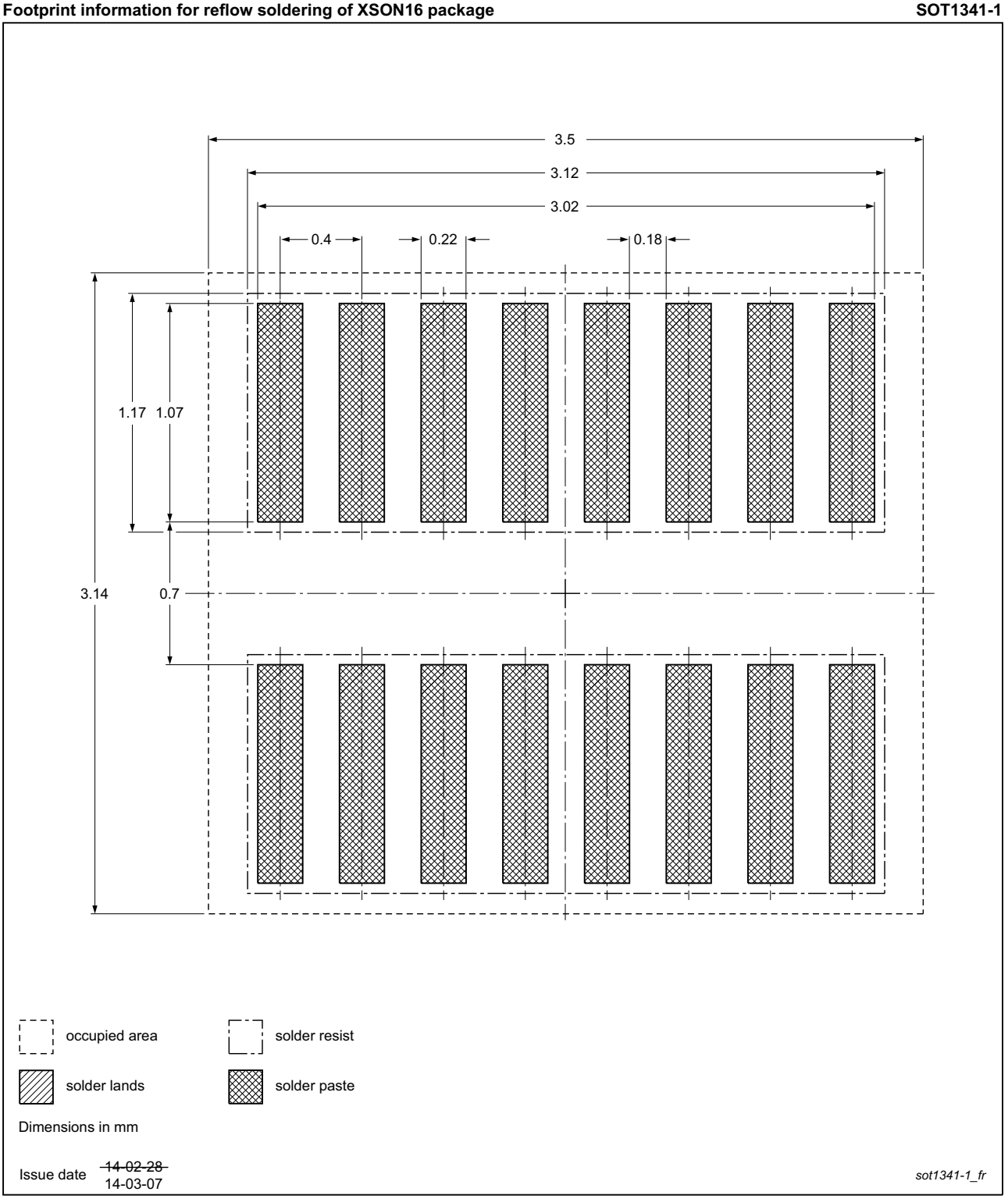


Fig 46. Reflow soldering of the XSON16 package