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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101jdh16j

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC810M021FN8	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT097-2
LPC811M001JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JD20	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC812M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC812M101JTB16	XSON16	plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 × 3.2 × 0.5 mm	SOT1341-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/kB	SRAM/kB	USART	I^2C-bus	SPI	Comparator	GPIO	Package
LPC810M021FN8	4	1	2	1	1	1	6	DIP8
LPC811M001JDH16	8	2	2	1	1	1	14	TSSOP16
LPC812M101JDH16	16	4	3	1	2	1	14	TSSOP16
LPC812M101JD20	16	4	2	1	1	1	18	SO20
LPC812M101JDH20	16	4	3	1	2	1	18	TSSOP20
LPC812M101JTB16	16	4	3	1	2	1	14	XSON16

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_12	3	2	2	-	[2]	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin. ISP entry pin on the SO20/TSSOP20/TSSOP16/XSON16 packages starting with chip version 4C (see Table 6). A LOW level on this pin during reset starts the ISP command handler. See pin PIO0_1 for the DIP8 package and chip versions 1A and 2A.
PIO0_13	2	1	1	-	[2]	I/O	I; PU	**PIO0_13 —** General purpose digital input/output pin.
PIO0_14	20	-	-	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin.
PIO0_15	11	-	-	-	[7]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin.
PIO0_16	10	-	-	-	[7]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin.
PIO0_17	1	-	-	-	[7]	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin.
V_{DD}	15	12	12	6		-	-	3.3 V supply voltage.
V_{SS}	16	13	13	7		-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[3] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

Remark: If this pin is not available on the package, prevent it from internally floating as follows: Set bits 10 and 11 in the GPIO DIR0 register to 1 to enable the output driver and write 1 to bits 10 and 11 in the GPIO CLR0 register to drive the outputs LOW internally.

[4] See Figure 11 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[5] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. In Deep power-down mode, pulling this pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low power oscillator is enabled for waking up the part from Deep power-down mode.

[7] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured as an analog I/O, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

Table 5. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.

Table 5. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
$\overline{\text{U1\_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U1\_CTS}}$	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
$\overline{\text{U2\_RTS}}$	O	Request To Send output for USART2.
$\overline{\text{U2\_CTS}}$	I	Clear To Send input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART2 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL	I/O	Slave select for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL	I/O	Slave select for SPI1.
CTIN_0	I	SCT input 0.
CTIN_1	I	SCT input 1.
CTIN_2	I	SCT input 2.
CTIN_3	I	SCT input 3.
CTOUT_0	O	SCT output 0.
CTOUT_1	O	SCT output 1.
CTOUT_2	O	SCT output 2.
CTOUT_3	O	SCT output 3.
I2C0_SCL	I/O	I^2C-bus clock input/output (open-drain if assigned to pin PIO0_10). High-current sink only if assigned to PIO0_10 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
I2C0_SDA	I/O	I^2C-bus data input/output (open-drain if assigned to pin PIO0_11). High-current sink only if assigned to pin PIO0_11 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
ACMP_O	O	Analog comparator digital output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC81xM contain a total of up to 4 kB on-chip static RAM data memory.

8.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I^2C-bus driver API routines

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Relocatable interrupt vector table using vector table offset register.

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

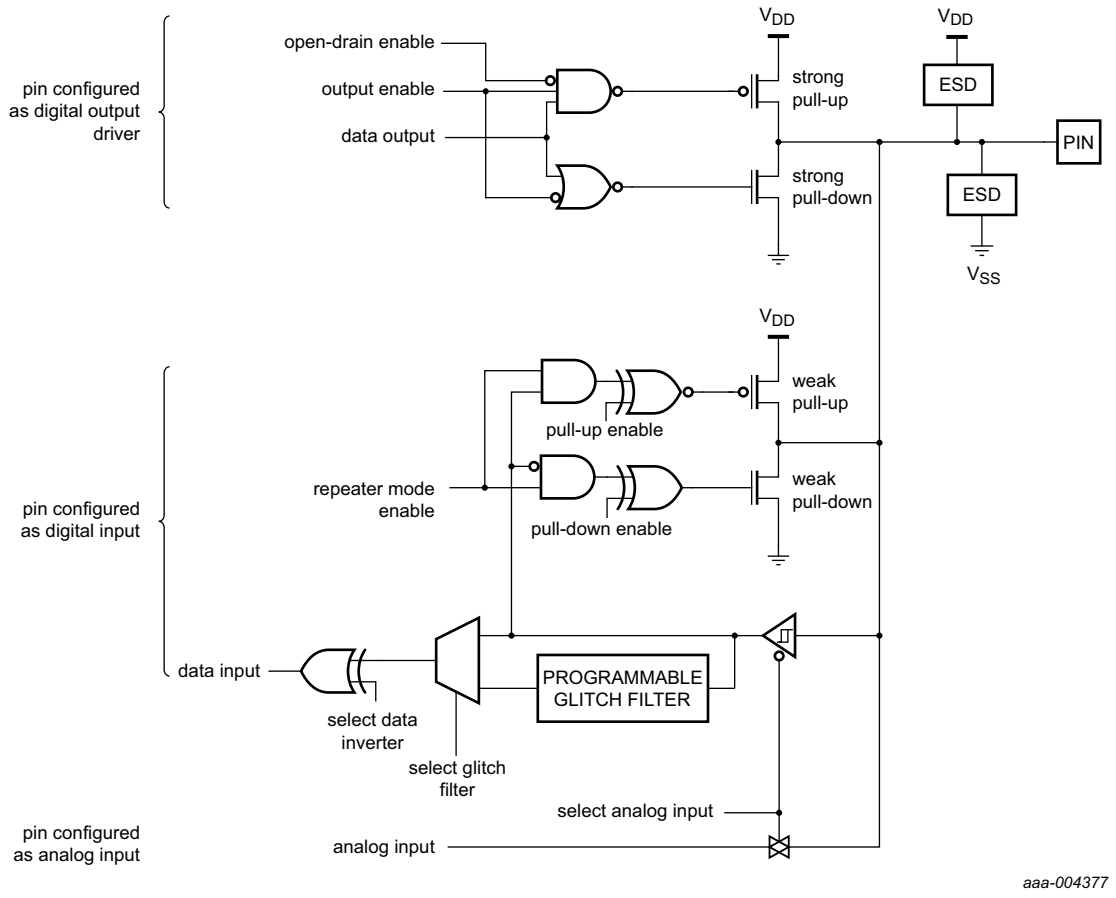


Fig 8. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 4. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 8).
-

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.

8.20 Clocking and power control

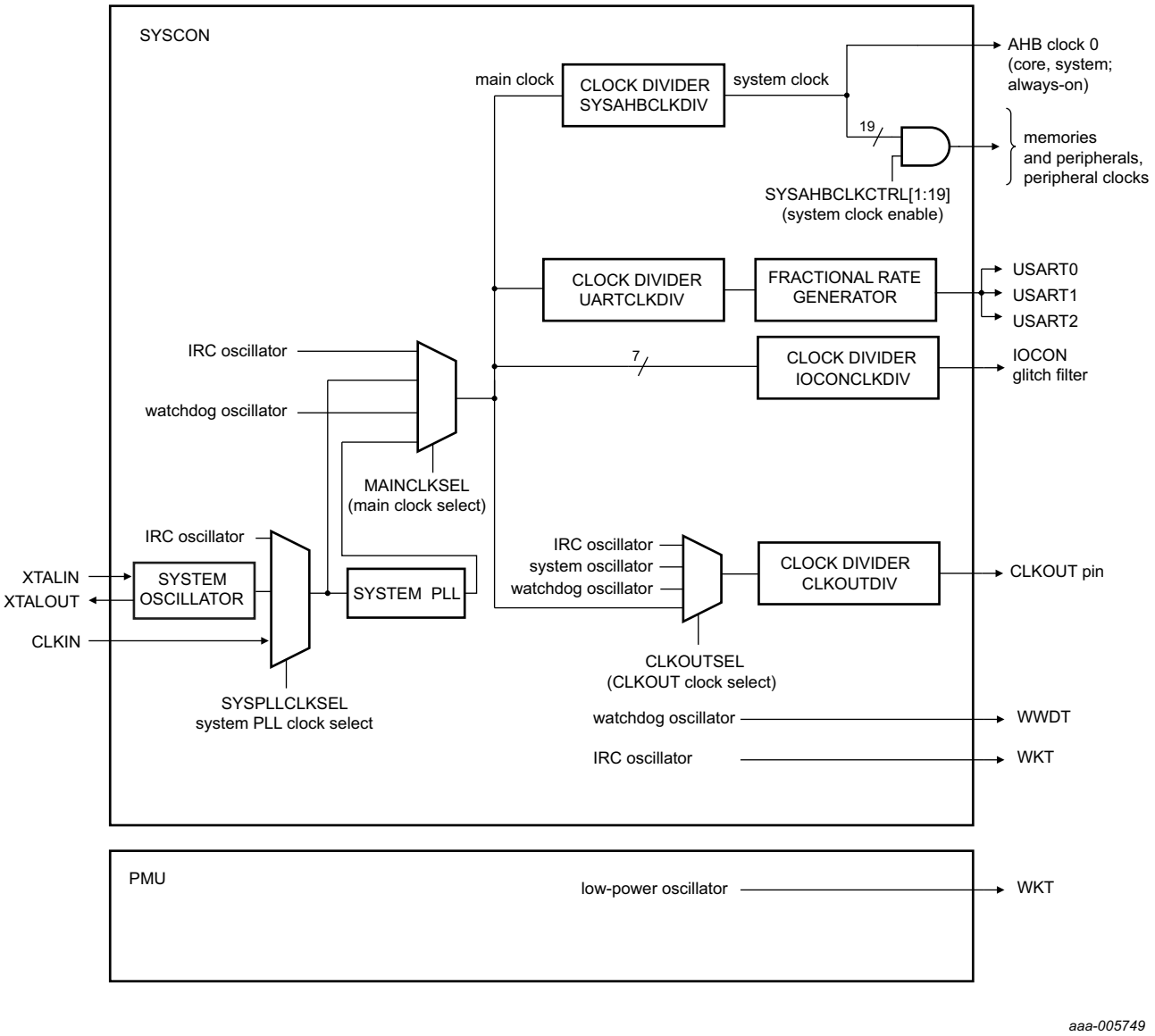


Fig 10. LPC81xM clock generation

8.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

8.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

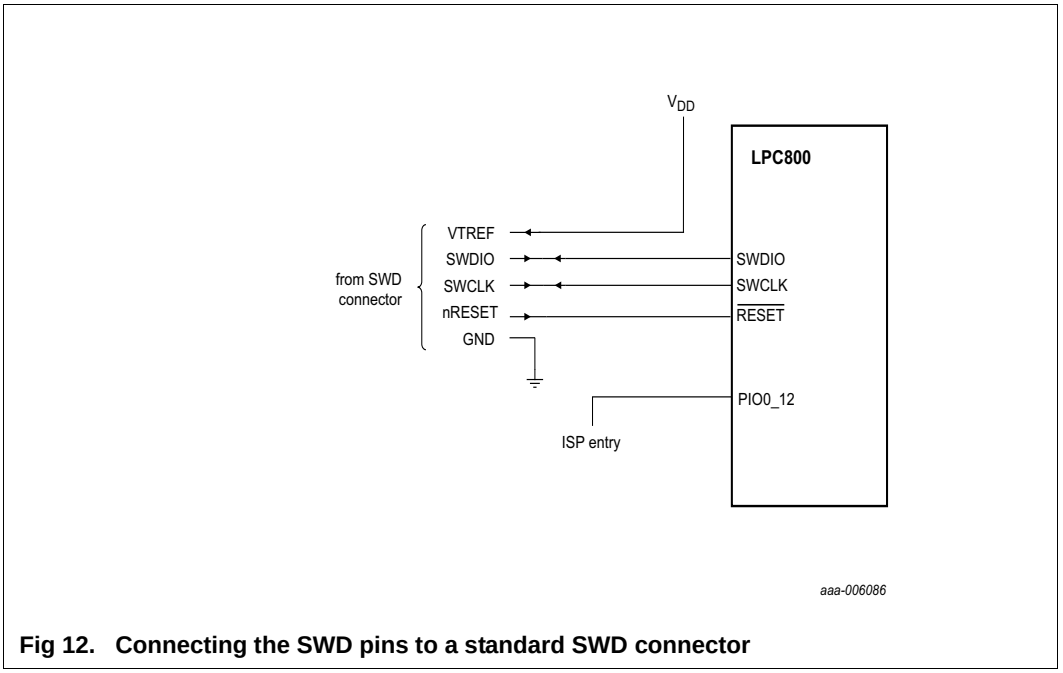


Fig 12. Connecting the SWD pins to a standard SWD connector

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V	[3]	−0.5	+5.5	V
		5 V tolerant open-drain pins PIO0_10 and PIO0_11	[4]	−0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	[5]	−0.5	+3.6	V
V_{IA}	analog input voltage		[6] [7]	−0.5	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[8]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[9]	-	5500	V
		charged device model; TSSOP20 and SOP20 packages		-	1200	V
		charged device model; TSSOP16 package		-	1000	V
		charged device model; XSON16 package		-	800	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 9.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 9) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Including voltage on outputs in tri-state mode. Does not apply to pin PIO0_6.

[4] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] V_{DD} present or not present.

[6] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[8] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[9] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

11. Static characteristics

Table 9. Static characteristics

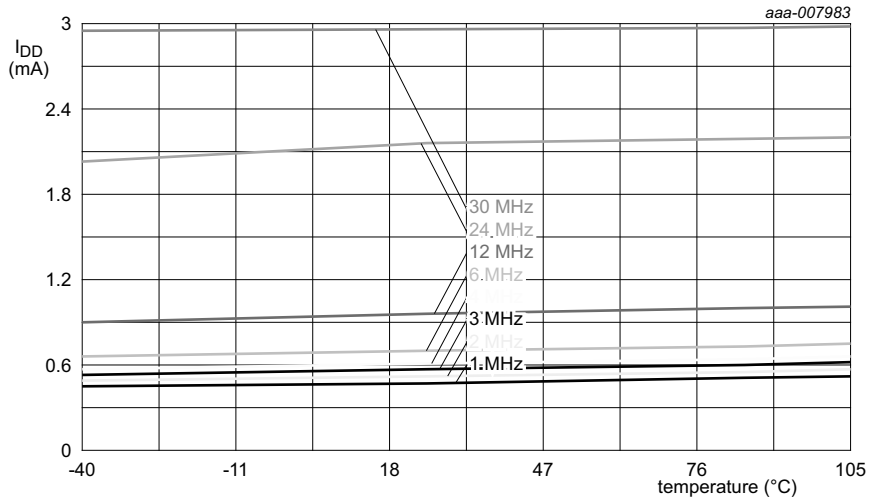
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][5]	-	1.4	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][5][6]	-	1.0	-	mA
		system clock = 24 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][7]	-	2.2	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][4][5][8]	-	3.3	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][8]	-	3	-	mA
		Sleep mode					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][5]	-	0.8	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][5][6]	-	0.7	-	mA
		system clock = 24 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][7]	-	1.3	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][4][5][8]	-	1.8	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][8]	-	1.7	-	mA
		Deep-sleep mode					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[2][9]	-	150	300	µA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[2][9]	-	-	400	µA
		Power-down mode					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[2][9]	-	0.9	5	µA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[2][9]	-	-	40	µA
		Deep power-down mode; Low-power oscillator and self wakeup timer (WKT) disabled					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[10]	-	170	1000	nA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[10]	-	-	4	µA
		Deep power-down mode; Low-power oscillator and self wakeup timer (WKT) enabled		-	1	-	µA

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, $\overline{\text{RESET}}$; see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_6	[11] [12]	0	-	5.0	V
		$V_{DD} \geq$ 1.8 V; on 3 V tolerant pin PIO0_6		0	-	3.6	
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = 4 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = 3 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[13]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		15	50	85	μA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	μA
		$V_{DD} < V_I$ < 5 V		0	0	0	μA
High-drive output pins configured as digital pins (PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13); see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA



Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: IRC disabled; SYSOSC enabled; PLL enabled.

Fig 15. Active mode: Typical supply current I_{DD} versus temperature

12. Dynamic characteristics

12.1 Power-up ramp conditions

Table 11. Power-up characteristics

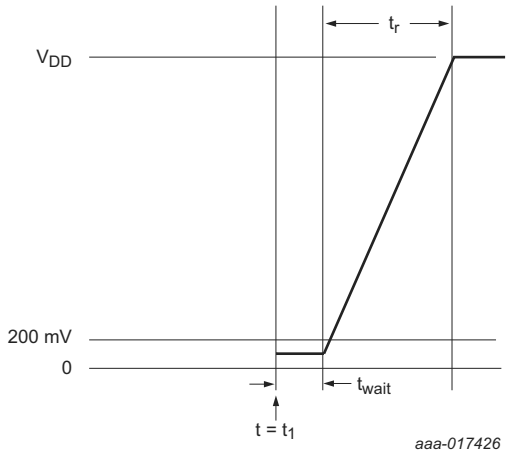
T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 200 mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2][3]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	200	mV

[1] See Figure 28.

[2] The wait time specifies the time the power supply must be at levels below 200 mV before ramping up. See the LPC81x errata sheet.

[3] Based on characterization, not tested in production.



Condition: 0 < V_I ≤ 200 mV at start of power-up (t = t_1)

Fig 28. Power-up ramp

12.2 Flash memory

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ret}	retention time	powered		10	20	-	years
		unpowered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. $T_{amb} \leq +85$ °C. Flash programming with IAP calls (see *LPC800 user manual*).

12.3 External clock for the oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.95 V (see Table 9). For connecting the oscillator to the XTAL pins, also see Section 14.2.

Table 13. Dynamic characteristic: external clock (XTALIN inputs)

T_{amb} = −40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

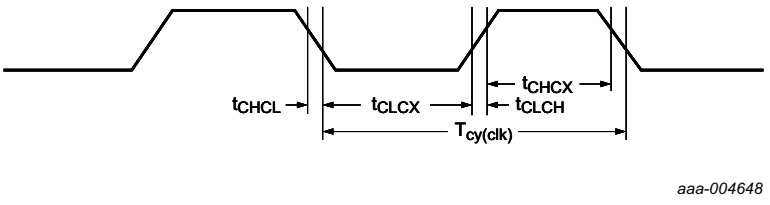


Fig 29. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

[3] Typical values are derived from nominal simulation (V_{DD} = 3.3 V; T_{amb} = 27 °C; nominal process models). Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 105 °C; slow process models).

[4] Maximum and minimum values are measured on samples from the corners of the process matrix lot.

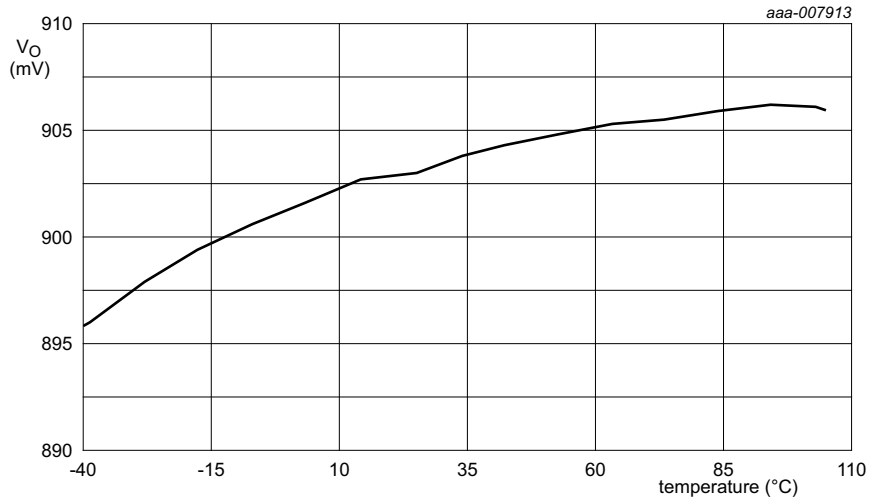


Fig 35. Typical internal voltage reference output voltage

13.3 Comparator

Table 22. Comparator characteristics

V_{DD} = 3.0 V and T_{amb} = 27 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin PIO0_6/VDDCMP configured for function VDDCMP		1.5	-	3.6	V
I_{DD}	supply current			-	55	-	µA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	1.9	-	mV
		V_{IC} = 1.5 V		-	2.1	-	mV
		V_{IC} = 2.8 V		-	2.0		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	µs

Table 24. Comparator voltage ladder reference static characteristics

V_{DD} = 3.3 V; T_{amb} = −40 °C to + 105 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal V_{DD} supply					
		decimal code = 00	[2]	-	0	0	%
		decimal code = 08		-	0	±0.4	%
		decimal code = 16		-	−0.2	±0.2	%
		decimal code = 24		-	−0.2	±0.2	%
		decimal code = 30		-	−0.1	±0.1	%
		decimal code = 31		-	−0.1	±0.1	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		-	0	0	%
		decimal code = 08		-	−0.1	±0.5	%
		decimal code = 16		-	−0.2	±0.4	%
		decimal code = 24		-	−0.2	±0.3	%
		decimal code = 30		-	−0.2	±0.2	%
		decimal code = 31		-	−0.1	±0.1	%

[1] Measured over a polyresistor matrix lot with a 2 kHz input signal and overdrive < 100 μV.

[2] All peripherals except comparator and IRC turned off.

R_S). Capacitance C_P in Figure 37 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

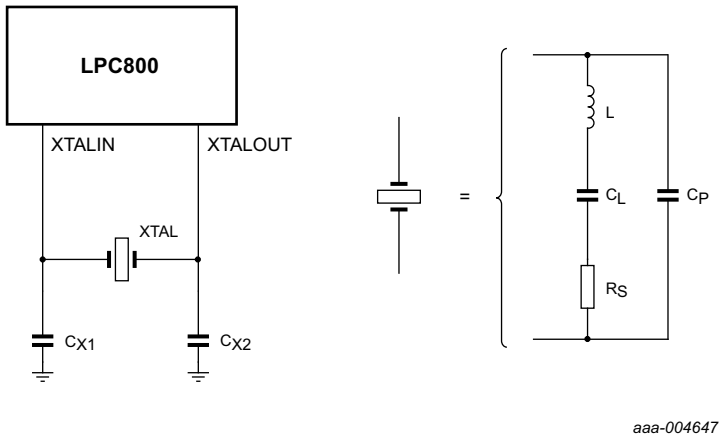


Fig 37. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

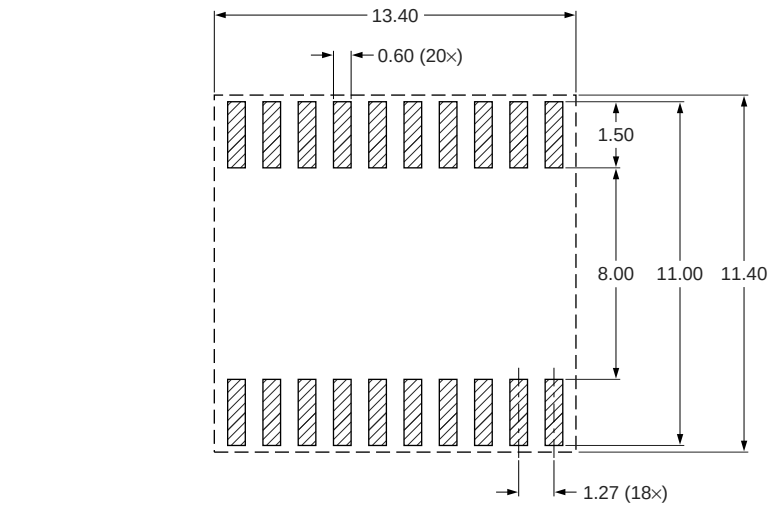


Fig 44. Reflow soldering of the SO20 package

19. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC81XM v.4.6	20180404	Product data sheet	201804004I	LPC81XM v.4.5
Modifications:	• Updated table note 2 of Section 12.1 “Power-up ramp conditions”.			
LPC81XM v.4.5	20160603	Product data sheet	-	LPC81XM v.4.4
Modifications:	• Added Section 12.1 “Power-up ramp conditions”. • Updated Figure 4 “Pin configuration SO20 package (LPC812M101JD20)”: Corrected function of pin 12 to ACMP_I2. • Updated the remark in Section 8.12 “USART0/1/2” to: USART2 is available on parts LPC812M101JTB16, LPC812M101JDH16, and LPC812M101JDH20 only.			
LPC81XM v.4.4	20150619	Product data sheet	-	LPC81XM v.4.3
Modifications:	• Section 14.4 “ElectroMagnetic Compatibility (EMC)” added.			
LPC81XM v.4.3	20140422	Product data sheet	-	LPC81XM v.4.2
Modifications:	• Section 8.20.2 “Clock input” updated for clarity. • CLKIN signal removed from Table 13 “Dynamic characteristic: external clock (XTALIN inputs)”. • Name “SCT” changed to “SCTimer/PWM” for clarity. • Remove slew rate control from GPIO features for clarity. • MRT bus stall mode added. • WWDT clock source corrected in Section 8.17.1. • Pin description table updated for clarification (I2C-bus pins, WAKEUP, $\overline{\text{RESET}}$). • Added reflow solder diagram and thermal resistance numbers for XSON16 (SOT1341-1). • Table 22: Added $V_{ref(cmp)}$ spec for PIO0_6/VDDCMP..			
LPC81XM v.4.2	20131210	Product data sheet	-	LPC81XM v.4.1
Modifications:	Corrected vertical axis marker in Figure 21 “CoreMark score”.			
LPC81XM v.4.1	20131112	Product data sheet	-	LPC81XM v.4
Modifications:	• Corrected XSON16 pin information in Figure 6 and Table 4.			
LPC81XM v.4	20131025	Product data sheet	-	LPC81XM v.3.1
Modifications:	• Added Section 14.1 “Typical wake-up times”. • Added LPC812M101JTB16 and XSON16 package.			
LPC81XM v.3.1	20130916	Product data sheet	-	LPC81XM v.3
Modifications:	• Correct the pin interrupt features: Pin interrupts can wake up the part from Sleep mode, Deep-sleep mode, and Power-down mode. See Section 8.11.1. • Table 9 “Static characteristics”: Updated power numbers for Deep-sleep, Power-down, and Deep power-down. • Added 30 MHz data to Figure 13 “Active mode: Typical supply current IDD versus supply voltage VDD”, Figure 14 “Active mode: Typical supply current IDD versus temperature”, and Figure 15 “Sleep mode: Typical supply current IDD versus temperature for different system clock frequencies”.			
LPC81XM v.3	20130729	Product data sheet	-	LPC81XM v.2.1

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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