Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101jdh20fp

5. Marking

The LPC81xM devices typically have the following top-side marking:

LPC81x

xxxxx

xxxxxxxx

xxYWWxR[x]

The last two letters in the last line (field ‘xR’) identify the boot code version and device revision.

Table 3. Device revision table

Revision identifier (xR)	Revision description
‘1A’	Initial device revision with boot code version 13.1
‘2A’	Device revision with boot code version 13.2
’4C’	Device revision with boot code version 13.4

Field ‘Y’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Remark: On the TSSOP16 package, the last line includes only the date code xxYWW.

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
SWDIO/PIO0_2/TMS	7	6	6	4	[2]	I/O	I; PU	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						I/O	-	**PIO0_2 —** General purpose digital input/output pin.
SWCLK/PIO0_3/ TCK	6	5	5	3	[2]	I/O	I; PU	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						I/O	-	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/WAKEUP/ TRST	5	4	4	2	[6]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. In ISP mode, this is the USART0 transmit pin U0_TXD. In boundary scan mode: TRST (Test Reset). This pin triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. This pin should be pulled HIGH externally before entering Deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit Deep power-down mode and wakes up the part.
RESET/PIO0_5	4	3	3	1	[4]	I/O	I; PU	**RESET —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO or for any movable function if an external RESET function is not needed and the Deep power-down mode is not used.
						I	-	**PIO0_5 —** General purpose digital input/output pin.
PIO0_6/VDDCMP	18	15	15	-	[9]	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
						AI	-	**VDDCMP —** Alternate reference voltage for the analog comparator.
PIO0_7	17	14	14	-	[2]	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin.
PIO0_8/XTALIN	14	11	11	-	[8]	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
						I	-	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	10	10	-	[8]	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
						O	-	**XTALOUT —** Output from the oscillator circuit.
PIO0_10	9	8	8	-	[3]	I	IA	**PIO0_10 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_11	8	7	7	-	[3]	I	IA	**PIO0_11 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.

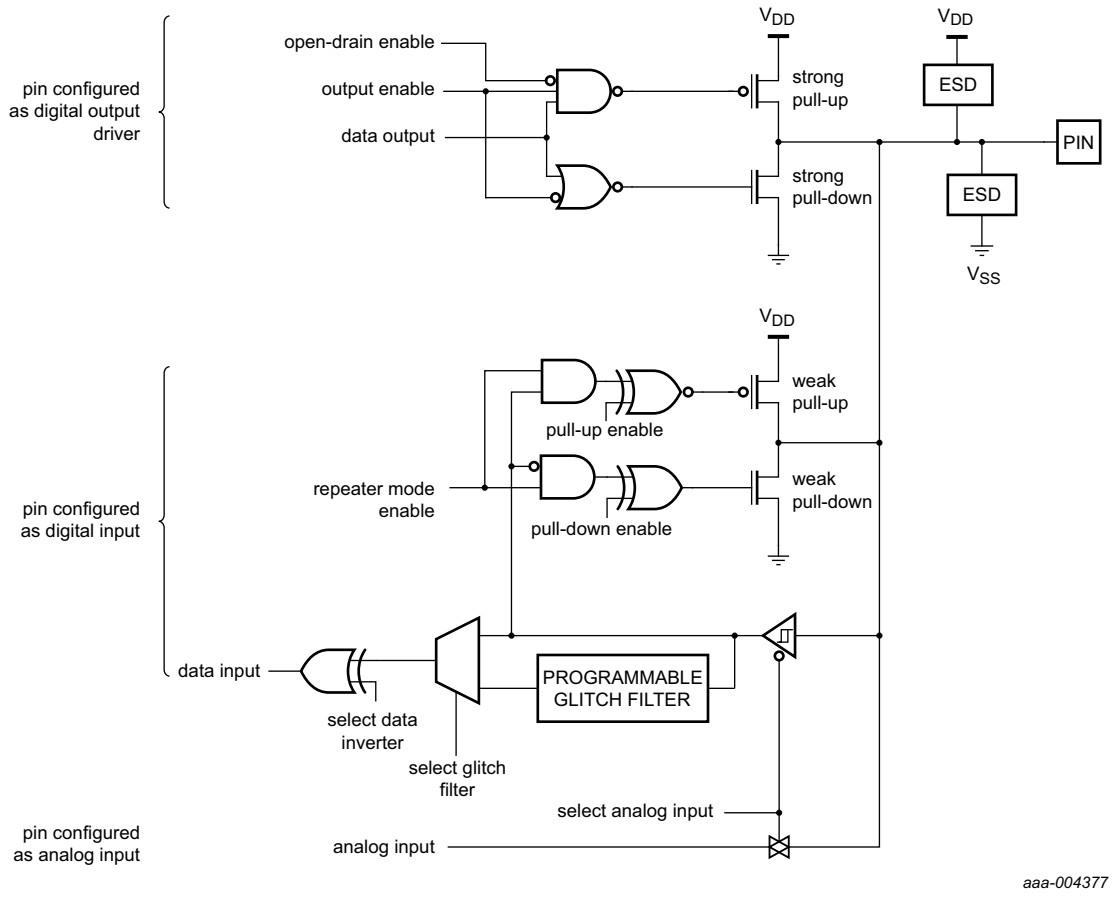


Fig 8. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 4. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 8).
-

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.

- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.14 I2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain PIO0_10 and PIO0_11 provide the electrical characteristics to support the full I2C-bus specification (see Ref. 1).

8.14.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Supported by on-chip ROM API.
- If the I2C functions are connected to the true open-drain pins (PIO0_10 and PIO0_11), the I2C supports the full I2C-bus specification:
  - Fail-safe operation: When the power to an I^2C-bus device is switched off, the SDA and SCL pins connected to the I^2C-bus are floating and do not disturb the bus.
  - Supports Fast-mode Plus with bit rates up to 1 Mbit/s.

8.15 State-Configurable Timer/PWM (SCTimer/PWM)

The state configurable timer (SCTimer/PWM or SCT) can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to two different programmable states, which can change under the control of events, to provide complex timing patterns.

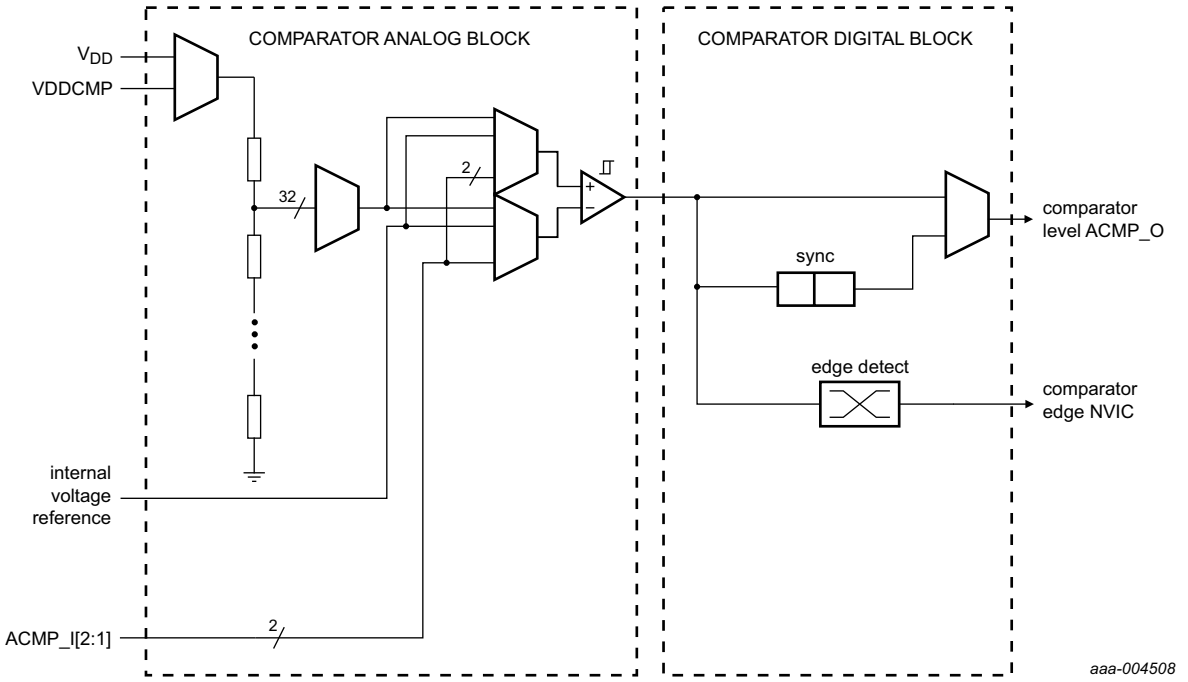


Fig 9. Comparator block diagram

8.19.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or VDDCMP on pin PIO0_6); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- The comparator output can be routed internally to the SCT input through the switch matrix.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.20.6.3 Deep-sleep mode

In Deep-sleep mode, the LPC81xM is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC and watchdog oscillator or low-power oscillator if selected. The IRC output is disabled. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC81xM can wake up from Deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from Deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

8.20.6.4 Power-down mode

In Power-down mode, the LPC81xM is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator or low-power oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC81xM can wake up from Power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from Power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.20.6.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the self wake-up timer if enabled. Four general-purpose registers are available to store information during Deep power-down mode. The LPC81xM can wake up from Deep power-down mode via the WAKEUP pin, or without an external signal by using the time-out of the self wake-up timer (see Section 8.18).

The LPC81xM can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V	[3]	−0.5	+5.5	V
		5 V tolerant open-drain pins PIO0_10 and PIO0_11	[4]	−0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	[5]	−0.5	+3.6	V
V_{IA}	analog input voltage		[6] [7]	−0.5	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[8]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[9]	-	5500	V
		charged device model; TSSOP20 and SOP20 packages		-	1200	V
		charged device model; TSSOP16 package		-	1000	V
		charged device model; XSON16 package		-	800	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 9.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 9) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Including voltage on outputs in tri-state mode. Does not apply to pin PIO0_6.

[4] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] V_{DD} present or not present.

[6] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[8] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[9] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 8. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
DIP8				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	60 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	81 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		38 ± 15 %	°C/W
TSSOP16				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	133 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	182 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		33 ± 15 %	°C/W
TSSOP20				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	110 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	153 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		23 ± 15 %	°C/W
SO20				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	87 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	112 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		50 ± 15 %	°C/W
XSON16				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	92 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	180 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		27 ± 15 %	°C/W

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Oscillator input pins (PIO0_8 and PIO0_9)							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[3] IRC enabled; system oscillator disabled; system PLL disabled.

[4] BOD disabled.

[5] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[6] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[7] IRC enabled; system oscillator disabled; system PLL enabled.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[10] WAKEUP pin pulled HIGH externally.

[11] Including voltage on outputs in tri-state mode.

[12] 3-state outputs go into tri-state mode in Deep power-down mode.

[13] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[14] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 8.

[15] To V_{SS}.

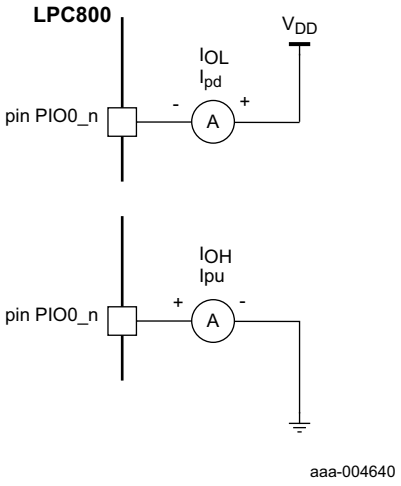
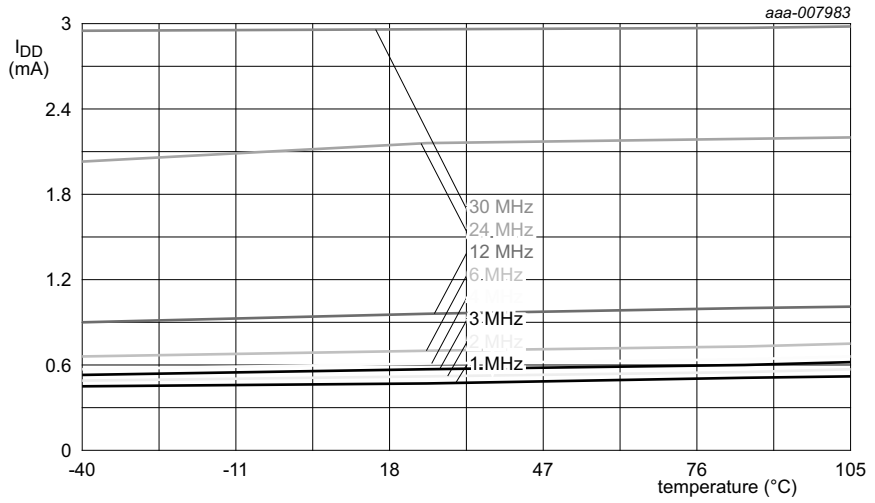


Fig 13. Pin input/output current measurement



Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: IRC disabled; SYSOSC enabled; PLL enabled.

Fig 15. Active mode: Typical supply current I_{DD} versus temperature

12. Dynamic characteristics

12.1 Power-up ramp conditions

Table 11. Power-up characteristics

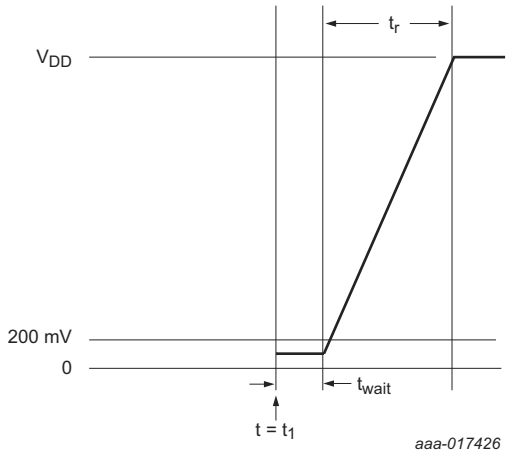
T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 200 mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2][3]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	200	mV

[1] See Figure 28.

[2] The wait time specifies the time the power supply must be at levels below 200 mV before ramping up. See the LPC81x errata sheet.

[3] Based on characterization, not tested in production.



Condition: 0 < V_I ≤ 200 mV at start of power-up (t = t_1)

Fig 28. Power-up ramp

12.2 Flash memory

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ret}	retention time	powered		10	20	-	years
		unpowered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. $T_{amb} \leq +85$ °C. Flash programming with IAP calls (see *LPC800 user manual*).

12.3 External clock for the oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.95 V (see Table 9). For connecting the oscillator to the XTAL pins, also see Section 14.2.

Table 13. Dynamic characteristic: external clock (XTALIN inputs)

T_{amb} = −40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

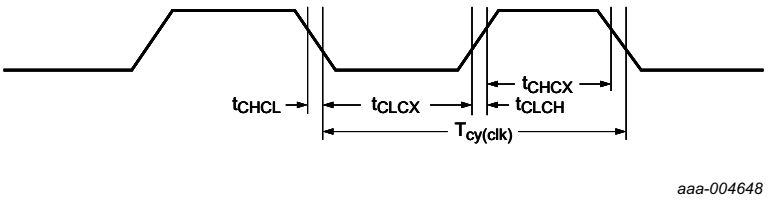


Fig 29. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.5 I/O pins

Table 16. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.6 I²C-bus

Table 17. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

R_S). Capacitance C_P in Figure 37 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

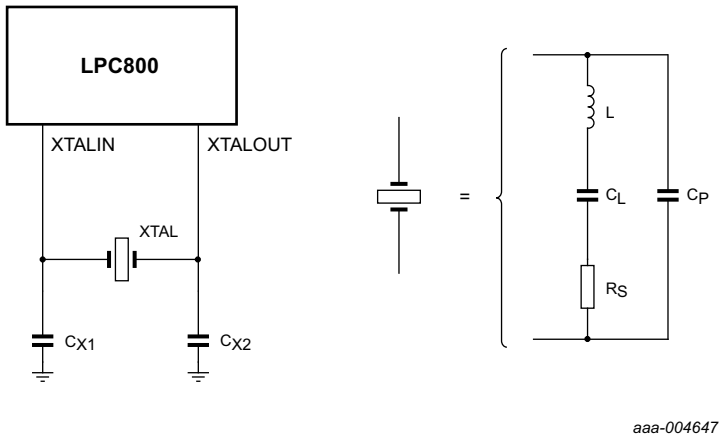


Fig 37. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.3 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

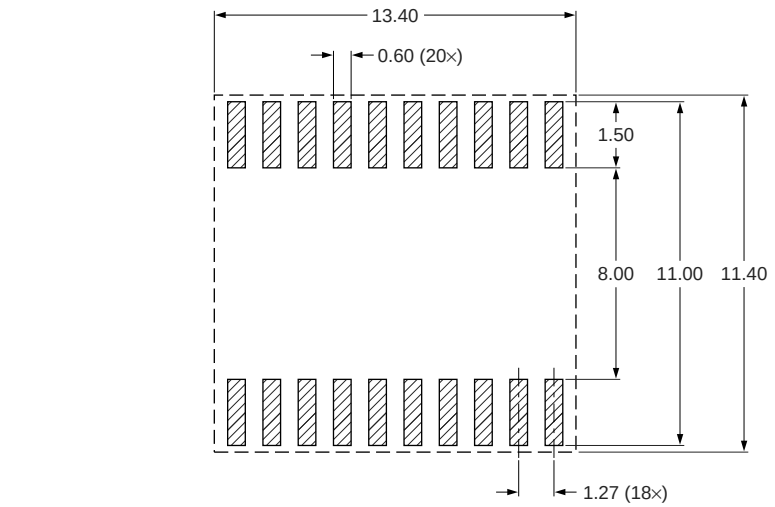


Fig 44. Reflow soldering of the SO20 package

17. Abbreviations

Table 29. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] I2C-bus specification *UM10204*.

Table 30. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Operating temperature range changed to −40 °C to 105 °C. • Type numbers updated to reflect the new operating temperature range. See Table 1 “Ordering information” and Table 2 “Ordering options”. • ISP entry pin moved from PIO0_1 to PIO0_12 for TSSOP, and SSOP packages. See Table 4 and Table 6. • Propagation delay values updated in Table 21 “Comparator characteristics”. • SPI characteristics updated. See Section 12.6. • IRC characteristics updated. See Section 12.3. • CoreMark data updated. See Figure 19 and Figure 20. • IRC frequency changed to 12 MHz +/- 1.5 %. See Table 13. • Data sheet status updated to Product data sheet.			
LPC81XM v.2.1	20130325	Preliminary data sheet	-	LPC81XM v.2
	• Editorial updates (temperature sensor removed). • CoreMark data added. See Figure 19 “Active mode: CoreMark power consumption IDD” and Figure 20 “CoreMark score”. • I_{DD} in Deep power-down mode added for condition Low-power oscillator on/WKT wake-up enabled. See Table 10. • Table note 3 updated for Table 4 “Pin description table (fixed pins)”. • Conditions for t_{er} and t_{prog} updated in Table 12 “Flash characteristics”. • Section 13.3 “Internal voltage reference” added. • Typical timing data added for SPI. See Section 12.6. • Typical timing data added for USART in synchronous mode. See Section 12.7. • BOD characterization added. See Section 13.1. • IRC characterization added. See Section 12.3. • Internal voltage reference characteristics added. See Section 13.3. • Data sheet status changed to Preliminary data sheet.			
LPC81XM v.2	20130128	Objective data sheet	-	LPC81XM v.1
Modifications:	• MTB memory space changed to 1 kB in Figure 6. • Electrical pin characteristics added in Table 10. • Figure 11 “Connecting the SWD pins to a standard SWD connector” added. • Peripheral power consumption added in Table 11. • Table 7 updated. • MRT implementation changed to 31-bit timer. • Power consumption data in active and sleep mode with IRC added. See Figure 13 to Figure 15. • Power consumption (parameter I_{DD}) in active and sleep mode for low-power mode at 12 MHz corrected in Table 10. • Power consumption (parameter I_{DD}) in active and sleep mode at 24 MHz added in Table 10. • Maximum USART speed in synchronous mode changed to 10 Mbit/s. • Section 5 “Marking” added.			
LPC81XM v.1	20121112	Objective data sheet	-	-

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

21. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**