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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101jdh20j

- State Configurable Timer/PWM (SCTimer/PWM) with input and output functions (including capture and match) assigned to pins through the switch matrix.
- Multiple-channel multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Self Wake-up Timer (WKT) clocked from either the IRC or a low-power, low-frequency internal oscillator.
- CRC engine.
- Windowed Watchdog timer (WWDT).

- Analog peripherals:
  - Comparator with internal and external voltage references with pin functions assigned or enabled through the switch matrix.
- Serial interfaces:
  - Three USART interfaces with pin functions assigned through the switch matrix.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - One I^2C-bus interface with pin functions assigned through the switch matrix.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1.5 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - 10 kHz low-power oscillator for the WKT.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input CLKIN, or the internal RC oscillator.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from Deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect.
- Unique device serial number for identification.
- Single power supply.
- Operating temperature range −40 °C to 105 °C except for the DIP8 package, which is available for a temperature range of −40 °C to 85 °C.
- Available as DIP8, TSSOP16, SO20, TSSOP20, and XSON16 package.

3. Applications

- 8/16-bit applications
- Consumer
- Climate control
- Lighting
- Motor control
- Fire and security applications

6. Block diagram

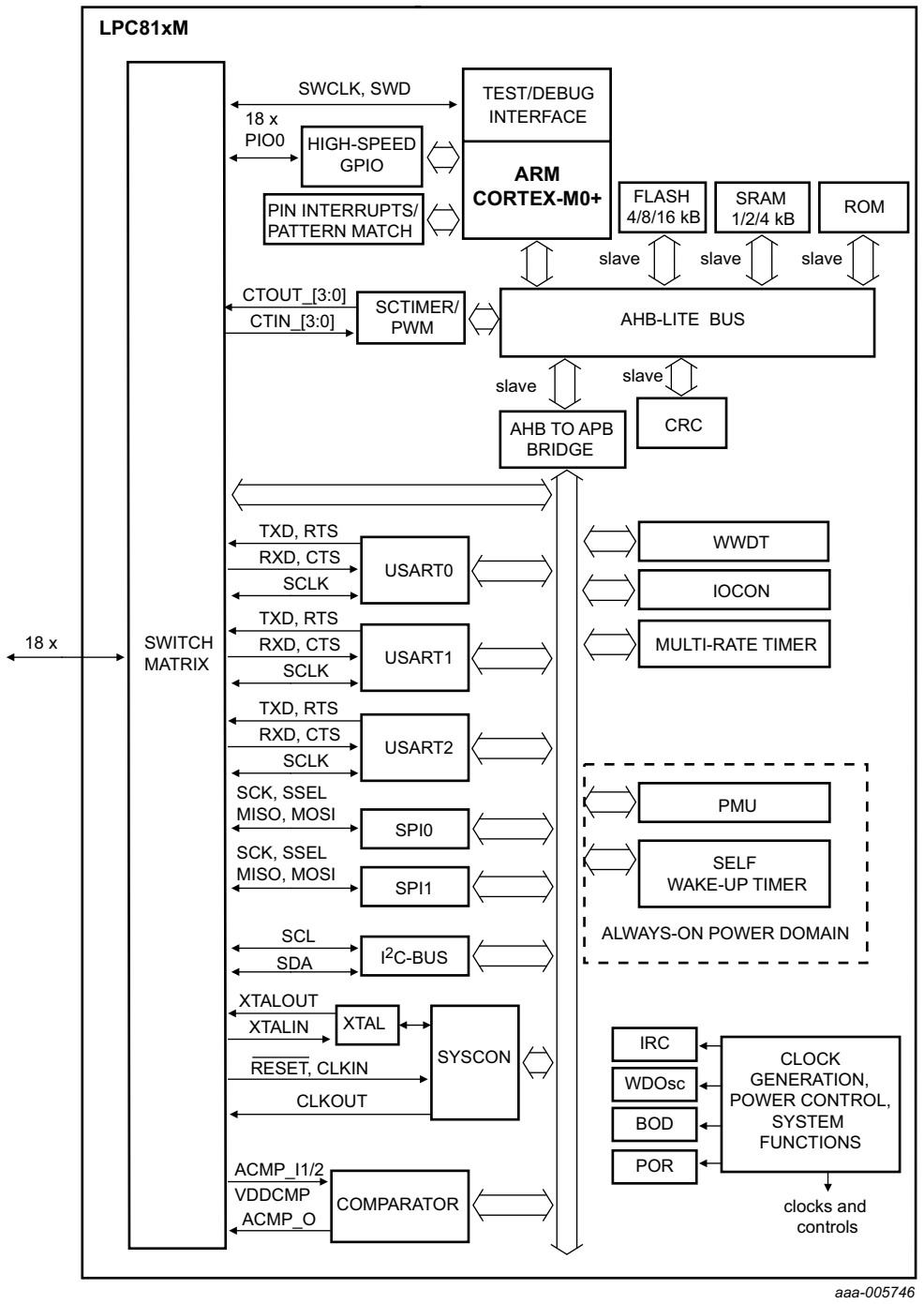


Fig 1. LPC81xM block diagram

7.2 Pin description

The pin description consists of two parts showing pin functions that are fixed to a certain package pin (see Table 4) and showing pin functions that can be assigned to any pin on the package through the switch matrix (see Table 5).

The pin description table in Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable between GPIO and the comparator inputs, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Table 5 shows the the I2C, USART, SPI, and SCT pin functions, which can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

For full I2C-bus compatibility, assign the I2C functions to the open-drain pins PIO0_11 and PIO0_10.

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_0/ACMP_I1/ TDO	19	16	16	8	[5]	I/O	I; PU	**PIO0_0 —** General purpose digital input/output port 0 pin 0. In ISP mode, this is the USART0 receive pin U0_RXD. In boundary scan mode: TDO (Test Data Out).
						AI	-	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	12	9	9	5	[5]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). ISP entry pin on chip versions 1A and 2A and on the DIP8 package (see Table 6). For these chip versions and packages, a LOW level on this pin during reset starts the ISP command handler. See PIO0_12 for all other packages.
						AI	-	**ACMP_I2 —** Analog comparator input 2.
						I	-	**CLKIN —** External clock input.

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
SWDIO/PIO0_2/TMS	7	6	6	4	[2]	I/O	I; PU	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						I/O	-	**PIO0_2 —** General purpose digital input/output pin.
SWCLK/PIO0_3/ TCK	6	5	5	3	[2]	I/O	I; PU	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						I/O	-	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/WAKEUP/ TRST	5	4	4	2	[6]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. In ISP mode, this is the USART0 transmit pin U0_TXD. In boundary scan mode: TRST (Test Reset). This pin triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. This pin should be pulled HIGH externally before entering Deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit Deep power-down mode and wakes up the part.
RESET/PIO0_5	4	3	3	1	[4]	I/O	I; PU	**RESET —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO or for any movable function if an external RESET function is not needed and the Deep power-down mode is not used.
						I	-	**PIO0_5 —** General purpose digital input/output pin.
PIO0_6/VDDCMP	18	15	15	-	[9]	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
						AI	-	**VDDCMP —** Alternate reference voltage for the analog comparator.
PIO0_7	17	14	14	-	[2]	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin.
PIO0_8/XTALIN	14	11	11	-	[8]	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
						I	-	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	10	10	-	[8]	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
						O	-	**XTALOUT —** Output from the oscillator circuit.
PIO0_10	9	8	8	-	[3]	I	IA	**PIO0_10 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_11	8	7	7	-	[3]	I	IA	**PIO0_11 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.

Table 6. Pin location in ISP mode

ISP entry pin	USART RXD	USART TXD	Marking	Boot loader version	Package
PIO0_1	PIO0_0	PIO0_4	1A	v 13.1	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	2A	v 13.2	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	4C and later	v 13.4 and later	DIP8
PIO0_12	PIO0_0	PIO0_4	4C and later	v 13.4 and later	TSSOP20; SO20; TSSOP16; XSON16

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC81xM contain a total of up to 4 kB on-chip static RAM data memory.

8.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I^2C-bus driver API routines

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Relocatable interrupt vector table using vector table offset register.

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

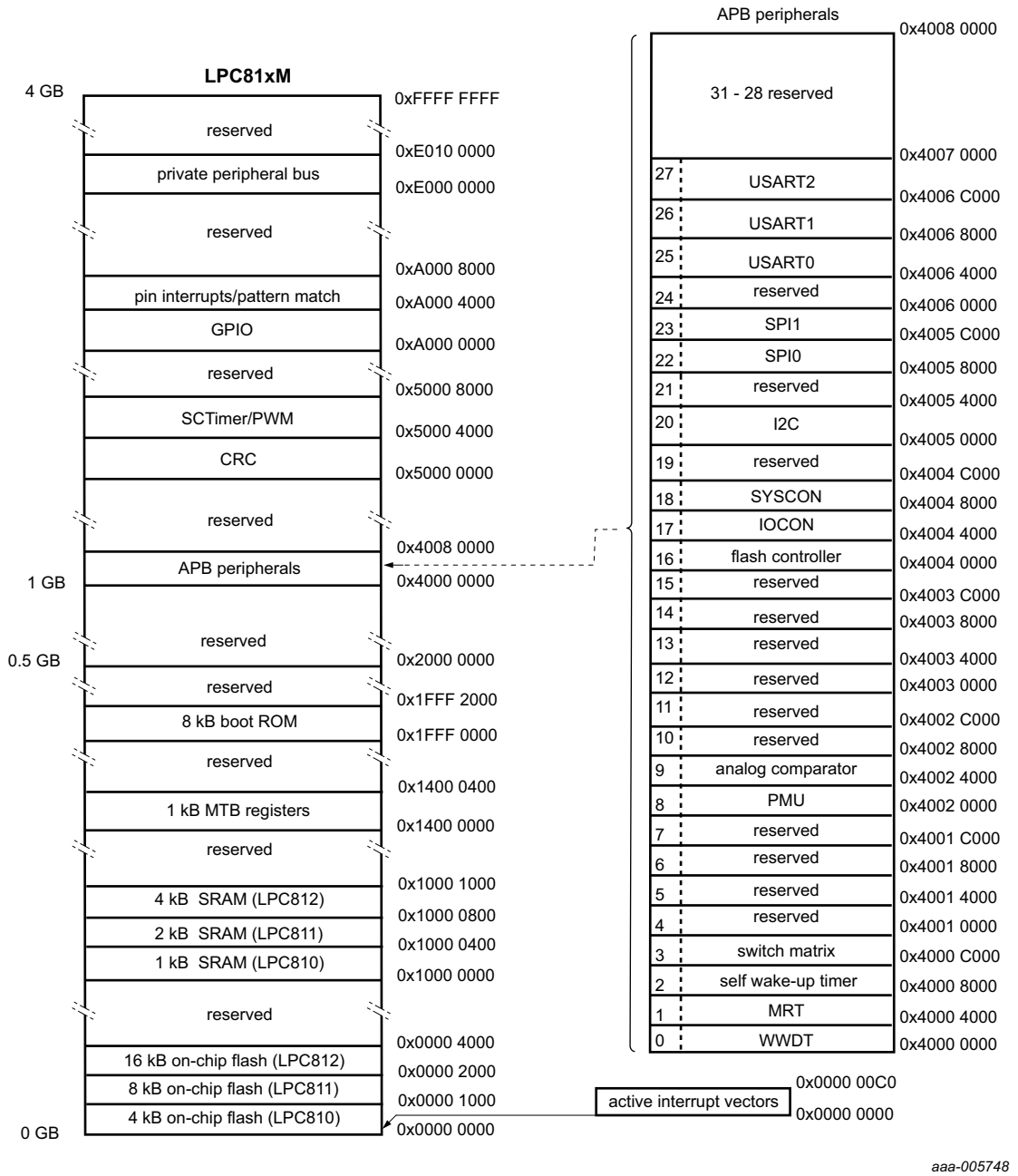


Fig 7. LPC81xM Memory map

8.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. This pin is not 5 V tolerant when V_{DD} = 0.

– The pattern match engine does not facilitate wake-up.

8.12 USART0/1/2

Remark: USART0 and USART1 are available on all LPC800 parts. USART2 is available on parts LPC812M101JTB16, LPC812M101JDH16, and LPC812M101JDH20 only.

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.12.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except PIO0_10 and PIO0_11.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Supported by on-chip ROM API.

8.13 SPI0/1

Remark: SPI0 is available on all LPC800 parts. SPI1 is available on parts LPC812M101JDH16 and LPC812M101JDH20 only.

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.13.1 Features

- Maximum data rates of 30 Mbit/s in master mode and 25 Mbit/s in slave mode for SPI functions connected to all digital pins except PIO0_10 and PIO0_11.

8.20 Clocking and power control

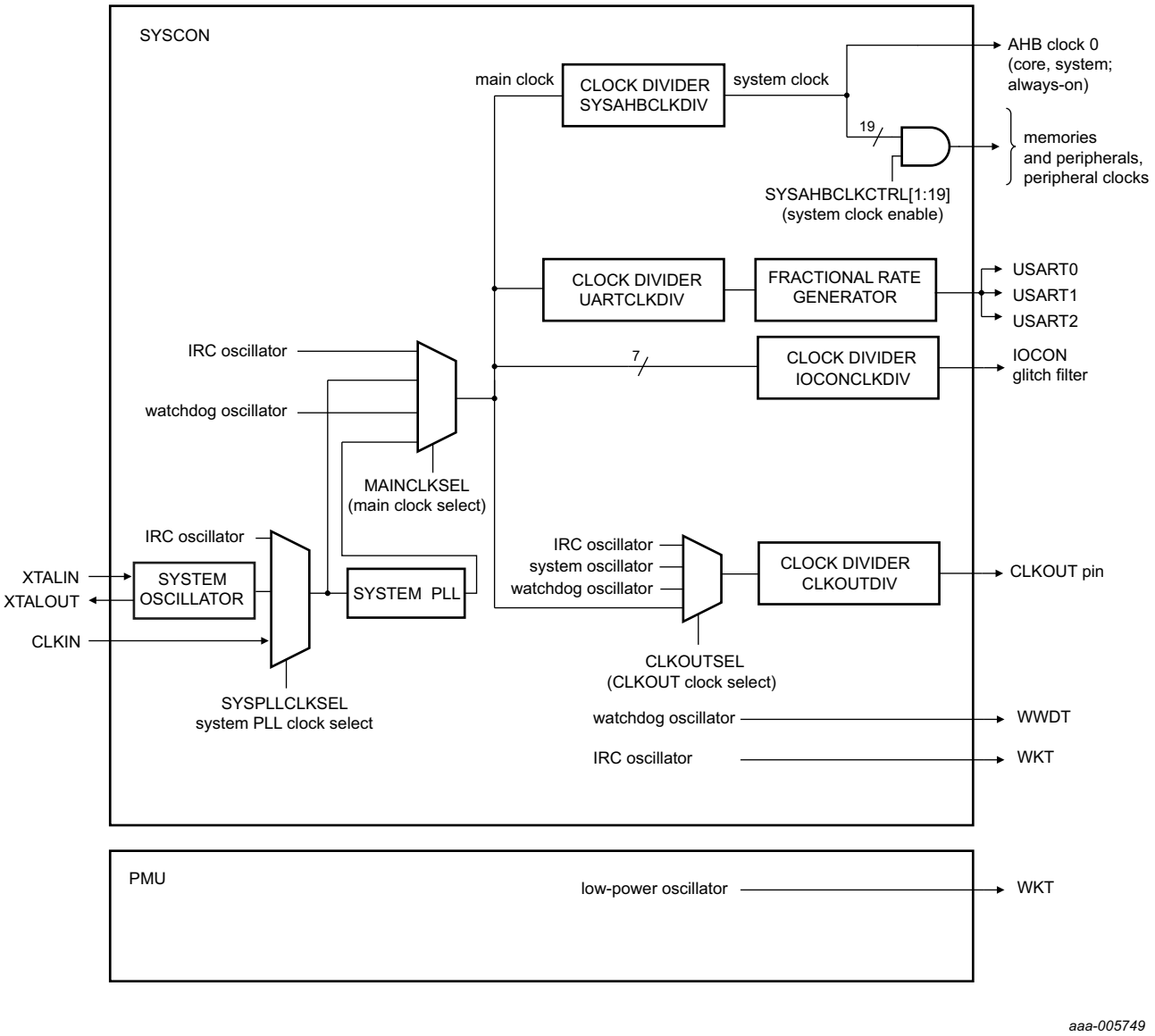


Fig 10. LPC81xM clock generation

8.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

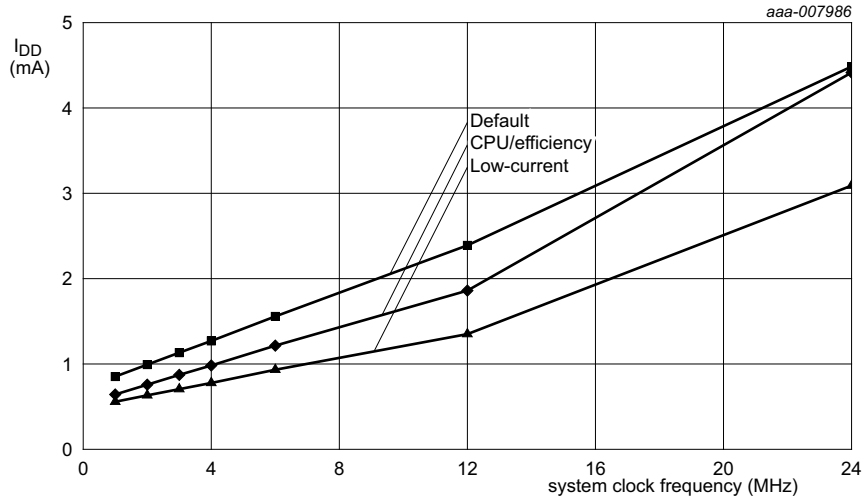
1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

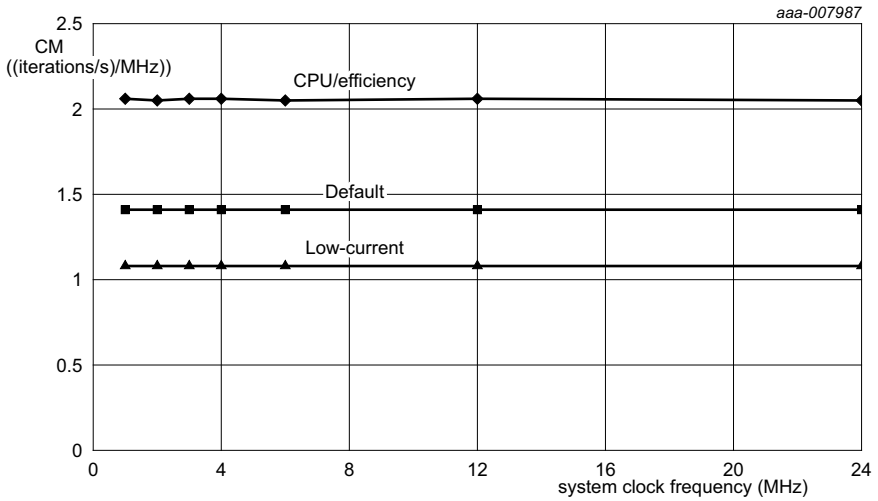
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, $\overline{\text{RESET}}$; see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_6	[11] [12]	0	-	5.0	V
		$V_{DD} \geq$ 1.8 V; on 3 V tolerant pin PIO0_6		0	-	3.6	
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = 4 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = 3 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[13]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		15	50	85	μA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	μA
		$V_{DD} < V_I$ < 5 V		0	0	0	μA
High-drive output pins configured as digital pins (PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13); see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA

11.2 CoreMark data



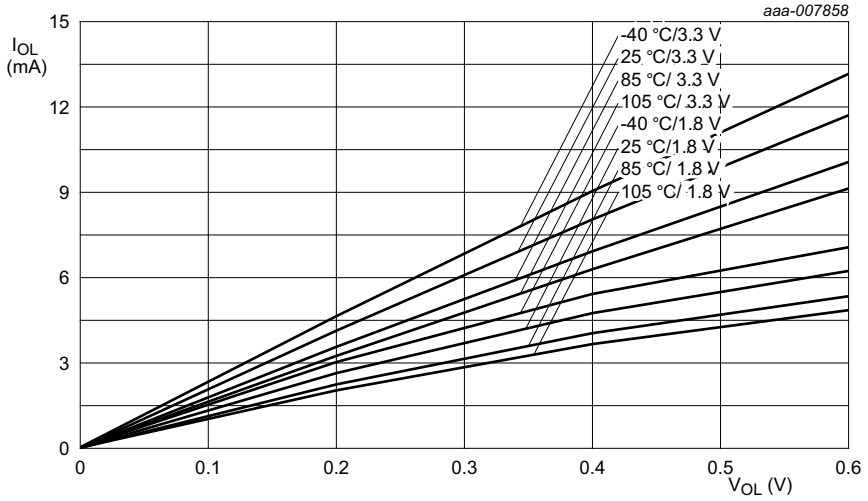
Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; system clock derived from the IRC; system oscillator disabled; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.7.

Fig 20. Active mode: CoreMark power consumption I_{DD}



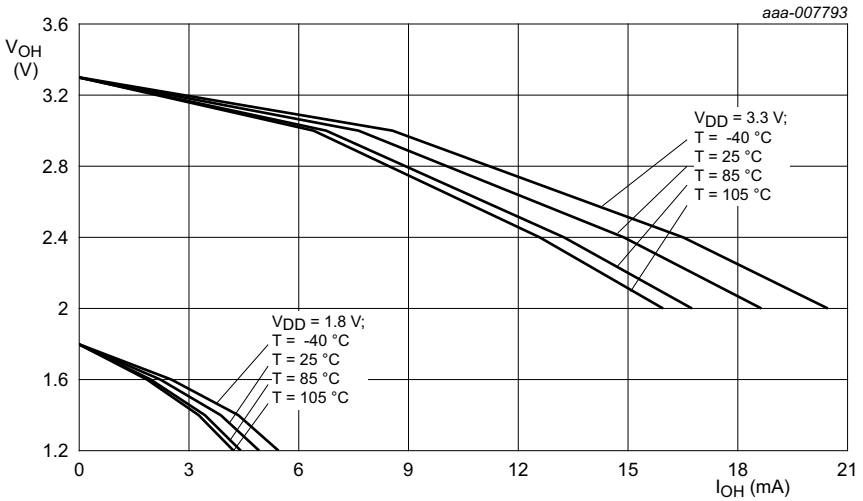
Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.7.

Fig 21. CoreMark score



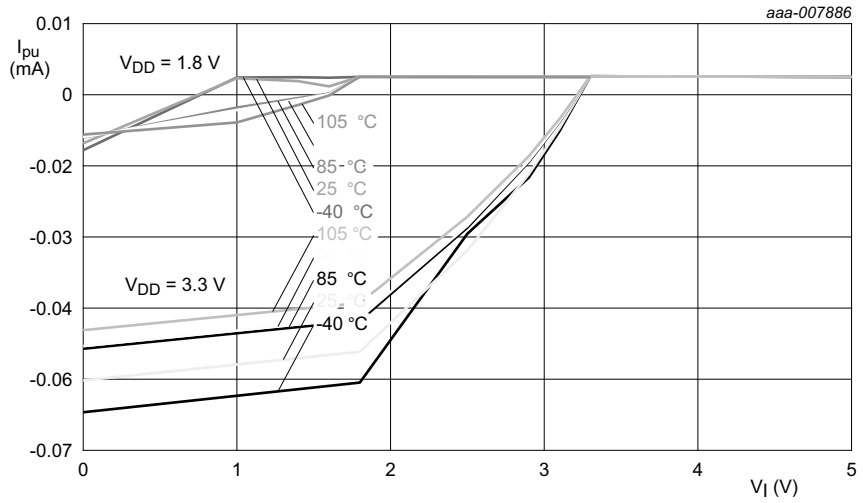
Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins and high-drive pins PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13.

Fig 24. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



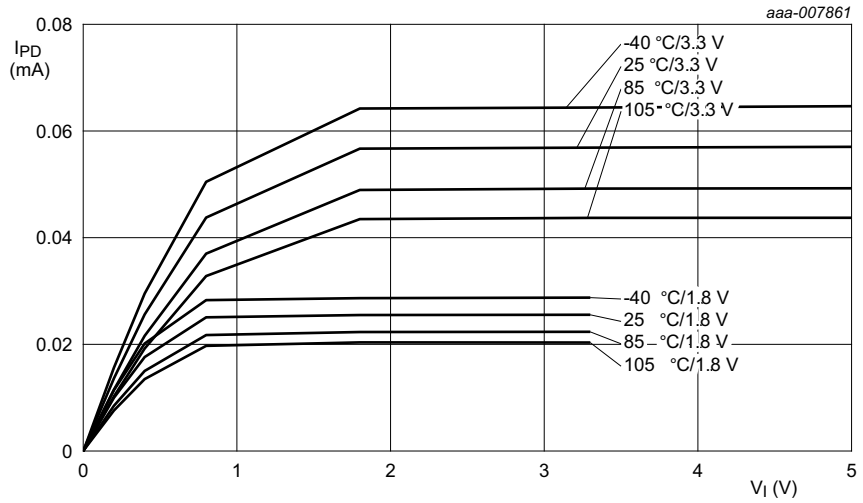
Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 25. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 26. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 27. Typical pull-down current I_{pd} versus input voltage V_I

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

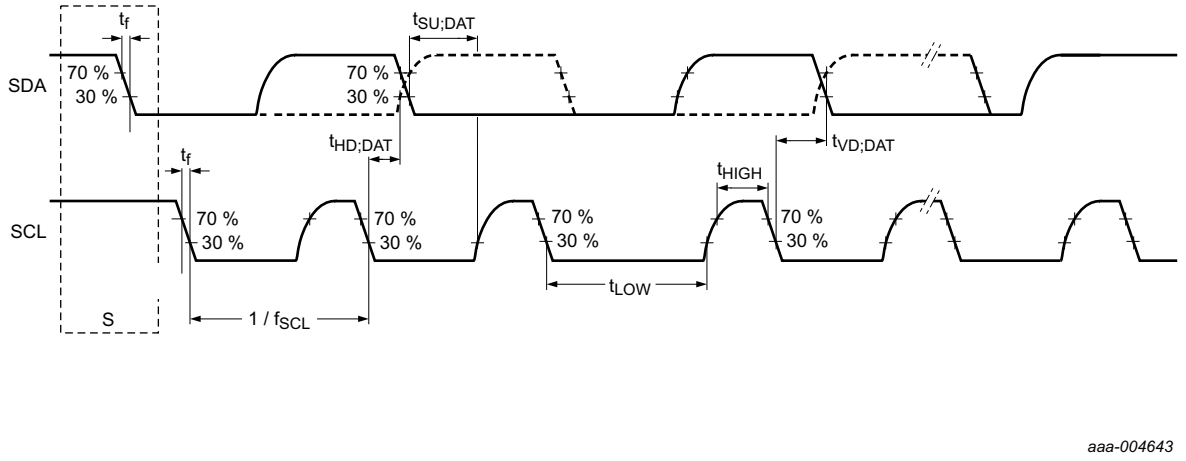


Fig 31. I^2C-bus pins clock timing

12.7 SPI interfaces

The maximum data bit rate is 30 Mbit/s in master mode and 25 Mbit/s in slave mode.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

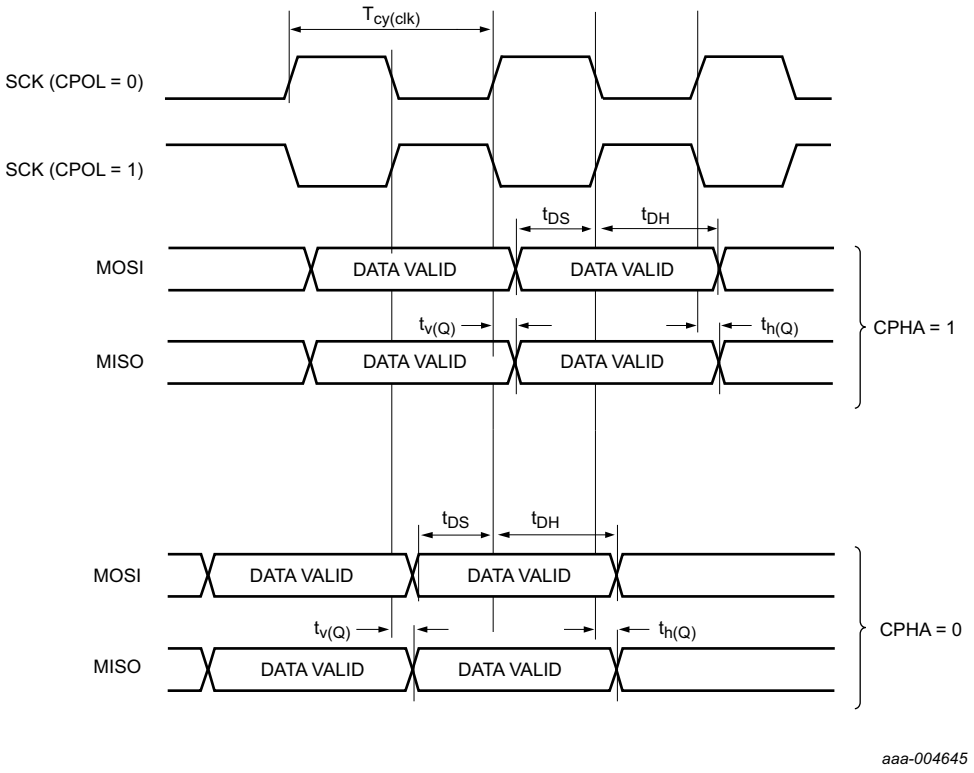
Table 18. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V. Simulated parameters sampled at the 50 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master[1]						
$T_{cy(clk)}$	clock cycle time		[2]	33	-	ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	0.5	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		0.5	-	ns
SPI slave						
$T_{cy(clk)}$				40		ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	10	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		10	-	ns

[1] Capacitance on pin SPIn_SCK C_{SCK} < 5 pF.

[2] $T_{cy(clk)}$ = DIVVAL/CCLK with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the *LPC800 User manual UM10601*.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 33. SPI slave timing

Table 22. Comparator characteristics *…continued*

V_{DD} = 3.0 V and T_{amb} = 27 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	109	121	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	155	164	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	95	105	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	101	108	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	122	129	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	74	82	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	246	260	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	57	59	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	218		ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	146	155	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	184	206	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	250	286	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2]	-	6, 11, 21	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2][2]	-	4, 9, 19	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = −40 °C to +105 °C. Typical data are for T_{amb} = 27 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable to three levels.

Table 23. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 105 °C; slow process models).

[2] Settling time applies to switching between comparator channels.

Footprint information for reflow soldering of XSON16 package **SOT1341-1**

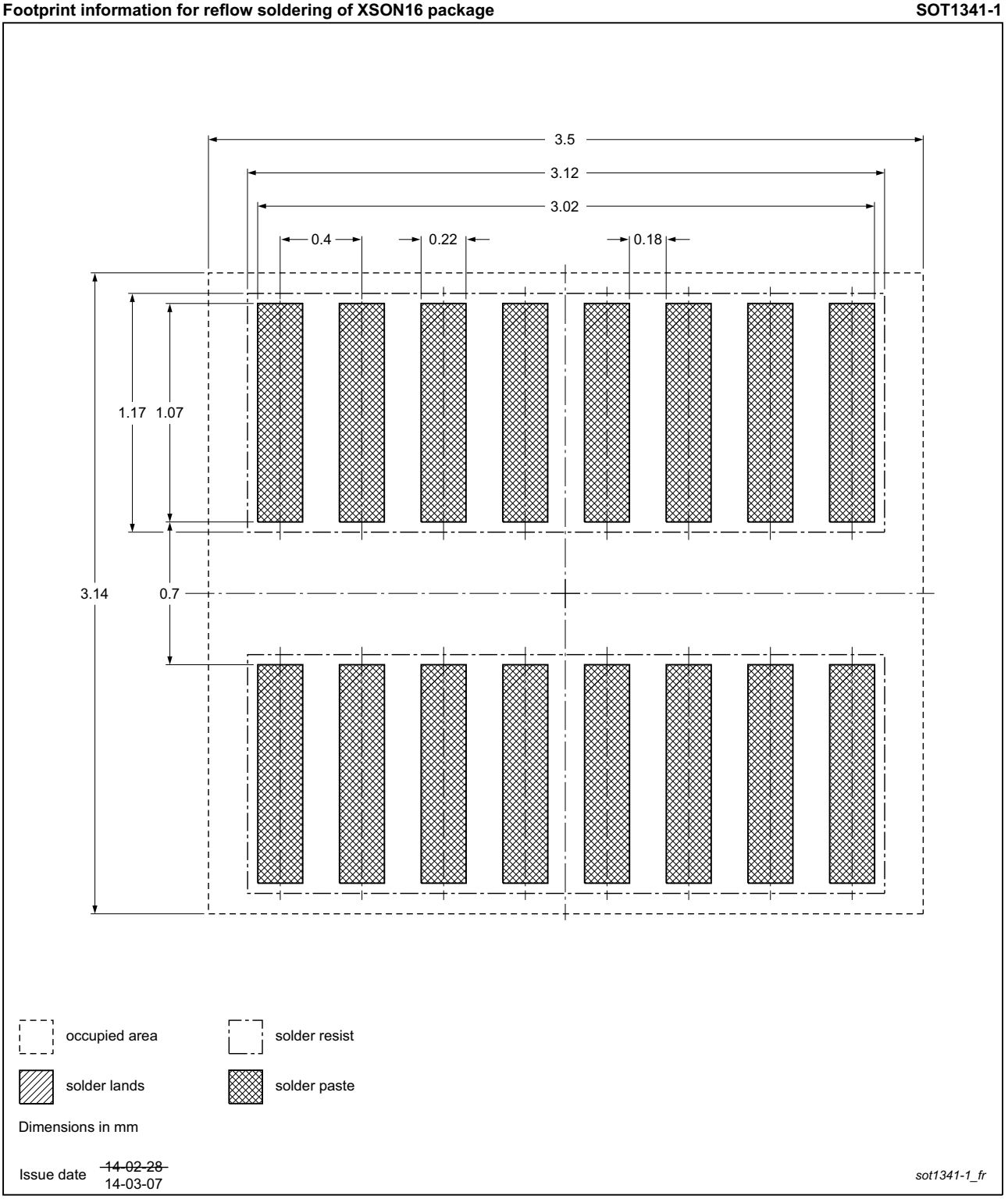


Fig 46. Reflow soldering of the XSON16 package

Table 30. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Operating temperature range changed to −40 °C to 105 °C. • Type numbers updated to reflect the new operating temperature range. See Table 1 “Ordering information” and Table 2 “Ordering options”. • ISP entry pin moved from PIO0_1 to PIO0_12 for TSSOP, and SSOP packages. See Table 4 and Table 6. • Propagation delay values updated in Table 21 “Comparator characteristics”. • SPI characteristics updated. See Section 12.6. • IRC characteristics updated. See Section 12.3. • CoreMark data updated. See Figure 19 and Figure 20. • IRC frequency changed to 12 MHz +/- 1.5 %. See Table 13. • Data sheet status updated to Product data sheet.			
LPC81XM v.2.1	20130325	Preliminary data sheet	-	LPC81XM v.2
	• Editorial updates (temperature sensor removed). • CoreMark data added. See Figure 19 “Active mode: CoreMark power consumption IDD” and Figure 20 “CoreMark score”. • I_{DD} in Deep power-down mode added for condition Low-power oscillator on/WKT wake-up enabled. See Table 10. • Table note 3 updated for Table 4 “Pin description table (fixed pins)”. • Conditions for t_{er} and t_{prog} updated in Table 12 “Flash characteristics”. • Section 13.3 “Internal voltage reference” added. • Typical timing data added for SPI. See Section 12.6. • Typical timing data added for USART in synchronous mode. See Section 12.7. • BOD characterization added. See Section 13.1. • IRC characterization added. See Section 12.3. • Internal voltage reference characteristics added. See Section 13.3. • Data sheet status changed to Preliminary data sheet.			
LPC81XM v.2	20130128	Objective data sheet	-	LPC81XM v.1
Modifications:	• MTB memory space changed to 1 kB in Figure 6. • Electrical pin characteristics added in Table 10. • Figure 11 “Connecting the SWD pins to a standard SWD connector” added. • Peripheral power consumption added in Table 11. • Table 7 updated. • MRT implementation changed to 31-bit timer. • Power consumption data in active and sleep mode with IRC added. See Figure 13 to Figure 15. • Power consumption (parameter I_{DD}) in active and sleep mode for low-power mode at 12 MHz corrected in Table 10. • Power consumption (parameter I_{DD}) in active and sleep mode at 24 MHz added in Table 10. • Maximum USART speed in synchronous mode changed to 10 Mbit/s. • Section 5 “Marking” added.			
LPC81XM v.1	20121112	Objective data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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