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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-XFDFN
Supplier Device Package	16-XSON (3.2x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101jtb16x

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC810M021FN8	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT097-2
LPC811M001JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JD20	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC812M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC812M101JTB16	XSON16	plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 × 3.2 × 0.5 mm	SOT1341-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/kB	SRAM/kB	USART	I^2C-bus	SPI	Comparator	GPIO	Package
LPC810M021FN8	4	1	2	1	1	1	6	DIP8
LPC811M001JDH16	8	2	2	1	1	1	14	TSSOP16
LPC812M101JDH16	16	4	3	1	2	1	14	TSSOP16
LPC812M101JD20	16	4	2	1	1	1	18	SO20
LPC812M101JDH20	16	4	3	1	2	1	18	TSSOP20
LPC812M101JTB16	16	4	3	1	2	1	14	XSON16

6. Block diagram

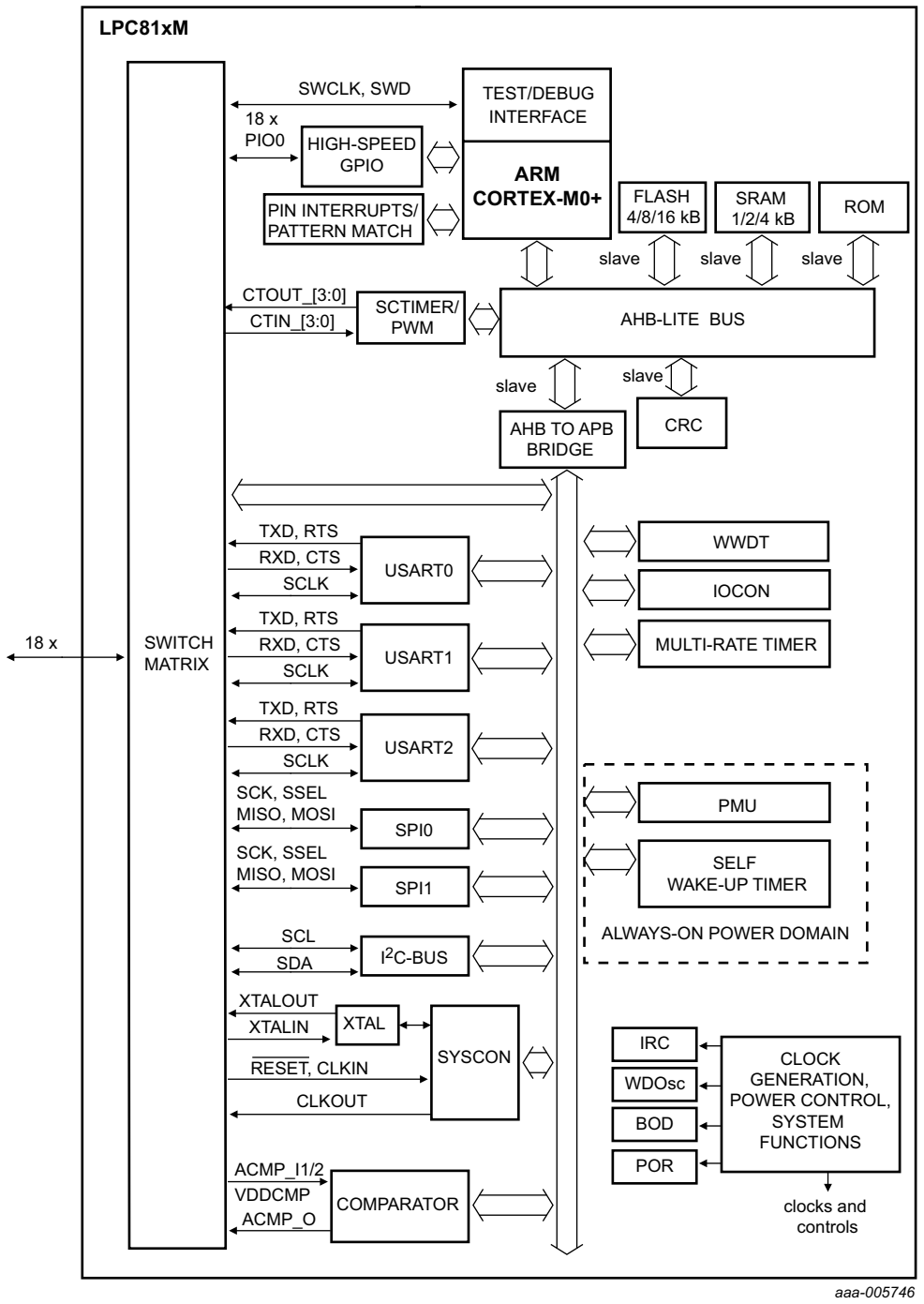


Fig 1. LPC81xM block diagram

7.2 Pin description

The pin description consists of two parts showing pin functions that are fixed to a certain package pin (see Table 4) and showing pin functions that can be assigned to any pin on the package through the switch matrix (see Table 5).

The pin description table in Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable between GPIO and the comparator inputs, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Table 5 shows the the I2C, USART, SPI, and SCT pin functions, which can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

For full I2C-bus compatibility, assign the I2C functions to the open-drain pins PIO0_11 and PIO0_10.

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_0/ACMP_I1/ TDO	19	16	16	8	[5]	I/O	I; PU	**PIO0_0 —** General purpose digital input/output port 0 pin 0. In ISP mode, this is the USART0 receive pin U0_RXD. In boundary scan mode: TDO (Test Data Out).
						AI	-	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	12	9	9	5	[5]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). ISP entry pin on chip versions 1A and 2A and on the DIP8 package (see Table 6). For these chip versions and packages, a LOW level on this pin during reset starts the ISP command handler. See PIO0_12 for all other packages.
						AI	-	**ACMP_I2 —** Analog comparator input 2.
						I	-	**CLKIN —** External clock input.

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_12	3	2	2	-	[2]	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin. ISP entry pin on the SO20/TSSOP20/TSSOP16/XSON16 packages starting with chip version 4C (see Table 6). A LOW level on this pin during reset starts the ISP command handler. See pin PIO0_1 for the DIP8 package and chip versions 1A and 2A.
PIO0_13	2	1	1	-	[2]	I/O	I; PU	**PIO0_13 —** General purpose digital input/output pin.
PIO0_14	20	-	-	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin.
PIO0_15	11	-	-	-	[7]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin.
PIO0_16	10	-	-	-	[7]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin.
PIO0_17	1	-	-	-	[7]	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin.
V_{DD}	15	12	12	6		-	-	3.3 V supply voltage.
V_{SS}	16	13	13	7		-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[3] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

Remark: If this pin is not available on the package, prevent it from internally floating as follows: Set bits 10 and 11 in the GPIO DIR0 register to 1 to enable the output driver and write 1 to bits 10 and 11 in the GPIO CLR0 register to drive the outputs LOW internally.

[4] See Figure 11 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[5] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. In Deep power-down mode, pulling this pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low power oscillator is enabled for waking up the part from Deep power-down mode.

[7] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured as an analog I/O, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

Table 5. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC81xM contain a total of up to 4 kB on-chip static RAM data memory.

8.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I^2C-bus driver API routines

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Relocatable interrupt vector table using vector table offset register.

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight pins, regardless of the selected function, can be programmed to generate an interrupt on a level, a rising or falling edge, or both. The interrupt generating pins can be selected from all digital or mixed digital/analog pins. The pin interrupt/pattern match block controls the edge or level detection mechanism.

8.6 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.7 Memory map

The LPC81xM incorporates several distinct memory regions. Figure 7 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

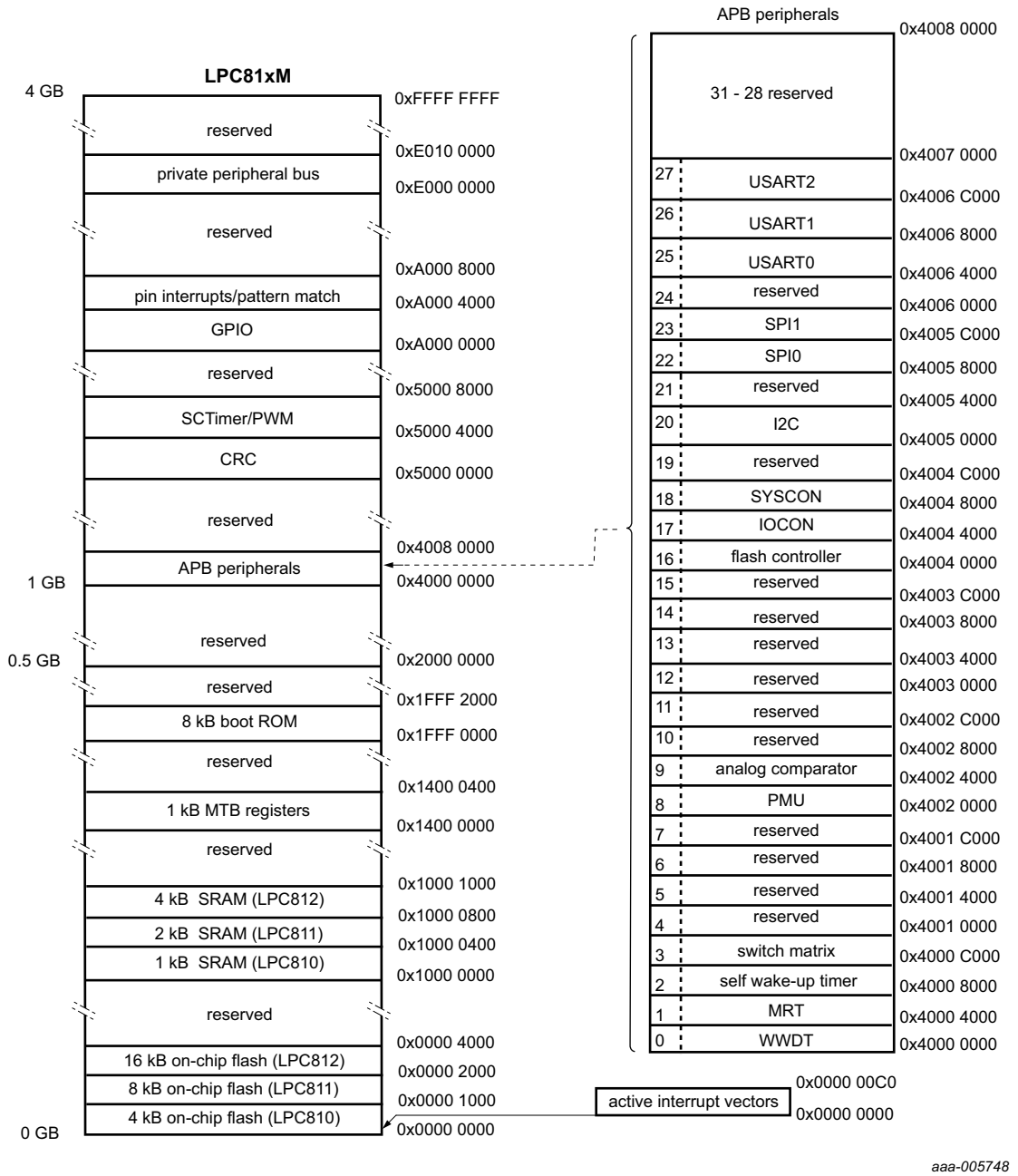


Fig 7. LPC81xM Memory map

8.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. This pin is not 5 V tolerant when V_{DD} = 0.

- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 10 “LPC81xM clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

8.8.1 Standard I/O pad configuration

Figure 8 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

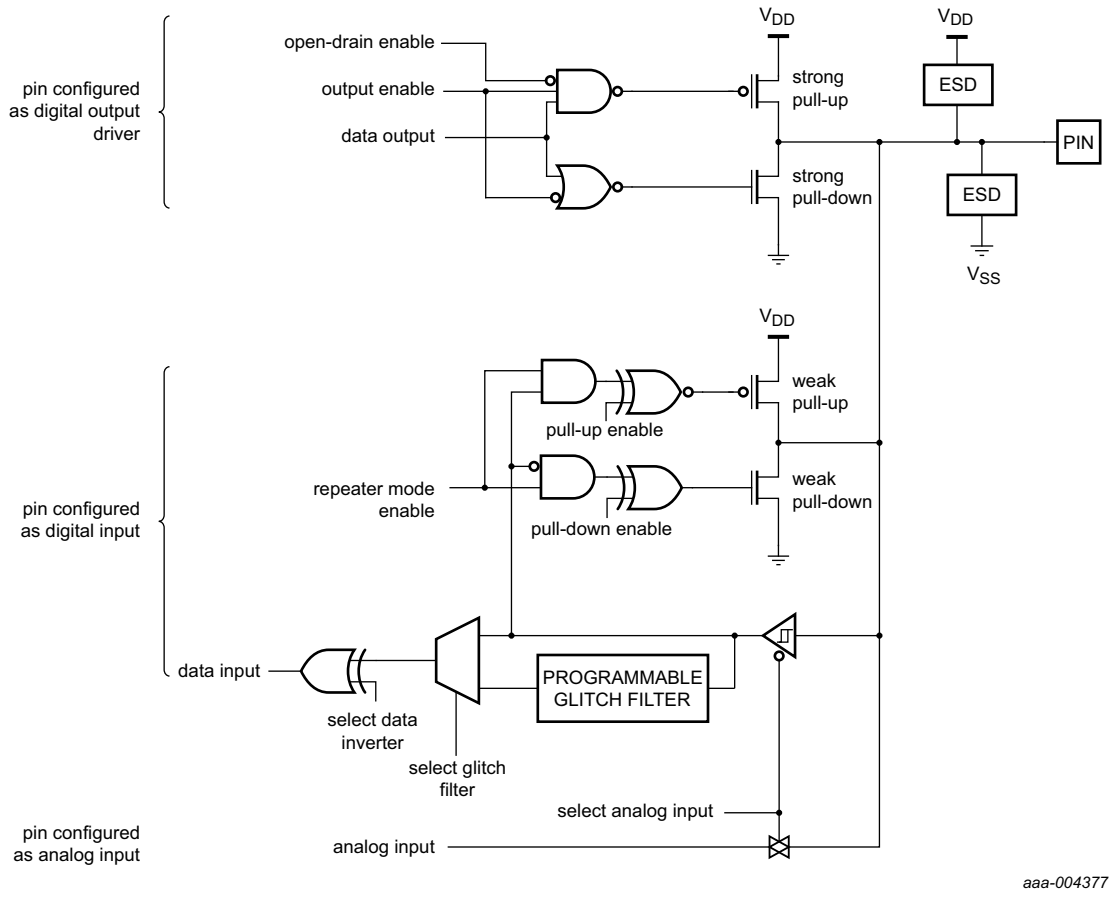


Fig 8. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 4. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 8).
-

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.

- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK)is generated by a the dedicated watchdog oscillator (WDOSC).

8.18 Self Wake-up Timer (WKT)

The self wake-up timer is a 32-bit, loadable down-counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur just prior to entering a reduced power mode.

8.18.1 Features

- 32-bit loadable down-counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports two clock sources: the low-power oscillator and the IRC. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in Deep power-down mode.
- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 23.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled or disabled on pins PIO0_0 and PIO0_1 through the switch matrix.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the RESET pin HIGH to prevent it from floating while in Deep power-down mode.

8.21 System control

8.21.1 Reset

Reset has four sources on the LPC81xM: the RESET pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The RESET pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the RESET pin.

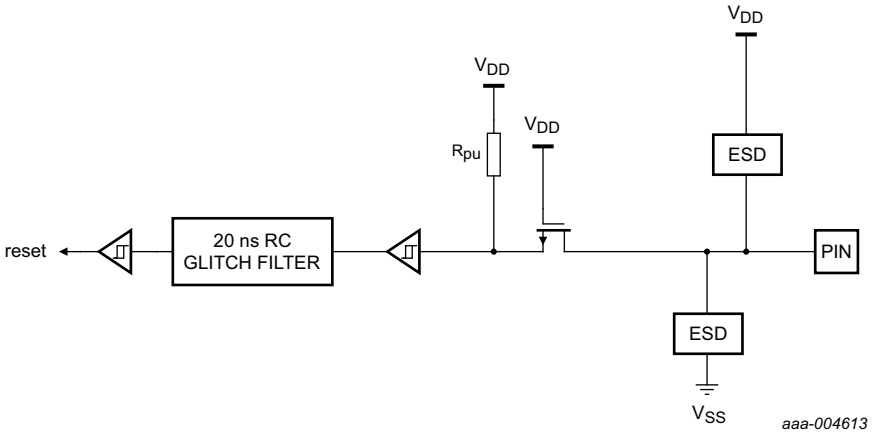


Fig 11. Reset pad configuration

8.21.2 Brownout detection

The LPC81xM includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

8.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

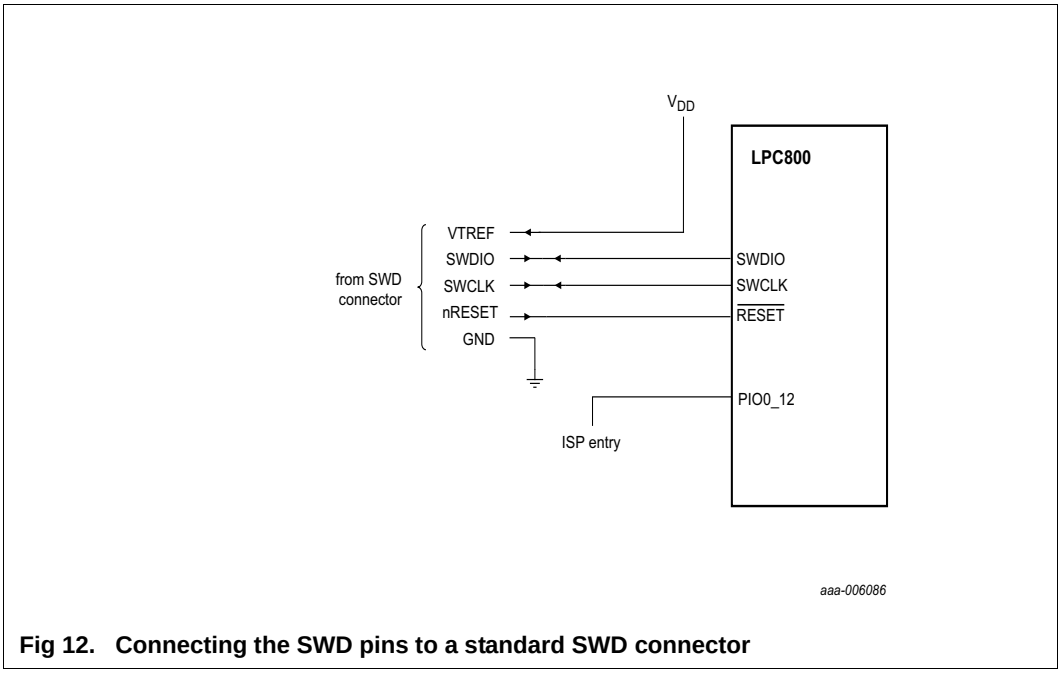


Fig 12. Connecting the SWD pins to a standard SWD connector

11. Static characteristics

Table 9. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][5]	-	1.4	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][5][6]	-	1.0	-	mA
		system clock = 24 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][7]	-	2.2	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][4][5][8]	-	3.3	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][8]	-	3	-	mA
		Sleep mode					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][5]	-	0.8	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][5][6]	-	0.7	-	mA
		system clock = 24 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][7]	-	1.3	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][4][5][8]	-	1.8	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][8]	-	1.7	-	mA
		Deep-sleep mode					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[2][9]	-	150	300	µA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[2][9]	-	-	400	µA
		Power-down mode					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[2][9]	-	0.9	5	µA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[2][9]	-	-	40	µA
		Deep power-down mode; Low-power oscillator and self wakeup timer (WKT) disabled					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[10]	-	170	1000	nA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[10]	-	-	4	µA
		Deep power-down mode; Low-power oscillator and self wakeup timer (WKT) enabled		-	1	-	µA

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, $\overline{\text{RESET}}$; see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_6	[11] [12]	0	-	5.0	V
		$V_{DD} \geq$ 1.8 V; on 3 V tolerant pin PIO0_6		0	-	3.6	
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = 4 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = 3 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[13]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		15	50	85	μA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	μA
		$V_{DD} < V_I$ < 5 V		0	0	0	μA
High-drive output pins configured as digital pins (PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13); see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA

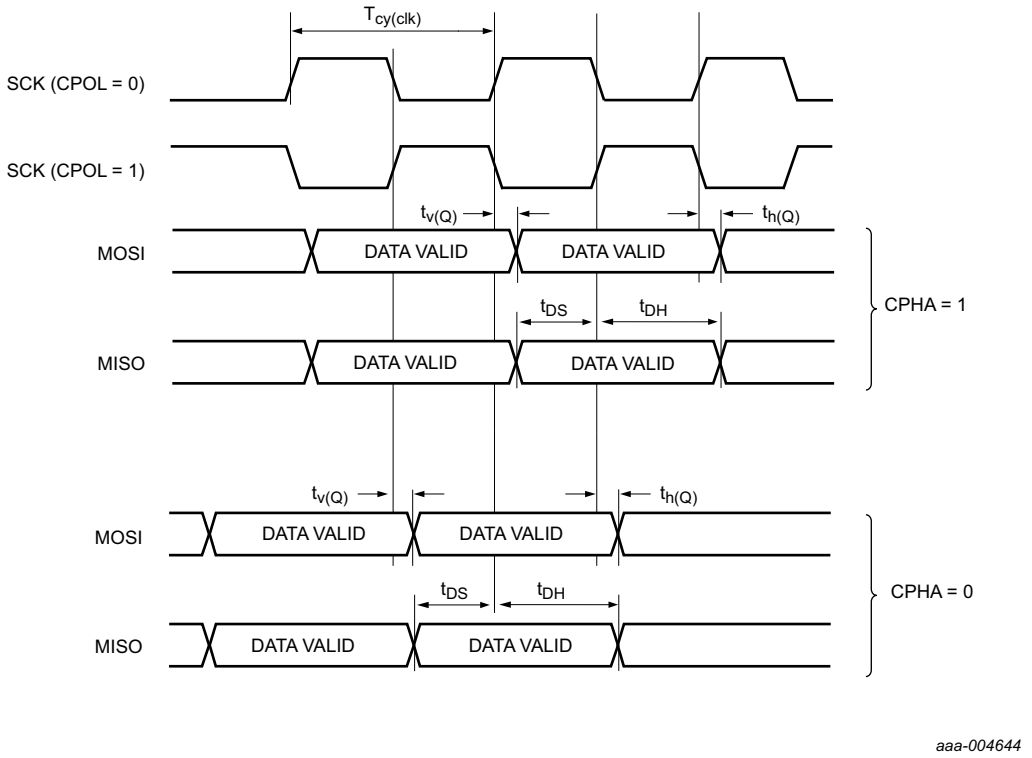
11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 30 MHz.

Table 10. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	30 MHz	
IRC	0.21	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.002	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
Main PLL	-	0.31	-	-
CLKOUT	-	0.06	0.09	Main clock divided by 4 in the CLKOUTDIV register.
ROM	-	0.08	0.19	-
I2C	-	0.06	0.15	-
GPIO + pin interrupt/pattern match	-	0.09	0.23	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	0.03	0.07	-
SCT	-	0.17	0.42	-
WKT	-	0.01	0.03	-
MRT	-	0.09	0.21	-
SPI0	-	0.05	0.13	-
SPI1	-	0.06	0.14	-
CRC	-	0.03	0.07	-
USART0	-	0.04	0.10	-
USART1	-	0.04	0.11	-
USART2	-	0.04	0.10	-
WWDT	-	0.04	0.10	Main clock selected as clock source for the WDT.
IOCON	-	0.03	0.08	-
Comparator	-	0.04	0.09	-



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 32. SPI master timing

14. Application information

14.1 Typical wake-up times

Table 25. Typical wake-up times (3.3 V, Temp = 25 °C)

Power modes	V_{DD} current	Wake-up time
Sleep mode (12 MHz)[1][2]	0.7 mA	2.6 μs
Deep-sleep mode[1][3]	150 μA	4 μs
Power-down mode[1][3]	0.9 μA	50 μs
Deep Power-down mode[4]	170 nA	215 μs

[1] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[2] IRC enabled, all peripherals off.

[3] Watchdog oscillator disabled, Brown-Out Detect (BOD) disabled.

[4] Self wakeup-timer disabled. Wake-up from deep power-down causes the LPC800 to go through entire reset process. The wake-up time measured is the time between when a wake-up pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the reset handler.

14.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

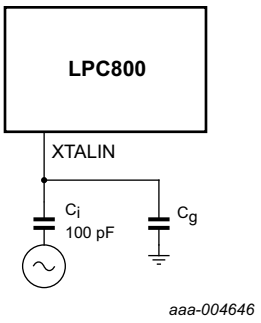
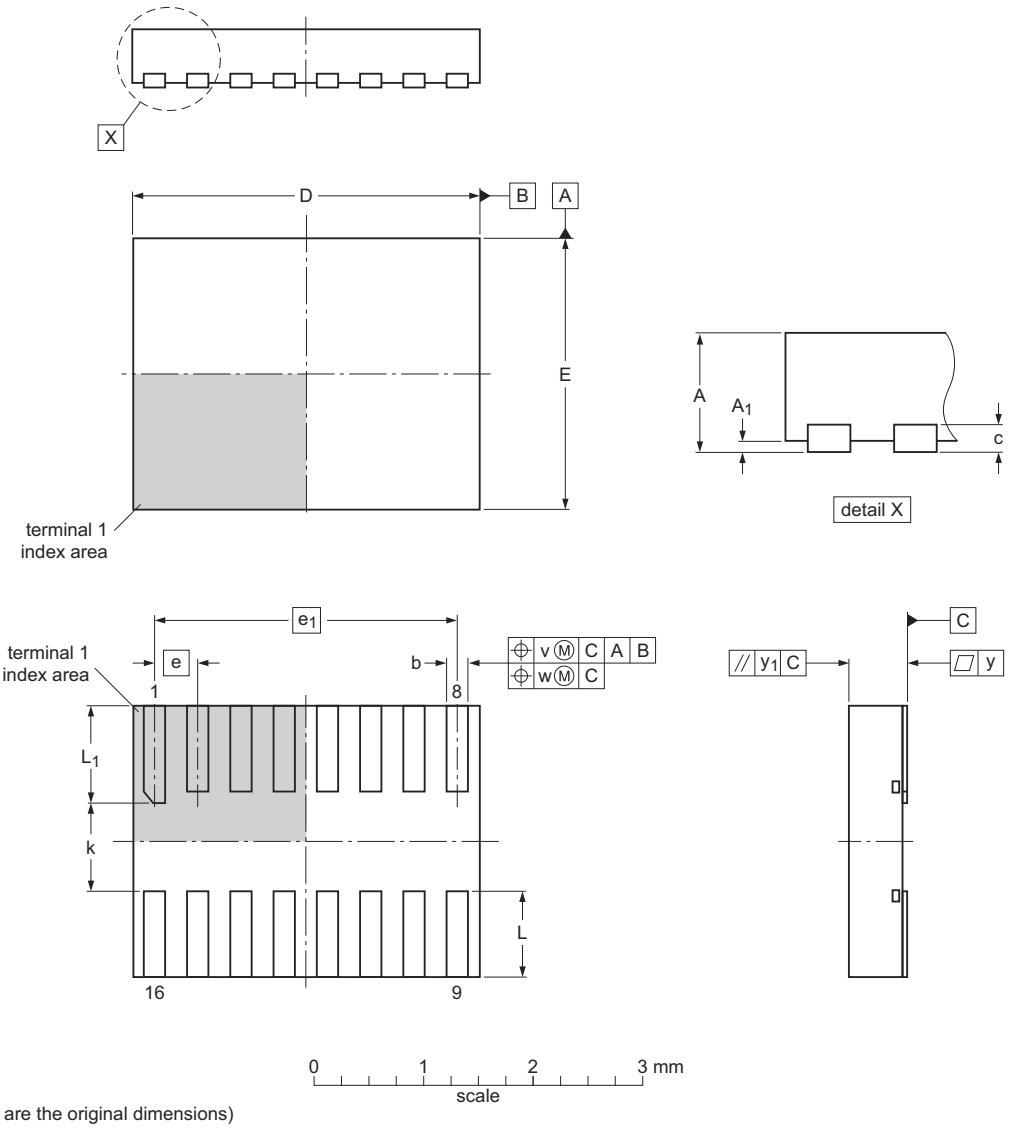


Fig 36. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 36), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 37 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and

XSON16: plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 x 3.2 x 0.5 mm **SOT1341-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	c	D	E	e	e_1	k	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	0.152	3.3	2.6				0.9	1.0				
	nom			0.20		3.2	2.5	0.4	2.8		0.8	0.9	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.050	3.1	2.4			0.2	0.7	0.8				

Note

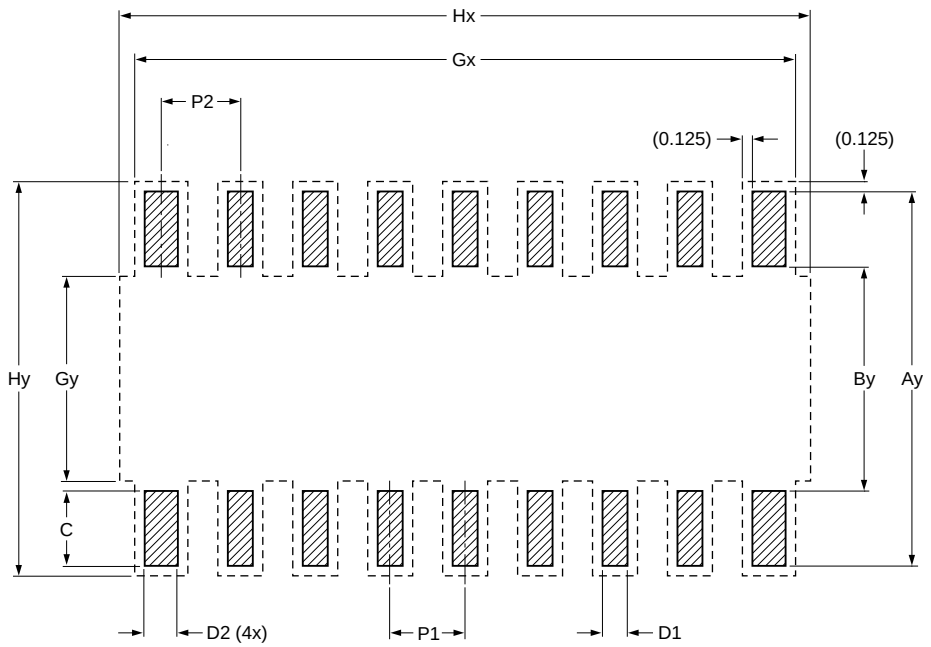
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1341-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1341-1	- - -	MO-252	- - -			~~12-09-05~~ 13-02-13

Fig 42. Package outline SOT1341-1 (XSON16)

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 45. Reflow soldering of the TSSOP20 package