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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Graphics Controller
Core Processor	x86
Program Memory Type	External Program Memory
Controller Series	STPC® Atlas
RAM Size	External
Interface	EBI/EMI, IDE, ISA, Local Bus, Monitor, PCMCIA, Serial, USB, Video
Number of I/O	-
Voltage - Supply	2.45V ~ 3.6V
Operating Temperature	-40°C ~ 115°C
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stpci2gdyi

controls for 3.3V suspend with Modem Ring Resume Detection.

The STPC Atlas implements a multi-function parallel port. The standard PC/AT compatible logical address assignments for LPT1, LPT2 and LPT3 are supported. It can be configured for any of the following three modes and supports the IEEE Standard 1284 parallel interface protocol standards, as follows:
- Compatibility Mode (Forward channel, standard)
- Nibble Mode (Reverse channel, PC compatible)
- Byte Mode (Reverse channel, PS/2 compatible)

The General Purpose Input/Output (GPIO) interface provides a 16-bit I/O facility, using 16 dedicated device pins. It is organised using two blocks of 8-bit Registers, one for lines 0 to 7, the other for lines 8 to 15.
Each GPIO port can be configured as an input or an output simply by programming the associated port direction control register. All GPIO ports are configured as inputs at reset, which also latches the input levels into the Strap Registers. The input states of the ports are thus recorded automatically at reset, and this can be used as a strap register anywhere in the system.

1.4. FEATURE MULTIPLEXING

The STPC Atlas BGA package has 516 balls. This however is not sufficient for all of the integrated functions available; some features therefore share the same balls and cannot thus be used at the same time. The STPC Atlas configuration is done by ‘strap options’. This is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the STPC Atlas.

There 3 multiplexed functions are the external ISA bus, the Local Bus and the PCMCIA interface.

1.5. POWER MANAGEMENT

The STPC Atlas core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit (PMU) module controls the power consumption, providing a comprehensive set of features that controls the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides the following hardware structures to assist the software in managing the system power consumption:

- System Activity Detection.

- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power-on state.

- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer periods of time is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate an SMI interrupt to allow the software to bring the system back up to full power-on state. The chip-set supports up to three power down states described above; these correspond to decreasing levels of power savings.

Power down puts the STPC Atlas into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power-down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

1.6. JTAG

JTAG stands for Joint Test Action Group and is the popular name for IEEE Std. 1149.1, Standard Test Access Port and Boundary-Scan Architec-ture. This built-in circuitry is used to assist in the test, maintenance and support of functional circuit blocks. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register so that a component is able to respond to a minimum set of test instructions.

1.7. CLOCK TREE

The STPC Atlas integrates many features and generates all its clocks from a single 14MHz oscillator. This results in multiple clock domains as described in Figure 1-2.

The speed of the PLLs is either fixed (DEVCLK), either programmable by strap option (HCLK) either programmable by software (DCLK, MCLK). When in synchronized mode, MCLK speed is fixed to HCLKO speed and HCLKI is generated from MCLKI.

Figure 1-2. STPC Atlas clock architecture

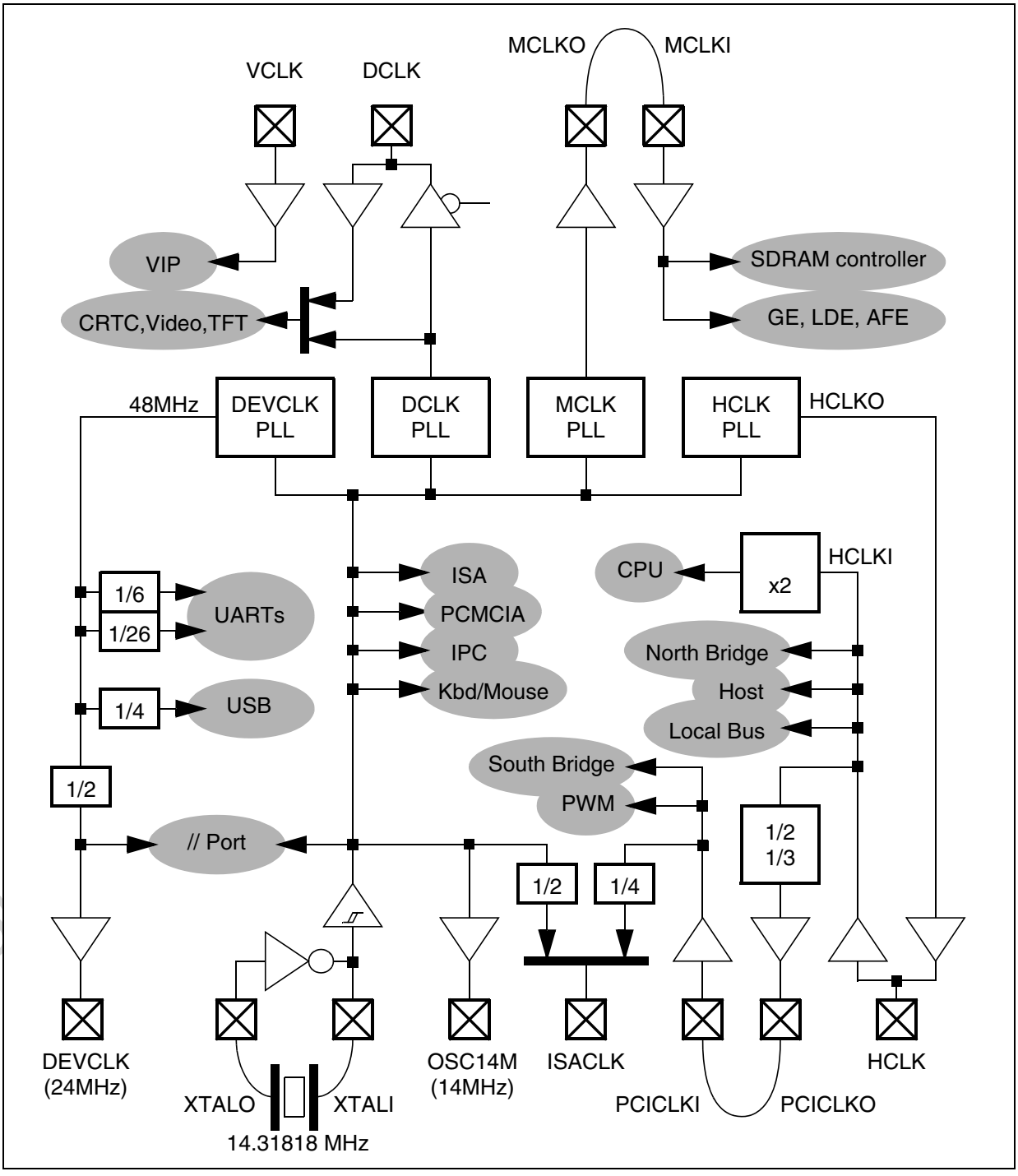


Table 2-6. Pinout

Pin#	Pin Name
E5	GND
E22	GND
F6	GND
F8	GND
F9	GND
F10	GND
F12	GND
F14	GND
F16	GND
F18	GND
F19	GND
F21	GND
H4	GND
H21	GND
H23	GND
J6	GND
L6	GND
L11:16	GND
L21	GND
M6	GND
M11:16	GND
N11:16	GND
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
N21	GND
P6	GND
P11:16	GND
R11:16	GND
R21	GND
T6	GND
T11:16	GND
T21	GND
V21	GND
V23	GND
W4	GND
W6	GND
W21	GND
AA6	GND
AA8	GND
AA9	GND
AA11	GND
AA13	GND
AA15	GND
AA17	GND
AA19	GND
AA21	GND
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
AB5	GND
AB22	GND
AC4	GND
AC11	GND
AC17	GND
AC23	GND
AD3	GND
AD24	GND
AE2	GND
AE25	GND
AF1	GND
AF26	GND
G3	*Reserved*
F1	*Reserved*
Note[1]; This signal is multiplexed see Table 2-4	

3.1.3 HCLK PLL STRAP REGISTER

This register is read only.

HCLK_STRAP0 Access = 0022h/0023h Regoffset =05Fh

7	6	5	4	3	2	1	0
RSV		MD[26]	MD[25]	MD[24]	RSV		
This register defaults to the values sampled on the MD pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-6	Rsv	These bits are fixed to ‘0’
Bits 5-3	MD[26:24]	These pins reflect the values sampled on MD[26:24] pins respectively and control the Host clock frequency synthesizer as shown in Table 3-1
Bits 2-0	Rsv	Reserved

Table 3-1. HCLK Frequency Configuration

MD[3]	MD[2]	MD[26]	MD[25]	MD[24]	HCLK Speed
0	0	0	0	0	25 MHz
0	0	0	0	1	50 MHz
0	0	0	1	0	60 MHz
0	0	0	1	1	66 MHz
All other settings are reserved					

Table 3-1. Typical Strap Option Implementation

Signal	Designation	Actual Settings	Description
MD35	Reserved[2]	Pull up	
MD36	Local Bus Boot Device Size	User defined	Not Applicable
MD37	Reserved[2]	Pull down	-
MD38	Reserved[2]	Pull down	-
MD40	CPU clock Multiplication	Pull up	X2 mode
MD41	Reserved[2]	Pull down	-
MD42	Reserved[2]	Pull up	-
MD 43	Reserved[2]	Pull down	-
MD 45	CPUCLK/HCKL Deskew Programming	Pull down	HCLK between 64MHz and 133MHz
MD 46		Pull up	
MD 47	Reserved[2]	Pull down	-
MD 48	Reserved[2]	Pull up	-
MD 50	Internal UART2 (see Section 3.1.4.)	Pull up	Enable
MD 51	Internal UART1 (see Section 3.1.4.)	Pull up	Enable
MD 52	Internal Kbd / Mouse (see Section 3.1.4.)	Pull up	Enable
MD 53	Internal Parallel Port (see Section 3.1.4.)	Pull up	Enable
TC[1]	Reserved[2]	Pull up	-
DACK_ENC[2][1]	Reserved[2]	Pull up	-
DACK_ENC[1][1]	Reserved[2]	Pull up	-
DACK_ENC[0][1]	Reserved[2]	Pull up	-

Note[1]: Strap options on TC/PA[3] and DACK_ENC[2:0]/PA[2:0] are required for all the STPC Atlas Configurations (ISA, PCMCIA, Local Bus).
Note[2]: Must be implemented.

Figure 4-3. Power-on timing diagram

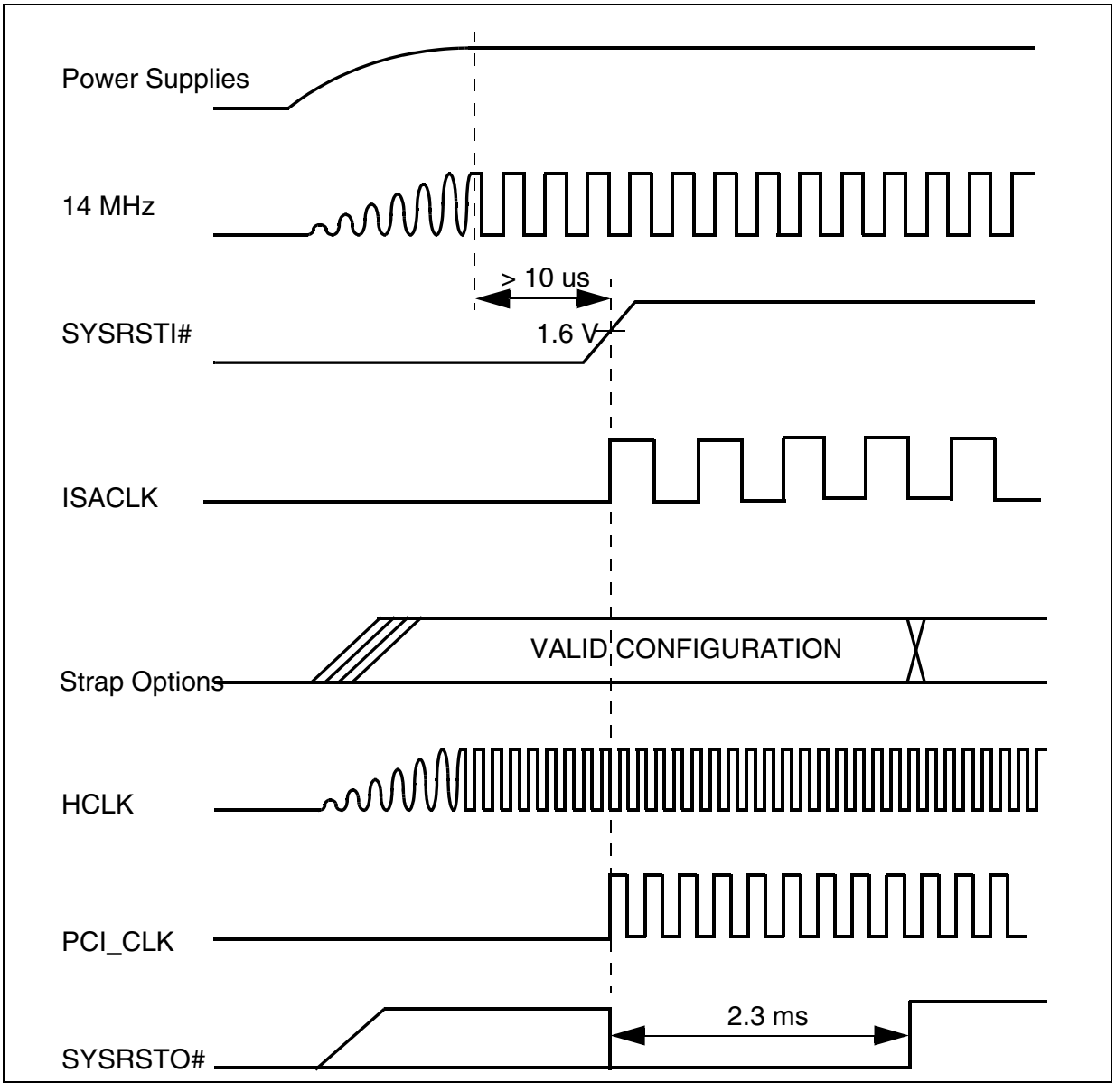


Table 4-11. SDRAM Bus AC Timings - Industrial Temperature Range

Name	Parameter	Min	Typ	Max	Unit
Tcycle	MCLKI Cycle Time	11			ns
Thigh	MCLKI High Time	4			ns
Tlow	MCLKI Low Time	4			ns
	MCLKI Rising Time			1	ns
	MCLKI Falling Time			1	ns
Tdelay	MCLKx to MCLKI delay	0.5	1	1.5	ns
Toutput	MCLKI to RAS# Valid	1.7		6.5	ns
	MCLKI to CAS# Valid	1.7		6.5	ns
	MCLKI to CS# Valid	1.7		6	ns
	MCLKI to DQM[ ] Outputs Valid	2		6	ns
	MCLKI to MD[ ] Outputs Valid	2		7.8	ns
	MCLKI to MA[ ] Outputs Valid	1.7		6.5	ns
	MCLKI to MWE# Valid	1.7		6	ns
Tsetup	MD[63:0] setup to MCKLI	4.7			ns
Thold	MD[63:0] hold from MCKLI	-0.36		2.3	ns
Note: These timings are for a load of 50pF, part running at 90MHz and ReadCLK not activated					

The PC100 memory is recommended to reach 90MHz operation.

4.5.9 IDE INTERFACE

Figure 4-13, Figure 4-14 and Table 4-18 lists the AC characteristics of the IDE interface.

Figure 4-13. IDE PIO timing diagram

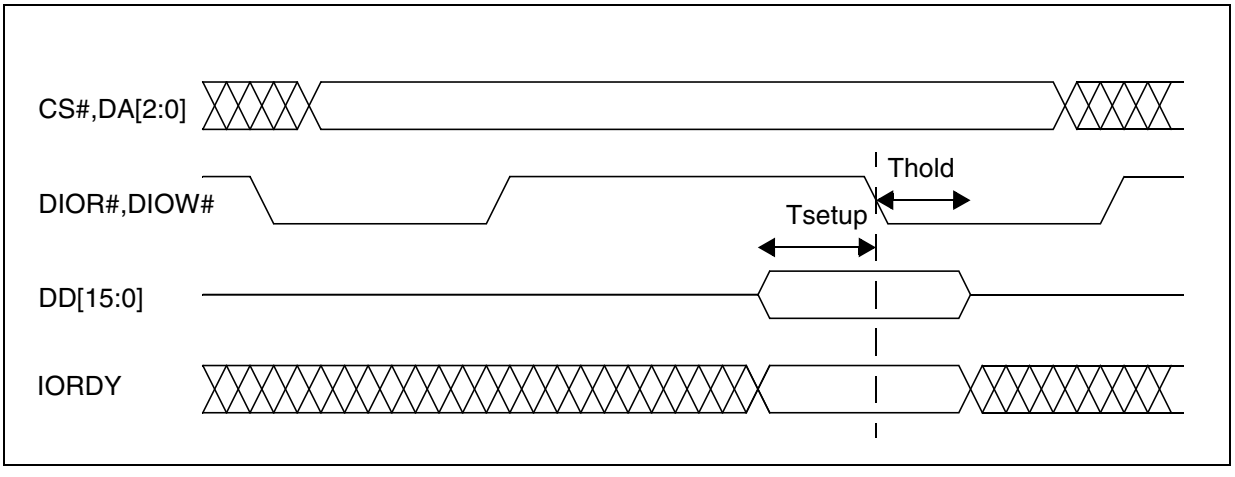


Figure 4-14. IDE DMA timing diagram

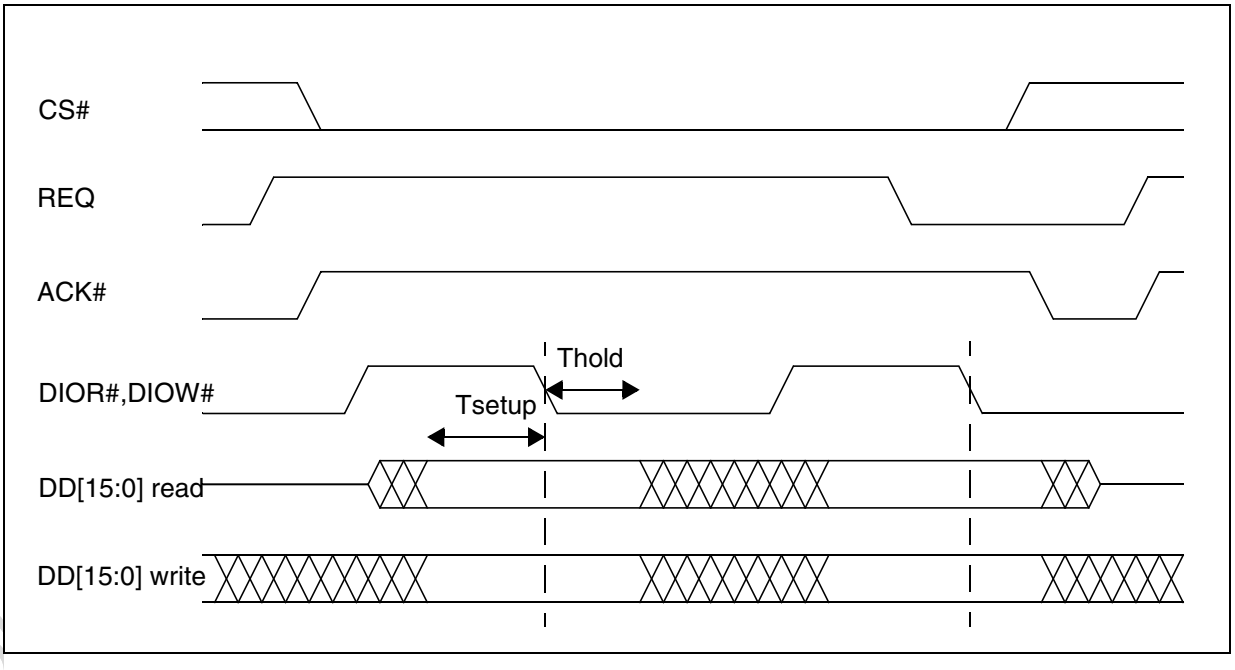


Table 4-18. IDE Interface Timing

Name	Parameters	Min	Max	Units
Tsetup	DD[15:0] setup to PIOR#/SIOR# falling	15	-	ns
Thold	DD[15:0} hold to PIOR#/SIOR# falling	0	-	ns

4.5.10 TFT INTERFACE

Table 4-19 lists the AC characteristics of the TFT interface.

Table 4-19. TFT Interface Timings

Name	Parameters	Min	Max	Units
	DCLK (input) to R[5:0], G[5:0], B[5;0]			nS
	DCLK (input) to FPLINE			nS
	DCLK (input) to FPFRAME			nS
	DCLK (output) to R[5:0], G[5:0], B[5;0]		15	nS
	DCLK (output) to FPLINE		15	nS
	DCLK (output) to FPFRAME		15	nS

4.5.11 USB INTERFACE

The USB interface integrated into the STPC device is compliant with the USB 1.1 standard.

4.5.12 KEYBOARD & MOUSE INTERFACES

Table 4-20 and Table 4-21 list the AC characteristics of the Keyboard and Mouse interfaces.

Table 4-20. Keyboard Interface AC Timing

Name	Parameters	Min	Max	Units
	Input setup to KBCLK	5	-	nS
	Input hold to KBCLK	1	-	nS
	KBCLK to KBDATA	-	12	nS

Table 4-21. Mouse Interface AC Timing

Name	Parameters	Min	Max	Units
	Input setup to MCLK	5	-	nS
	Input hold to MCLK	1	-	nS
	MCLK to MDATA	-	12	nS

4.5.13 IEEE1284 INTERFACE

Table 4-22 lists the AC characteristics of the Keyboard and Mouse interfaces.

Table 4-22. Parallel Interface AC Timing

Name	Parameters	Min	Max	Units
	STROBE# to BUSY setup	0	-	nS
	PD bus to AUTPFD# hold	0	-	nS
	PB bus to BUSY setup	0	-	nS

Table 5-1. 516-pin PBGA Package - PCB Dimensions

F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 5-3. 516-pin PBGA Package - Dimensions

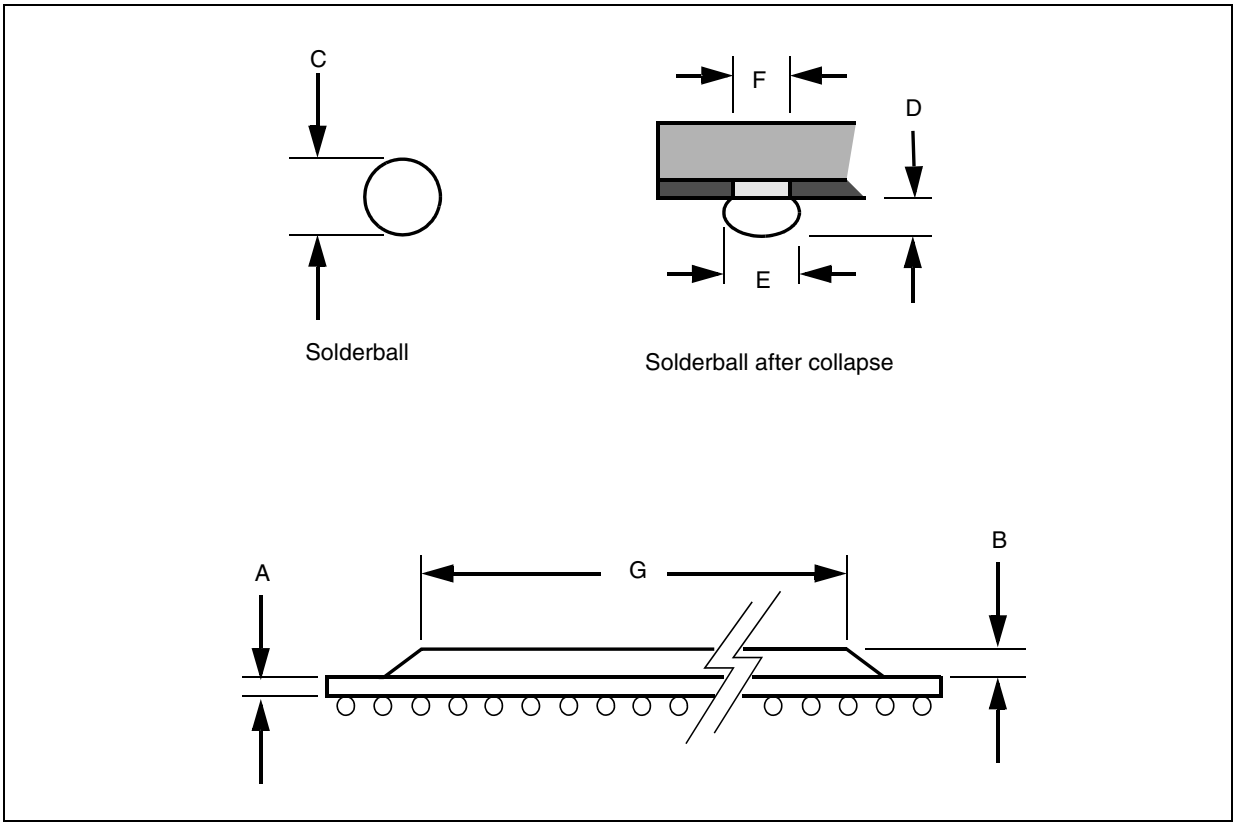


Table 5-2. 516-pin PBGA Package - Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

5.2. 516-PIN PACKAGE THERMAL DATA

516-pin PBGA package has a Power Dissipation Capability of 4.5W which increases to 6W when used with a Heatsink.

The structure in shown in Figure 5-4.

Thermal dissipation options are illustrated in Figure 5-5 and Figure 5-6.

Figure 5-4. 516-Pin PBGA Structure

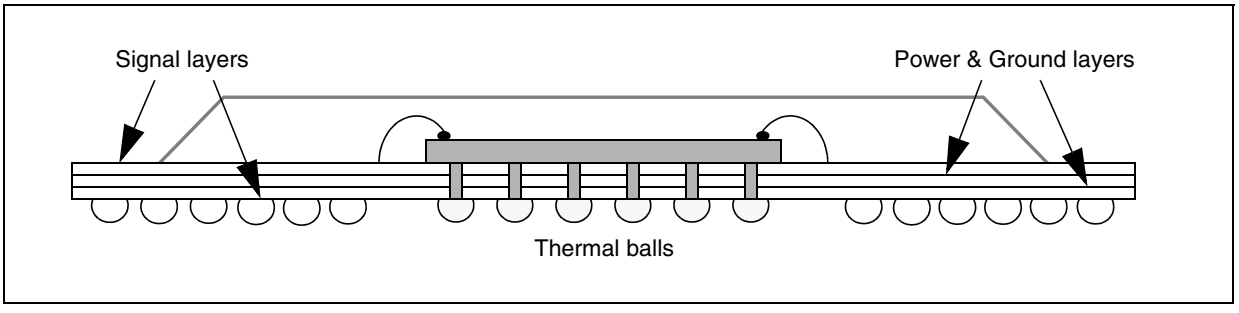
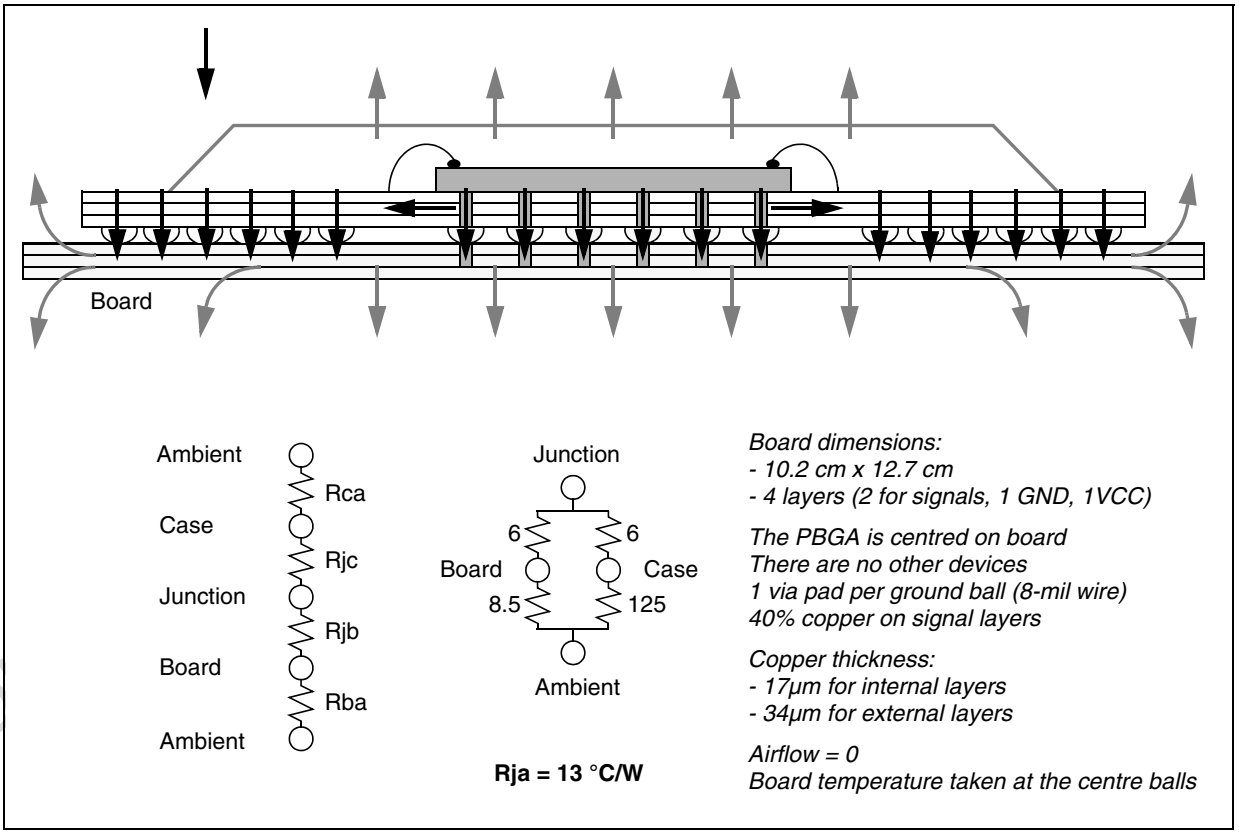


Figure 5-5. Thermal Dissipation Without Heatsink



5.3. SOLDERING RECOMMENDATIONS

High quality, low defect soldering requires identifying the **optimum temperature profile** for reflowing the solder paste, therefore optimizing the process. The heating and cooling rise rates must be compatible with the solder paste and components. A typical profile consists of a preheat, dryout, reflow and cooling sections.

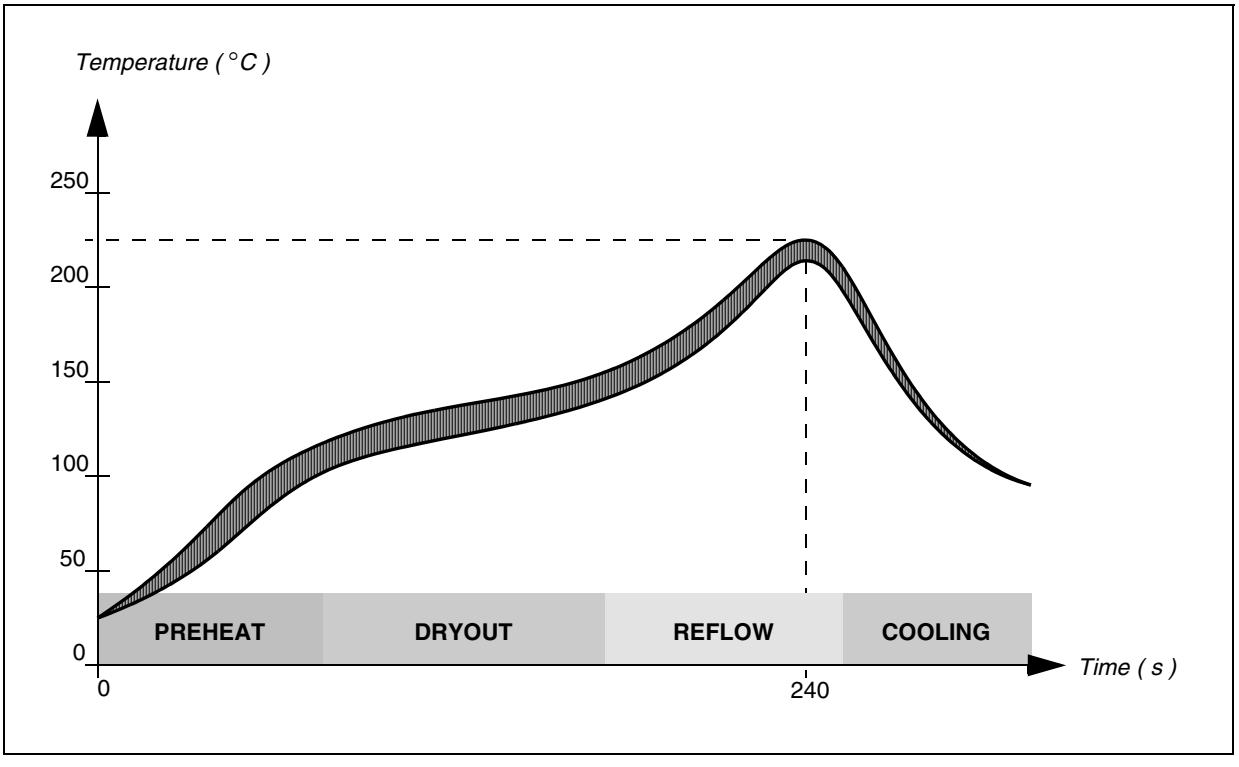
The most critical parameter in the **preheat section** is to minimize the rate of temperature rise to less than 2°C / second, in order to minimize thermal shock on the semi-conductor components.

Dryout section is used primarily to ensure that the solder paste is fully dried before hitting reflow temperatures.

Solder reflow is accomplished in the **reflow zone**, where the solder paste is elevated to a temperature greater than the melting point of the solder. Melting temperature must be exceeded by approximately 20°C to ensure quality reflow.

In reality the profile is not a line, but rather **a range of temperatures** all solder joints must be exposed. The total temperature deviation from component thermal mismatch, oven loading and oven uniformity must be within the band.

Figure 5-7. Reflow soldering temperature range



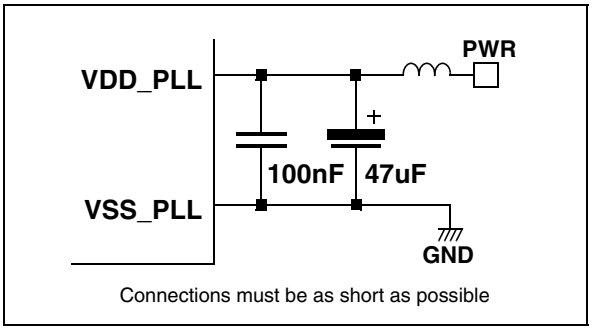
6.3.1. POWER DECOUPLING

An appropriate decoupling of the various STPC power pins is mandatory for optimum behaviour. When insufficient, the integrity of the signals is deteriorated, the stability of the system is reduced and EMC is increased.

6.3.1.1. PLL decoupling

This is the most important as the STPC clocks are generated from a single 14MHz stage using multiple PLLs which are highly sensitive analog cells. The frequencies to filter are the 25-50 KHz range which correspond to the internal loop bandwidth of the PLL and the 10 to 100 MHz frequency of the output. PLL power pins can be tied together to simplify the board layout.

Figure 6-3. PLL decoupling



6.3.1.2. Decoupling of 3.3V and Vcore

A power plane for each of these supplies with one decoupling capacitance for each power pin is the minimum. The use of multiple capacitances with values in decade is the best (for example: 10pF, 1nF, 100nF, 10uF), the smallest value, the closest to the power pin. Connecting the various digital power planes through capacitances will reduce furthermore the overall impedance and electrical noise.

6.3.2. 14MHZ OSCILLATOR STAGE

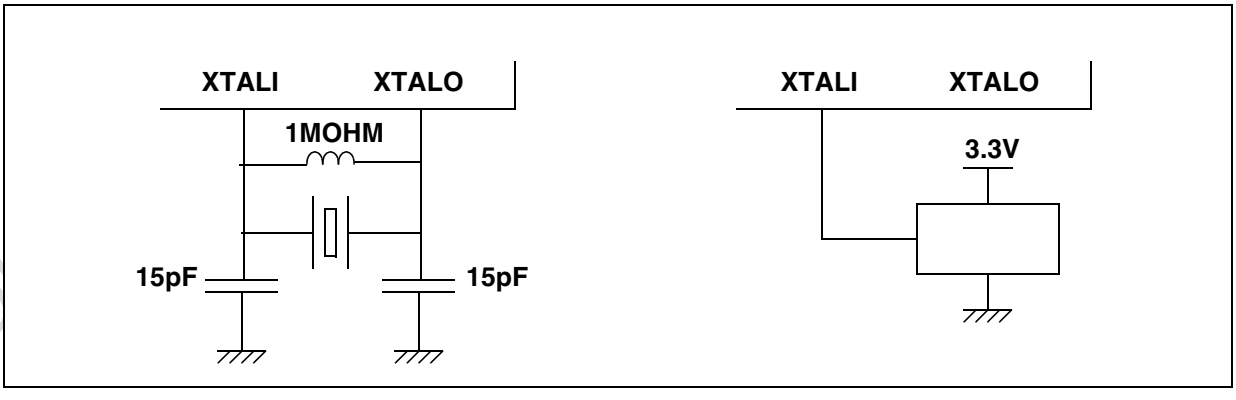
The 14.31818 MHz oscillator stage can be implemented using a quartz, which is the preferred and cheaper solution, or using an external 3.3V oscillator.

The crystal must be used in its series-cut fundamental mode and not in overtone mode. It must have an Equivalent Series Resistance (ESR, sometimes referred to as Rm) of less than 50 Ohms (typically 8 Ohms) and a shunt capacitance (Co) of less than 7 pF. The balance capacitors of 16 pF must be added, one connected to each pin, as described in Figure 6-4.

In the event of an external oscillator providing the master clock signal to the STPC device, the LVTTL signal should be connected to XTALI, as described in Figure 6-4.

As this clock is the reference for all the other on-chip generated clocks, it is **strongly recommended to shield this stage**, including the 2 wires going to the STPC balls, in order to reduce the jitter to the minimum and reach the optimum system stability.

Figure 6-4. 14.31818 MHz stage

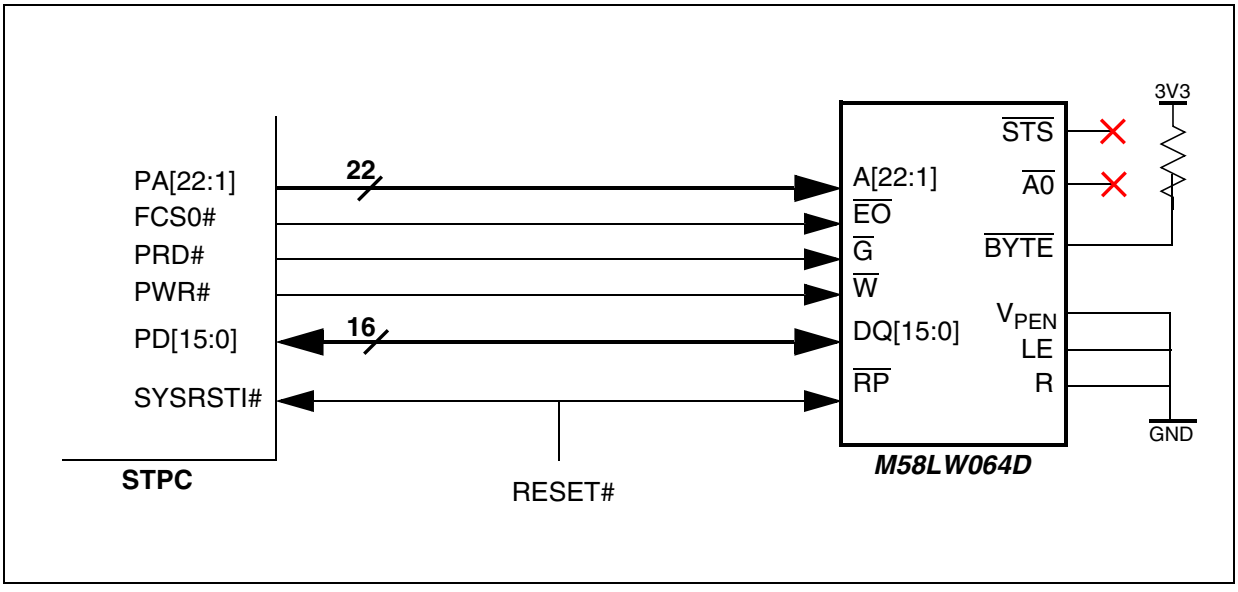


6.3.5. LOCAL BUS

The local bus has all the signals to directly connect flash devices or I/O devices.

Figure 6-10 describes how to connect a 16-bit boot flash (the corresponding strap options must be set accordingly).

Figure 6-10. Typical 16-bit boot flash implementation

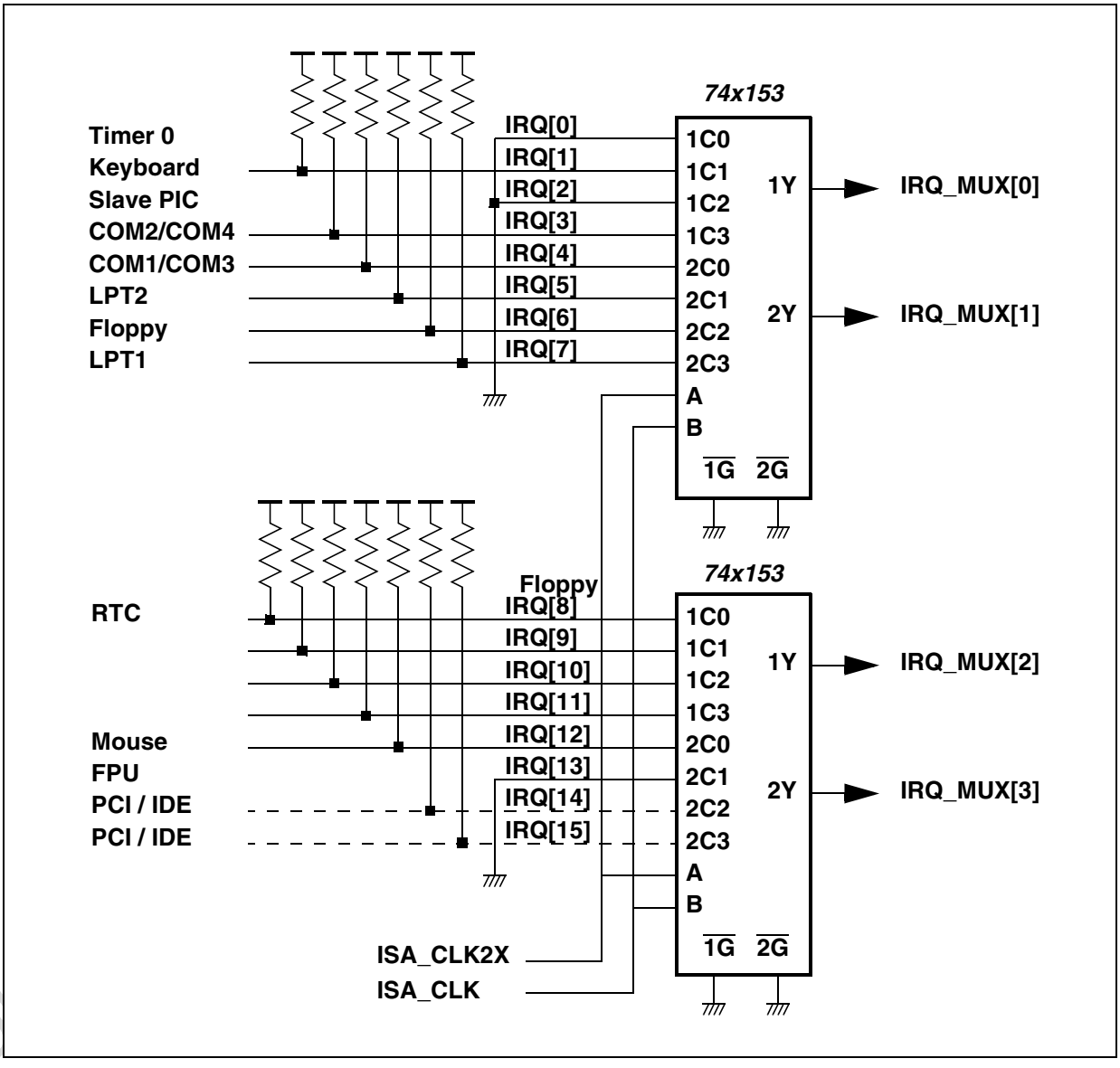


6.3.6. IPC

Most of the IPC signals are multiplexed: Interrupt inputs, DMA Request inputs, DMA Acknowledge outputs. The figure below describes a complete implementation of the IRQ[15:0] time-multiplexing.

When an interrupt line is used internally, the corresponding input can be grounded. In most of the embedded designs, only few interrupts lines are necessary and the glue logic can be simplified.

Figure 6-11. Typical IRQ multiplexing



When the interface is integrated into the STPC, the corresponding interrupt line can be grounded as it is connected internally.

For example, if the integrated IDE controller is activated, the IRQ[14] and IRQ[15] inputs can be grounded.

6.5.1. PCI INTERFACE

6.5.1.1. Introduction

In order to achieve a PCI interface which work at clock frequencies up to 33MHz, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration.

6.5.1.2. PCI Clocking Scheme

The PCI Clocking Scheme deserves a special mention here. Basically the PCI clock (PCICLKO) is generated on-chip from HCLK through a programmable delay line and a clock divider. The nominal frequency is 33MHz. This clock must be looped to PCICLKI and goes to the internal South Bridge through a deskewer. On the contrary, the internal North Bridge is clocked by HCLK, putting some additionnal constraints on T_0 and T_1.

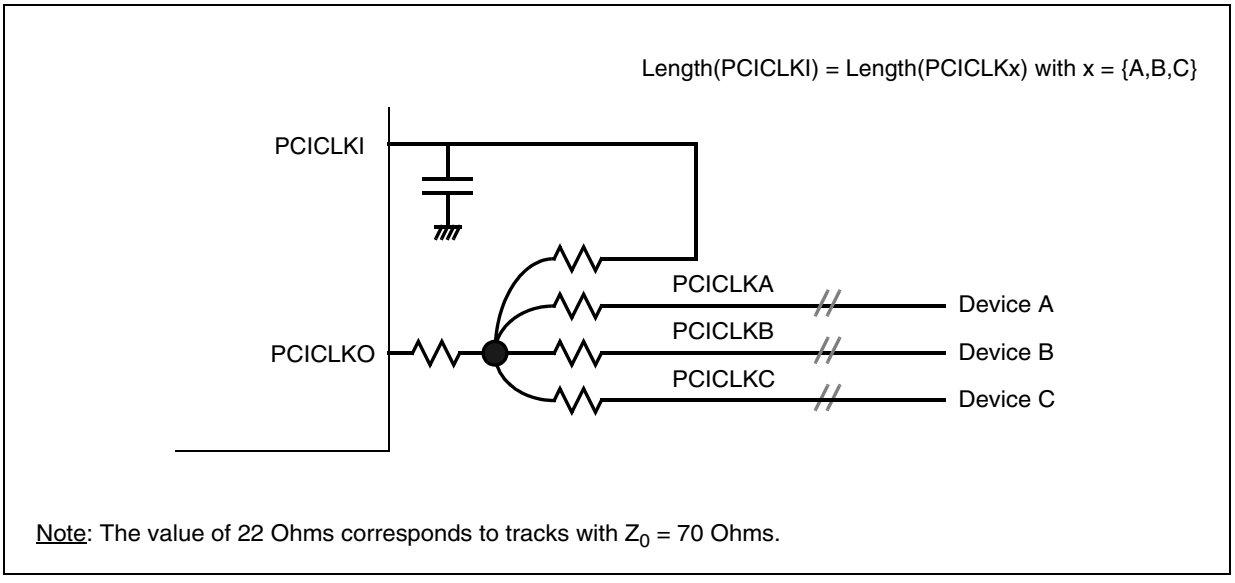
6.5.1.3. Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown in Figure 6-29. For the PCI interface, the most critical signal is the clock. Any skew between the clocks at the PCI components and the STPC will impact the timing budget. In order to get well matched clocks at all components it is recommended that all the PCI clocks are individually driven from a serial resistance with matched routing lengths. In other words, all clock line lengths that go from the resistor to the PCI chips (PCICLKx) must be identical.

The figure below is for PCI devices soldered on-board. In the case of a PCI slot, the wire length must be shortened by 2.5" to compensate the clock layout on the PCI board. The maximum clock skew between all devices is 2ns according to PCI specifications.

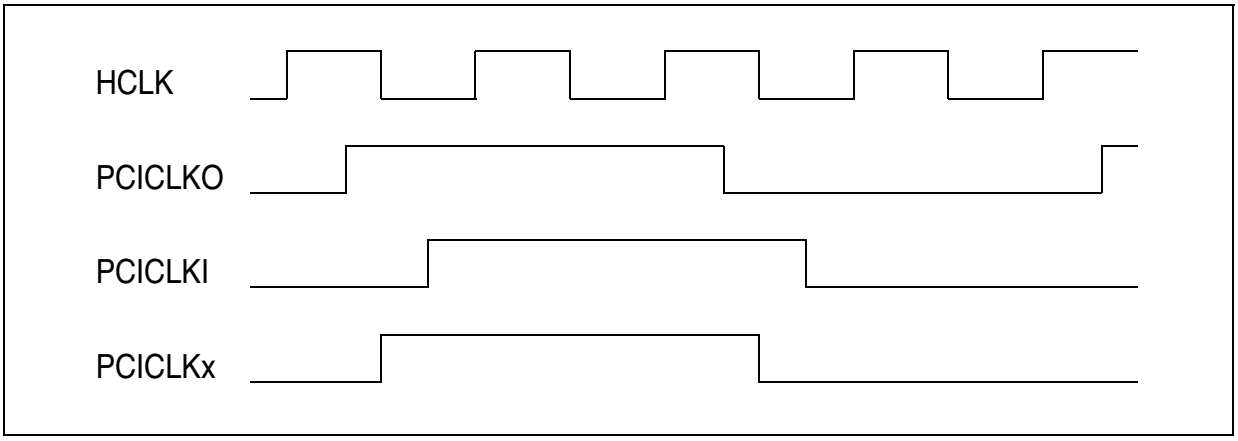
The Figure 6-30 describes a typical clock delay implementation. The exact timing constraints are listed in the PCI section of the **Electrical Specifications** Chapter.

Figure 6-29. Typical PCI clock routing



Note: The value of 22 Ohms corresponds to tracks with Z_0 = 70 Ohms.

Figure 6-30. Clocks relationships



6.5.2. THERMAL DISSIPATION

6.5.2.1. Power saving

Thermal dissipation of the STPC depends mainly on supply voltage. When the system does not need to work at the upper voltage limit, it may therefore be beneficial to reduce the voltage to the lower voltage limit, where possible. This could save a few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

6.5.2.2. Thermal balls

The standard way to route thermal balls to ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

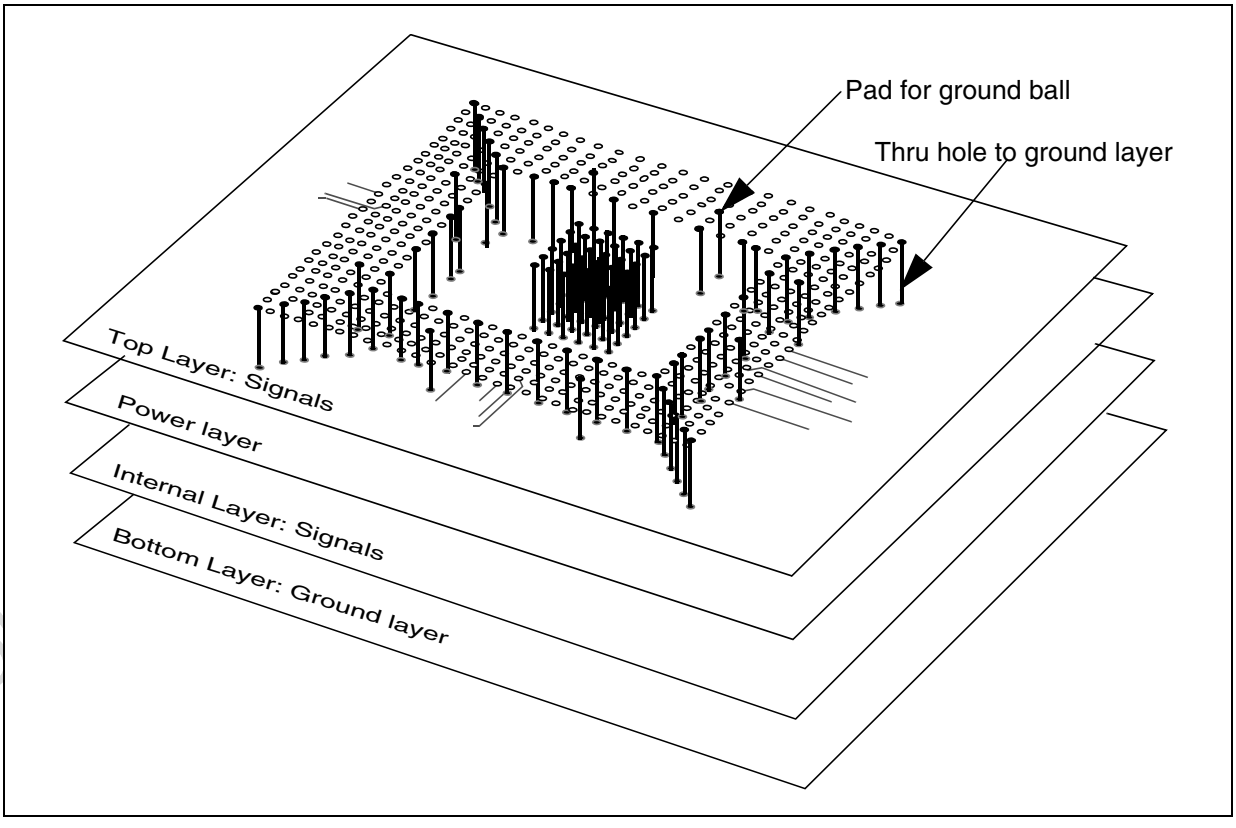
With such configuration the Plastic BGA package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die. The remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules must be followed when routing the STPC in order to avoid thermal problems.

As the whole ground layer acts as a heat sink, the ground balls must be directly connected to it, as illustrated in Figure 5-2. If one ground layer is not enough, a second ground plane may be added.

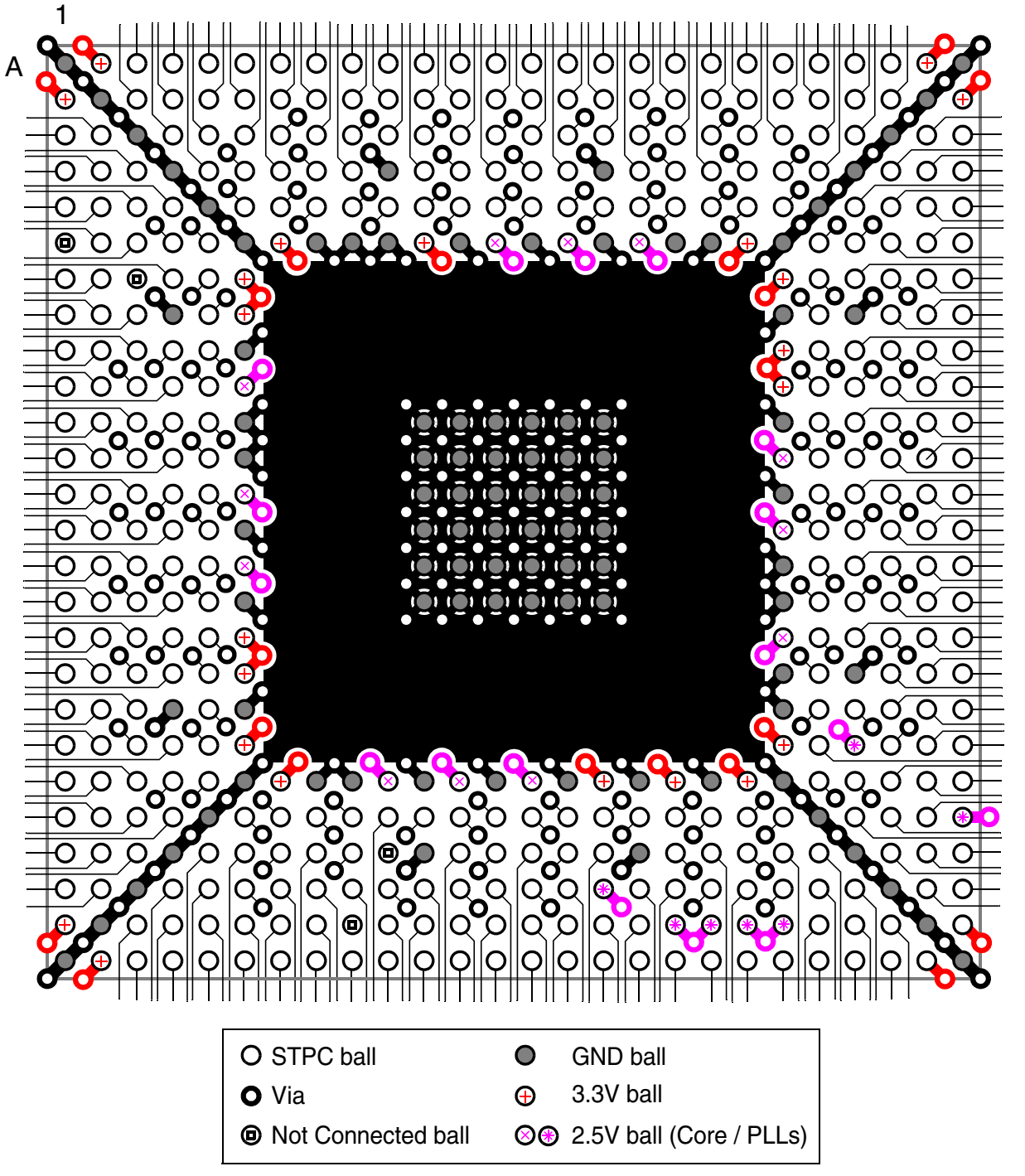
When possible, it is important to avoid other devices on-board using the PCB for heat dissipation, like linear regulators, as this would heat the STPC itself and reduce the temperature range of the whole system, In case these devices can not use a separate heat sink, they must not be located just near the STPC

Figure 6-31. Ground Routing



As the PCB acts as a heat sink, the layout of top and ground layers must be done with care to maximize the board surface dissipating the heat. The only limitation is the risk of losing routing channels. Figure 6-36 and Figure 6-37 show a routing with a good thermal dissipation thanks to an optimized placement of power and signal vias. The ground plane should be on bottom layer for the best heat spreading (thicker layer than internal ones) and dissipation (direct contact with air). .

Figure 6-36. Layout for Good Thermal Dissipation - top layer



6.6.3.3. POST code

Once the 16 first bytes are fetched and decoded, the CPU core continue its execution depending on the content of these first data. Usually, it corresponds to a JUMP instruction and the code fetching continues, generating read cycles on the ISA bus.

Most of the BIOS and boot loaders are reading the content of the flash, decompressing it in SDRAM, and then continue the execution by jumping to the entry point in RAM. This boot process ends with a JUMP to the entry point of the OS launcher.
These various steps of the booting sequence are codified by the so-called POST codes (Power-On Self-Test). A 8-bit code is written to the port 80H at the beginning of each stage of the booting process (I/O write to address 0080H) and can be displayed on two 7-segment display, enabling a fast visual check of the booting completion level.
Usually, the last POST code is 0x00 and corresponds to the jump into the OS launcher.

When the execution fails or hangs, the lastest written code stays visible on that display, indicating either the piece of code to analyse, either the area of the hardware not working properly.

6.6.4. LOCAL BUS MODE

As the Local Bus controller is located into the Host interface, there is no access to the cycles on the PCI, reducing the amount of signals to check.

6.6.4.1. First code fetches

When booting on the Local Bus, the key signal to check at the very beginning is FCS0#. This signal is a Chip Select for the boot flash and should toggle together with PRD# to fetch the first 16 bytes of code. This corresponds to the loading of the first line of the CPU cache.
In case FCS0# does not toggle, then one of the previous steps has not been done properly, like HCLK speed and CPU clock multiplier (x1, x2).

6.6.4.2. Boot Flash size

The Local Bus support 8-bit and 16-bit boot memory devices only.

6.6.4.3. POST code

Like in ISA mode, POST codes can be implemented on the Local Bus. The difference is that an IOCS# must be programmed at I/O address 80H prior to writing these code, the POST display being connected to this IOCS# and to the lower 8 bits of the bus.

6.6.5. SUMMARY

Here is a check-list for the STPC board debug from power-on to CPU execution.

For each step, in case of failure, verify first the corresponding balls of the STPC:
- check if the voltage or activity is correct
- search for potential shortcuts.

For troubleshooting in steps 5 to 10, verify the related strap options:
- value & connection. Refer to Section 3.
- see Figure 4-3 for timing constraints

Steps 8a and 9a are for debug in ISA mode while steps 8b and 9b are for Local Bus mode.

6.6.6. PCMCIA mode

As the STPC uses the RMRTCCS# signal for booting in that mode, the methodology is the same as for the ISA bus. The PCMCIA cards being 3.3V or 5V, the boot flash device must be 5V tolerant when directly connected on the address and data busses. An other solution is to isolate the flash from the PCMCIA lines using 5V tolerant LVTTL buffers.

	Check:	How?	Troubleshooting
1	Power supplies	Verify that voltage is within specs: - this must include HF & LF noise - avoid full range sweep Refer to Table 4-1 for values	Measure voltage near STPC balls: - use very low GND connection. Add some decoupling capacitor: - the smallest, the nearest to STPC balls.
2	14.318 MHz	Verify OSC14M speed	The 2 capacitors used with the quartz must match with the capacitance of the crystal. Try other values.
3	SYSRSTI# (Power Good)	Measure SYSRSTI# of STPC See Figure 4-3 for waveforms.	Verify reset generation circuit: - device reference - components value