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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Graphics Controller
Core Processor	x86
Program Memory Type	External Program Memory
Controller Series	STPC® Atlas
RAM Size	External
Interface	EBI/EMI, IDE, ISA, Local Bus, Monitor, PCMCIA, Serial, USB, Video
Number of I/O	-
Voltage - Supply	2.45V ~ 3.6V
Operating Temperature	0°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stpci2heyc

- **PCMCIA interface**
- Support one PCMCIA 68-pin standard PC Card Socket.
- Power Management support.
- Support PCMCIA/ATA specifications.
- Support I/O PC Card with pulse-mode interrupts.

- **USB Interface**
- USB 1.1 compatible.
- Open HCI 1.0 compliant.
- User configurable RootHub.
- Support for both LowSpeed and HighSpeed USB devices.
- No bi-directionnal or Tri-state busses.
- No level sensitive latches.
- System Management Interrupt pin support
- Hooks for legacy device support.

- **Keyboard interface**
- Fully PC/AT+ compatible

- **Mouse interface**
- Fully PS/2 compatible

- **Serial interface**
- 16550 compatible
- Programmable word length, stop bits, parity.
- 16-bit programmable baud rate generator.
- Interrupt generator.
- Loop-back mode.
- 8-bit scratch register.
- Two 16-bit FIFOs.
- Two DMA handshake lines.

Parallel port

- All IEEE Standard 1284 protocols supported: Compatibility, Nibble, Byte, EPP, and ECP modes.
- 16 bytes FIFO for ECP.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports Intel & Cyrix SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.

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PanelLink is a trademark of SiliconImage, Inc

controls for 3.3V suspend with Modem Ring Resume Detection.

The STPC Atlas implements a multi-function parallel port. The standard PC/AT compatible logical address assignments for LPT1, LPT2 and LPT3 are supported. It can be configured for any of the following three modes and supports the IEEE Standard 1284 parallel interface protocol standards, as follows:
- Compatibility Mode (Forward channel, standard)
- Nibble Mode (Reverse channel, PC compatible)
- Byte Mode (Reverse channel, PS/2 compatible)

The General Purpose Input/Output (GPIO) interface provides a 16-bit I/O facility, using 16 dedicated device pins. It is organised using two blocks of 8-bit Registers, one for lines 0 to 7, the other for lines 8 to 15.
Each GPIO port can be configured as an input or an output simply by programming the associated port direction control register. All GPIO ports are configured as inputs at reset, which also latches the input levels into the Strap Registers. The input states of the ports are thus recorded automatically at reset, and this can be used as a strap register anywhere in the system.

1.4. FEATURE MULTIPLEXING

The STPC Atlas BGA package has 516 balls. This however is not sufficient for all of the integrated functions available; some features therefore share the same balls and cannot thus be used at the same time. The STPC Atlas configuration is done by ‘strap options’. This is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the STPC Atlas.

There 3 multiplexed functions are the external ISA bus, the Local Bus and the PCMCIA interface.

1.5. POWER MANAGEMENT

The STPC Atlas core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit (PMU) module controls the power consumption, providing a comprehensive set of features that controls the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides the following hardware structures to assist the software in managing the system power consumption:

- System Activity Detection.

- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power-on state.

- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer periods of time is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate an SMI interrupt to allow the software to bring the system back up to full power-on state. The chip-set supports up to three power down states described above; these correspond to decreasing levels of power savings.

Power down puts the STPC Atlas into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power-down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

1.6. JTAG

JTAG stands for Joint Test Action Group and is the popular name for IEEE Std. 1149.1, Standard Test Access Port and Boundary-Scan Architec-ture. This built-in circuitry is used to assist in the test, maintenance and support of functional circuit blocks. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register so that a component is able to respond to a minimum set of test instructions.

Figure 1-5. Typical Local-Bus-based Application.

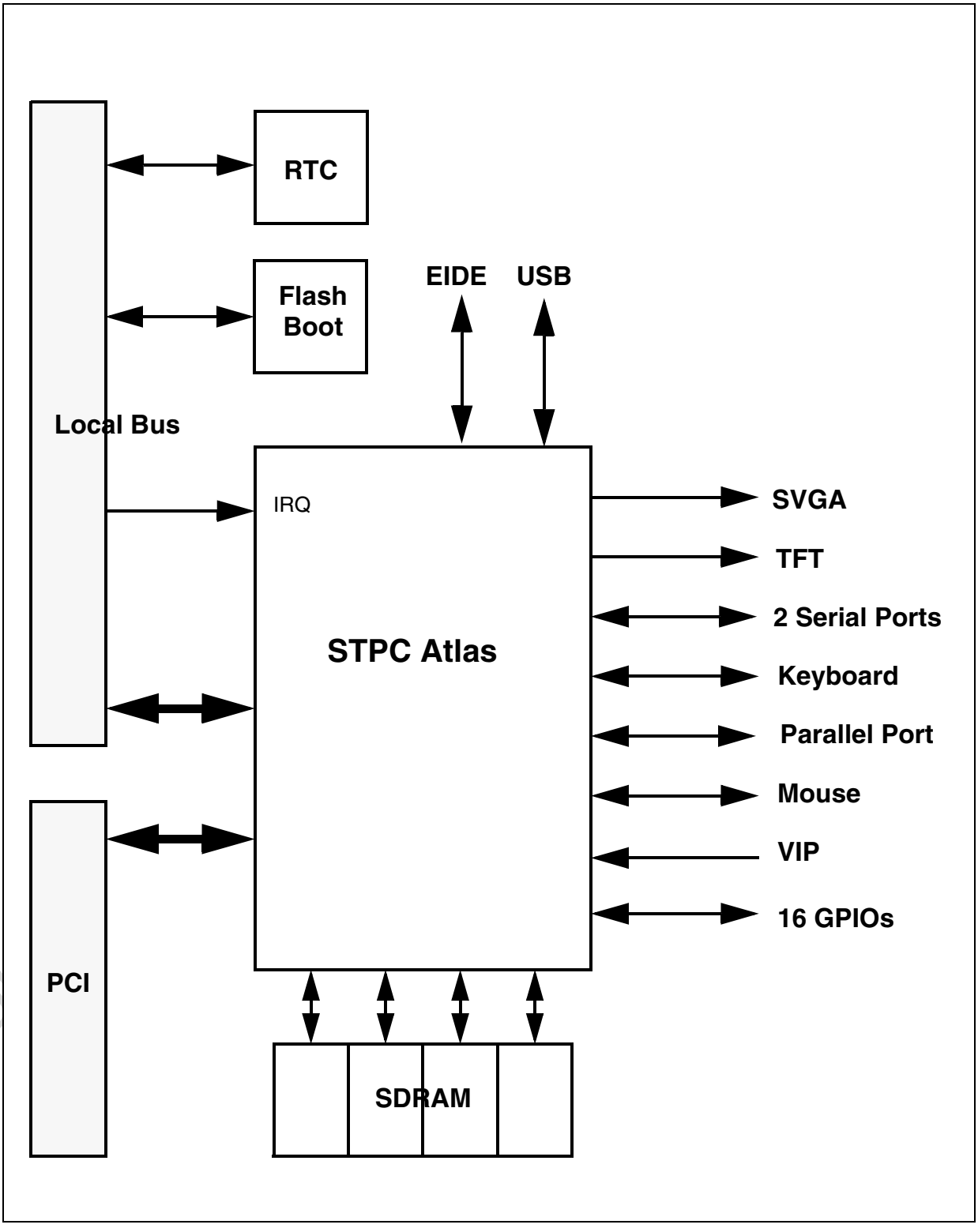


Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
USB INTERFACE				
OC	I	TLCHTU_TC	Over Current Detect	1
USBDPLS[0][1] USBDMNS[0][1]	I/O	USBDS_2V5	Universal Serial Bus Port 0	2
USBDPLS[1][1] USBDMNS[1][1]	I/O	USBDS_2V5	Universal Serial Bus Port 1	2
POWERON[1]	O	BT4CRP	USB power supply lines	1
SERIAL CONTROLLER				
CTS0#, CTS1#	I	TLCHT_FT	Clear to send, MSR[4] status bit	2
DCD0#, DCD1#	I	TLCHT_FT	Data Carrier detect, MSR[7] status bit	2
DSR0#, DSR1#	I	TLCHT_FT	Data set ready, MSR[5] status bit.	2
DTR0#, DTR1#	O	BD4STRP_TC	Data terminal ready, MSR[0] status bit	2
RI0#, RI1#	I	TLCHT_FT	Ring indicator, MSR[6] status bit	2
RTS0#, RTS1#	O	BD4STRP_TC	Request to send, MSR[1] status bit	2
RXD0, RXD1	I	TLCHT_FT	Receive data, Input Serial Input	2
TXD0, TXD1	O	BD4STRP_TC	Transmit data, Serial Output	2
KEYBOARD & MOUSE INTERFACE				
KBCLK	I/O	BD4STRP_TC	Keyboard Clock Line	1
KBDATA	I/O	BD4STRP_TC	Keyboard Data Line	1
MCLK	I/O	BD4STRP_TC	Mouse Clock Line	1
MDATA	I/O	BD4STRP_TC	Mouse Data Line	1
PARALLEL PORT				
PE	I	BD14STARP_FT	Paper End	1
SLCT	I	BD14STARP_FT	SELECT	1
BUSY#	I	BD14STARP_FT	BUSY	1
ERR#	I	BD14STARP_FT	ERROR	1
ACK#	I	BD14STARP_FT	Acknowledge	1
PDIR#	O	BD14STARP_FT	Parallel Device Direction	1
STROBE#	O	BD14STARP_FT	PCS / STROBE#	1
INIT#	O	BD14STARP_FT	INIT	1
AUTOFD#	O	BD14STARP_FT	Automatic Line Feed	1
SLCTIN#	O	BD14STARP_FT	SELECT IN	1
PPD[7:0]	I/O	BD14STARP_FT	Data Bus	8
GPIO SIGNALS				
GPIO[15:0]	I/O	BD4STRP_FT	General Purpose IOs	16
JTAG				
TCLK	I	TLCHT_FT	Test Clock	1
TRST	I	TLCHT_FT	Test Reset	1
TDI	I	TLCHTD_FT	Test Data Input	
TMS	I	TLCHT_FT	Test Mode Set	1
TDO	O	BT8TRP_TC	Test Data output	1
MISCELLANEOUS				
SCAN_ENABLE	I	TLCHTD_FT	Test Pin - Reserved	1
Note[1]; See Table 2-3 for buffer type descriptions				

IOCHRDY *IO Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Atlas. The STPC Atlas monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh. ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Atlas since the access to the system memory can be considerably delayed due to CRT refresh or a write back cycle.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Atlas to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Atlas.
ALE is driven low after reset.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data Byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Atlas generates SMEMR# signal of the ISA bus only when the address is below one MByte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Atlas generates SMEMW# signal of the ISA bus only when the address is below one MByte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Atlas ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Atlas does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Atlas is executed as an extended 8-bit IO cycle.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Atlas performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Atlas performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

GPIOCS# *I/O General Purpose Chip Select 1.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices to power down or any other desired function.

RTCRW# *Real Time Clock RW#.* This pin is used as RTCRW#. This signal is asserted for any I/O write to port 71h.

RTCDS# *Real Time Clock DS*. This pin is used as RTCDS#. This signal is asserted for any I/O read to port 71h. Its polarity complies with the DS pin of the MT48T86 RTC device when configured with Intel timings.

RTCAS *Real time clock address strobe.* This signal is asserted for any I/O write to port 70h.

CTS0#, CTS1# *Input Clear to send.*

RTS0#, RTS1# *Output Request to send.*

DTR0#, DTR1# *Output Data terminal read.*

2.2.14. KEYBOARD/MOUSE INTERFACE

KBCLK, *Keyboard Clock line.* Keyboard data is latched by the controller on each negative clock edge produced on this pin. The keyboard can be disabled by pulling this pin low by software control.

KBDATA, *Keyboard Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to KBCLK.

MCLK, *Mouse Clock line.* Mouse data is latched by the controller on each negative clock edge produced on this pin. The mouse can be disabled by pulling this pin low by software control.

MDATA, *Mouse Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to MCLK.

2.2.15. PARALLEL PORT

PE *Paper End.* Input status signal from printer.

SLCT *Printer Select.* Printer selected input.

BUSY# *Printer Busy*.
Input status signal from printer.

ERR# *Error*. Input status signal from printer.

ACK# *Acknowledge.*
Input status signal from printer.

PDDIR# *Parallel Device Direction.*
Bidirectional control line output.

STROBE# *PCS/Strobe#.*
Data transfer strobe line to printer.

INIT# *Initialize Printer.* This output sends an initialize command to the connected printer.

AUTOFD# *Automatic Line feed.* This output sends a command to the connected printer to automatically generate line feed on received carriage returns.

SLCTIN# *Select In.* Printer select output.

PPD[7-0] *Parallel Port Data Lines* Data transfer lines to printer. Bidirectional depending on modes.

2.2.16. MISCELLANEOUS

SPKRD *Speaker Drive.* This is the output to the speaker and is the AND of the counter 2 output with bit 1 of Port 61h and drives an external speaker driver. This output should be connected to a 7407 type high voltage driver.

SCAN_ENABLE *Reserved*. This pin is reserved for Test and Miscellaneous functions. It has to be set to '0' or connected to ground in normal operation.

2.2.17. **COL_SEL** *Colour Select. JTAG INTERFACE*

TCLK *Test clock*

TDI *Test data input*

TMS *Test mode input*

TDO *Test data output*

TRST Test reset input

2.3 SIGNAL DETAIL

The muxing between ISA, LOCAL BUS and PCMCIA is performed by external strap options.

The resulting interface is then dynamically muxed with the IDE Interface.

Table 2-4. Multiplexed Signals (on the same pin)

IDE Pin Name	ISA Pin Name	PCMCIA Pin Names	Local Bus Pin Name
DIORDY	IOCHRDY	-	
DA[2]	LA[19]	*= 0*	
DA[1:0]	LA[18:17]	A[25:24]	
SCS3,SCS1	LA[23:22]	A[23:22]	
PCS3,PCS1	LA[21:20]	A[21:20]	
DD[15]	RMRTCCS#	ROMCS#	
DD[14]	KBCS#	*Hi-Z*	
DD[13:12]	RTCRW#, RTCDS#	*Hi-Z*	
DD[11:0]	SA[19:8]	A[19:8]	

Table 2-5. Signal value on Reset

Signal Name	SYSRSTI# active	SYSRSTI# inactive SYSRSTO# active	release of SYSRSTO#
CS#[0]	High		SDRAM init sequence: Write Cycles
MA[10:0], BA[0]	0x00		
RAS#[1:0], CAS#[1:0]	High		
MWE#, DQM[7:0]	High		
MD[63:0]	Input		
PCI INTERFACE			
AD[31:0]	0x0000		First prefetch cycles when not in Local Bus mode.
CBE[3:0], PAR	Low		
FRAME#, TRDY#, IRDY#	Input		
STOP#, DEVSEL#	Input		
PERR#, SERR#	Input		
PCI_GNT#[2:0]	High		
ISA BUS INTERFACE			
ISAOE#	High		Low
RMRTCCS#	Hi-Z		First prefetch cycles when in ISA or PCMCIA mode. Address start is 0xFFFFF0
LA[23:17]	Unknown	0x00	
SA[19:0]	0xFFFXX	0xFFF03	
SD[15:0]	Unknown	0xFF	
BHE#, MEMR#	Unknown	High	
MEMW#, SMEMR#, SMEMW#, IOR#, IOW#	Unknown	High	
REF#	Unknown	High	
ALE, AEN	Low		
DACK_ENC[2:0]	Input		0x04
TC	Input		Low
GPIOCS#	Hi-Z		High
RTCDS#, RTCRW#, KBCS#	Hi-Z		
RTCAS	Unknown	Low	
PCMCIA INTERFACE			
RESET	Unknown	High	
A[23:0]	Unknown	0x00	First prefetch cycles using RMRTCCS#
D[15:0]	Unknown	0xFF	
IORD#, IOWR#, OE#	Unknown	High	
WE#, REG#	High		
CE2#, CE1#, VCC5_EN, VCC3_EN	High		
VPP_PGM, VPP_VCC	Low		
LOCAL BUS INTERFACE			
PA[24:0]	Unknown		First prefetch cycles
PD[15:0]	Unknown	0xFF	
PRD#	Unknown	High	
PBE#[1:0], FCS0#, FCS_0H#	High		
FCS_0L#, FCS1#, FCS_1H#, FCS_1L#	High		
PWR#, IOCS#[7:0]	High		
IDE CONTROLLER			
DD[15:0]	0xFF		
DA[2:0]	Unknown	Low	
PCS1, PCS3, SCS1, SCS3	Unknown	Low	
PDACK#, SDACK#	High		
PDIOR#, PDIOW#, SDIOR#, SDIOW#	High		
VGA CONTROLLER			
RED, GREEN, BLUE	Black		
VSYNC, HSYNC	Low		

Table 2-6. Pinout

Pin#	Pin Name
Y3	CS#[2]/MA[11]
Y4	CS#[3]/MA[12]/BA[1]
T2	DQM[0]
T4	DQM[1]
Y5	DQM[2]
AA2	DQM[3]
T3	DQM[4]
T5	DQM[5]
AA1	DQM[6]
AA3	DQM[7]
B3	AD[0]
A3	AD[1]
C4	AD[2]
B4	AD[3]
A4	AD[4]
D5	AD[5]
C5	AD[6]
B5	AD[7]
A5	AD[8]
D6	AD[9]
C6	AD[10]
B6	AD[11]
A6	AD[12]
E7	AD[13]
D7	AD[14]
C7	AD[15]
A9	AD[16]
E10	AD[17]
C10	AD[18]
B10	AD[19]
A10	AD[20]
E11	AD[21]
D11	AD[22]
C11	AD[23]
A11	AD[24]
E12	AD[25]
D12	AD[26]
C12	AD[27]
B12	AD[28]
A12	AD[29]
E13	AD[30]
D13	AD[31]
E6	CBE[0]
B7	CBE[1]
B9	CBE[2]
B11	CBE[3]
C9	FRAME#
E9	TRDY#
D9	IRDY#
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
B8	STOP#
A8	DEVSEL#
A7	PAR
D8	PERR#
E8	SERR#
C8	LOCK#
C14	PCI_REQ#[0]
B14	PCI_REQ#[1]
A14	PCI_REQ#[2]
A13	PCI_GNT#[0]
B13	PCI_GNT#[1]
C13	PCI_GNT#[2]
C20	LA[17][1]
B21	LA[18][1]
B20	LA[19][1]
E19	LA[20][1]
E18	LA[21][1]
C21	LA[22][1]
D19	LA[23][1]
P22	SA[0][1]
P23	SA[1][1]
P24	SA[2][1]
P25	SA[3][1]
P26	SA[4][1]
N26	SA[5][1]
N25	SA[6][1]
N24	SA[7][1]
N23	SA[8][1]
N22	SA[9][1]
M26	SA[10][1]
M25	SA[11][1]
M24	SA[12][1]
M23	SA[13][1]
M22	SA[14][1]
L26	SA[15][1]
L25	SA[16][1]
L24	SA[17][1]
L23	SA[18][1]
L22	SA[19][1]
K24	SD[0][1]
J26	SD[1][1]
J25	SD[2][1]
J24	SD[3][1]
K23	SD[4][1]
K22	SD[5][1]
H26	SD[6][1]
H25	SD[7][1]
H24	SD[8][1]
G26	SD[9][1]
Note[1]; This signal is multiplexed see Table 2-4	

3.1 STRAP OPTION REGISTER DESCRIPTION

3.1.1. STRAP REGISTER 0

This register is read only.

STRAP0 Access = 0022h/0023h Regoffset =04Ah

7	6	5	4	3	2	1	0
MD[7]	MD[6]	MD[9]	MD[8]	RSV	MD[5]	MD[4]	MD[17]
This register defaults to the values sampled on the MD pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-6	MD[7:6]	PCICLK PLL set-up: The value sampled on MD[7:6] controls the PCICLK PLL programming according to the PCICLK frequency. MD7 MD6 0 0 PCICLK frequency between 16 & 32 MHz 0 1 PCICLK frequency between 32 & 64 MHz 1 X Reserved
Bits 5-4	MD[9:8]	Mode selection: MD9 MD8 0 0 ISA mode: ISA enabled, PCMCIA & Local Bus disabled 0 1 PCMCIA mode: PCMCIA enabled, ISA & Local Bus disabled 1 0 Local Bus mode: Local Bus enabled, ISA & PCMCIA disabled 1 1 Reserved
Bit 3	Rsv	Reserved
Bit 2	MD[5]	Host Memory synchronization. This bit reflects the value sampled on [MD5] and controls the MCLK/HCLK synchronization. 0: MCLK and HCLK not synchronized 1: MCLK and HCLK synchronized.
Bits 1-0	MD[4], MD[17]	PCICLK division: These bits reflect the values sampled on [MD4] and MD[17] to select the PCICLK frequency. MD4 MD17 0 X PCI Clock output = HCLK / 4 1 0 PCI Clock output = HCLK / 3 1 1 PCI Clock output = HCLK / 2

4.5. AC CHARACTERISTICS

This section lists the AC characteristics of the STPC interfaces including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 and Figure 4-2. The rising clock edge reference level VREF and other reference levels are shown in Table 4-9 below. Input or output signals must cross these levels during testing.

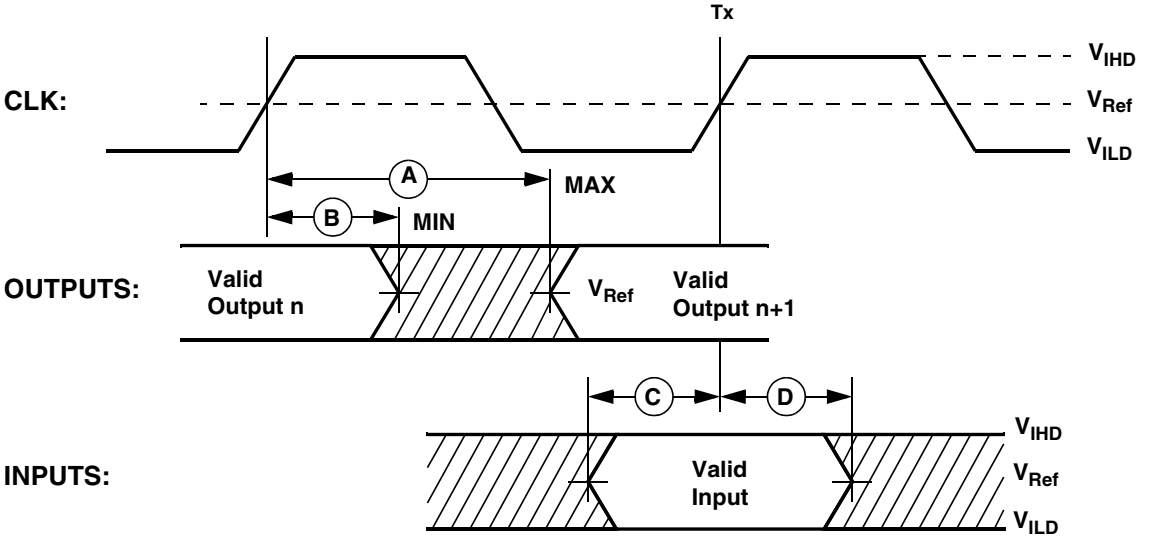
Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-9. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	2.5	V
V_{ILD}	0.0	V

Note: Refer to Figure 4-1.

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics



LEGEND:
A - Maximum Output Delay Specification
B - Minimum Output Delay Specification
C - Minimum Input Setup Specification
D - Minimum Input Hold Specification

4.5.2 RESET SEQUENCE

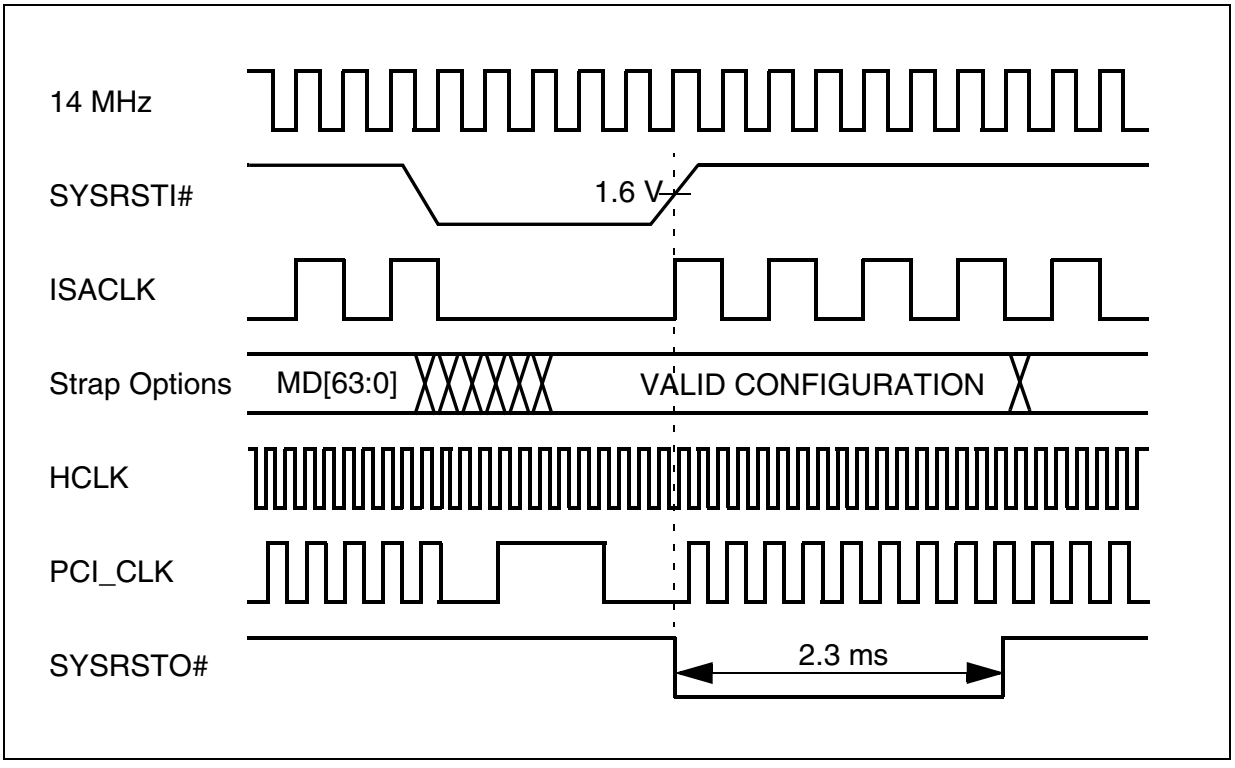
Figure 4-4 describes the reset sequence of the STPC, also called warm reset.

The constraints on the strap options and the bus activities are the same as for the cold reset.
The SYSRSTI# pulse duration must be long enough to have all the strap options stabilized and must be adjusted depending on resistor values.

It is mandatory to have a clean reset pulse without glitches as the STPC could then sample invalid strap option setting and enter into an unpredictable mode.

While SYSRSTI# is active, the PCI clock PLL runs in open loop mode at a speed of few 100's KHz.

Figure 4-4. Reset timing diagram



4.5.3. SDRAM INTERFACE

Figure 4-5, Table 4-10, Table 4-11 lists the AC characteristics of the SDRAM interface. The MCLKx clocks are the input clock of the SDRAM devices.

Figure 4-5. SDRAM Timing Diagram

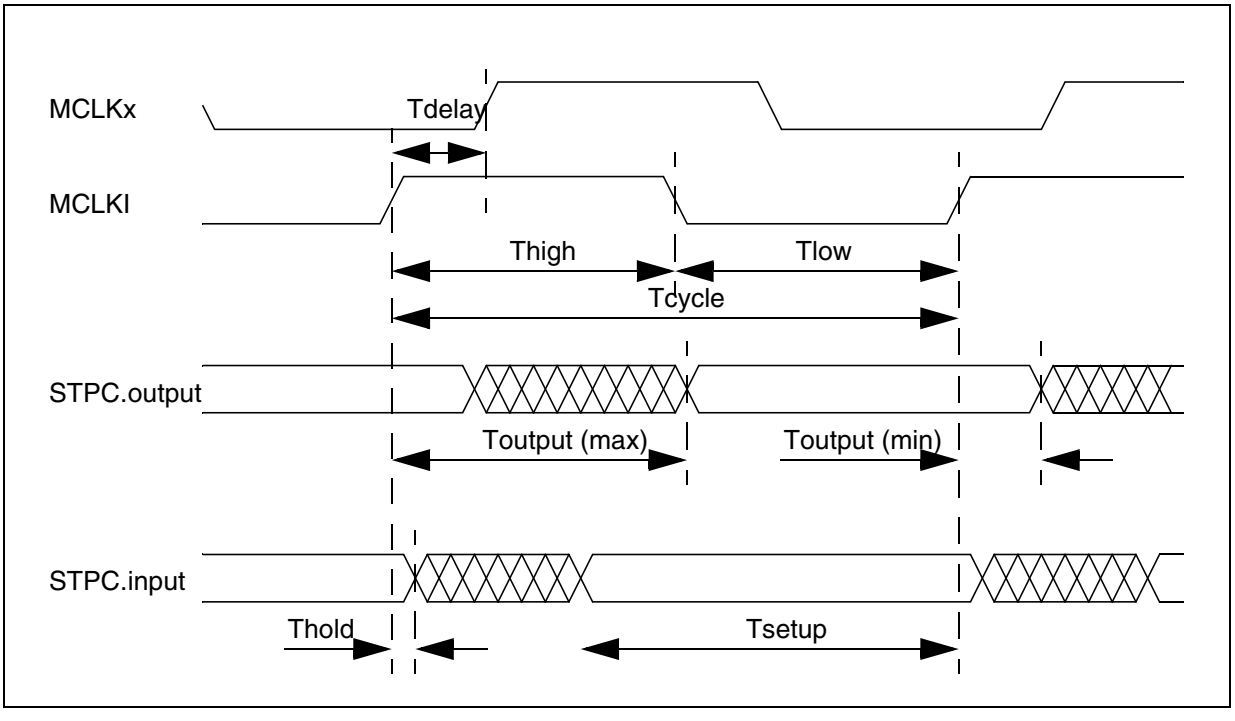


Table 4-10. SDRAM Bus AC Timings - Commercial Temperature Range

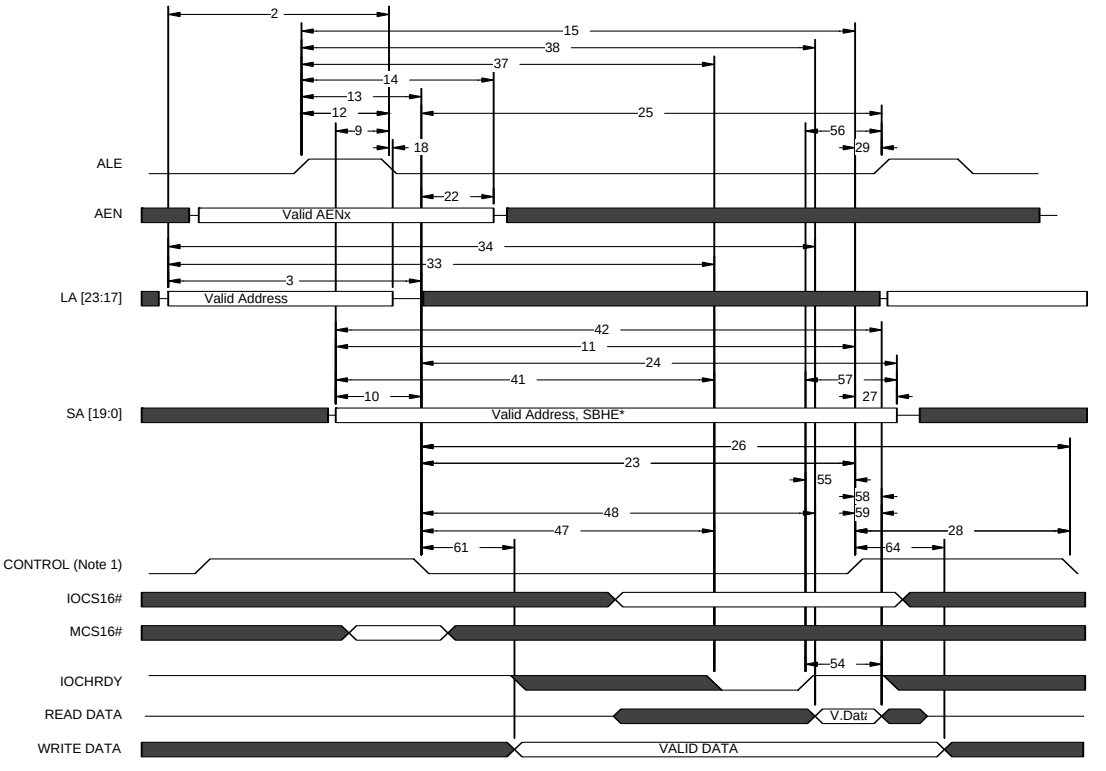
Name	Parameter	Min	Typ	Max	Unit
Tcycle	MCLKI Cycle Time	11			ns
Thigh	MCLKI High Time	4			ns
Tlow	MCLKI Low Time	4			ns
	MCLKI Rising Time			1	ns
	MCLKI Falling Time			1	ns
Tdelay	MCLKx to MCLKI delay	0.5	1	1.5	ns
Toutput	MCLKI to RAS# Valid	1.6		5.2	ns
	MCLKI to CAS# Valid	1.6		5.2	ns
	MCLKI to CS# Valid	1.6		5.2	ns
	MCLKI to DQM[ ] Outputs Valid	1.35		5.2	ns
	MCLKI to MD[ ] Outputs Valid	1.35		5.2	ns
	MCLKI to MA[ ] Outputs Valid	1.6		5.2	ns
	MCLKI to MWE# Valid	1.6		5.2	ns
Tsetup	MD[63:0] setup to MCKLI	4.7			ns
Thold	MD[63:0] hold from MCKLI	-0.36		2.3	ns
Note: These timings are for a load of 50pF, part running at 100MHz and ReadCLK activated and set to 0					

The PC100 memory is recommended to reach 90MHz operation.

4.5.6 ISA INTERFACE AC TIMING CHARACTERISTICS

Figure 4-8 and Table 4-14 list the AC characteristics of the ISA interface.

Figure 4-8. ISA Cycle (ref Table 4-14.)



Note 1: Stands for SMEMR#, SMEMW#, MEMR#, MEMW#, IOR# & IOW#.
The clock has not been represented as it is dependent on the ISA Slave mode.

Table 4-14. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
2	LA[23:17] valid before ALE# negated	5T		Cycles
3	**LA[23:17] valid before MEMR#, MEMW# asserted**			
3a	Memory access to 16-bit ISA Slave	5T		Cycles
3b	Memory access to 8-bit ISA Slave	5T		Cycles
9	SA[19:0] & SBHE valid before ALE# negated	1T		Cycles
10	**SA[19:0] & SBHE valid before MEMR#, MEMW# asserted**			
10a	Memory access to 16-bit ISA Slave	2T		Cycles
10b	Memory access to 8-bit ISA Slave	2T		Cycles
10	**SA[19:0] & SHBE valid before SMEMR#, SMEMW# asserted**			
Note: The signal numbering refers to Figure 4-8				

Table 4-14. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	61e	I/O access to 16-bit ISA Slave	2T		Cycles
	61f	I/O access to 8-bit ISA Slave	2T		Cycles
64a	MEMW# negated to write data invalid - 16-bit		1T		Cycles
64b	MEMW# negated to write data invalid - 8-bit		1T		Cycles
64c	SMEMW# negated to write data invalid - 16-bit		1T		Cycles
64d	SMEMW# negated to write data invalid - 8-bit		1T		Cycles
64e	IOW# negated to write data invalid		1T		Cycles
64f	MEMW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master		1T		Cycles
64g	IOW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master		1T		Cycles
Note: The signal numbering refers to Figure 4-8					

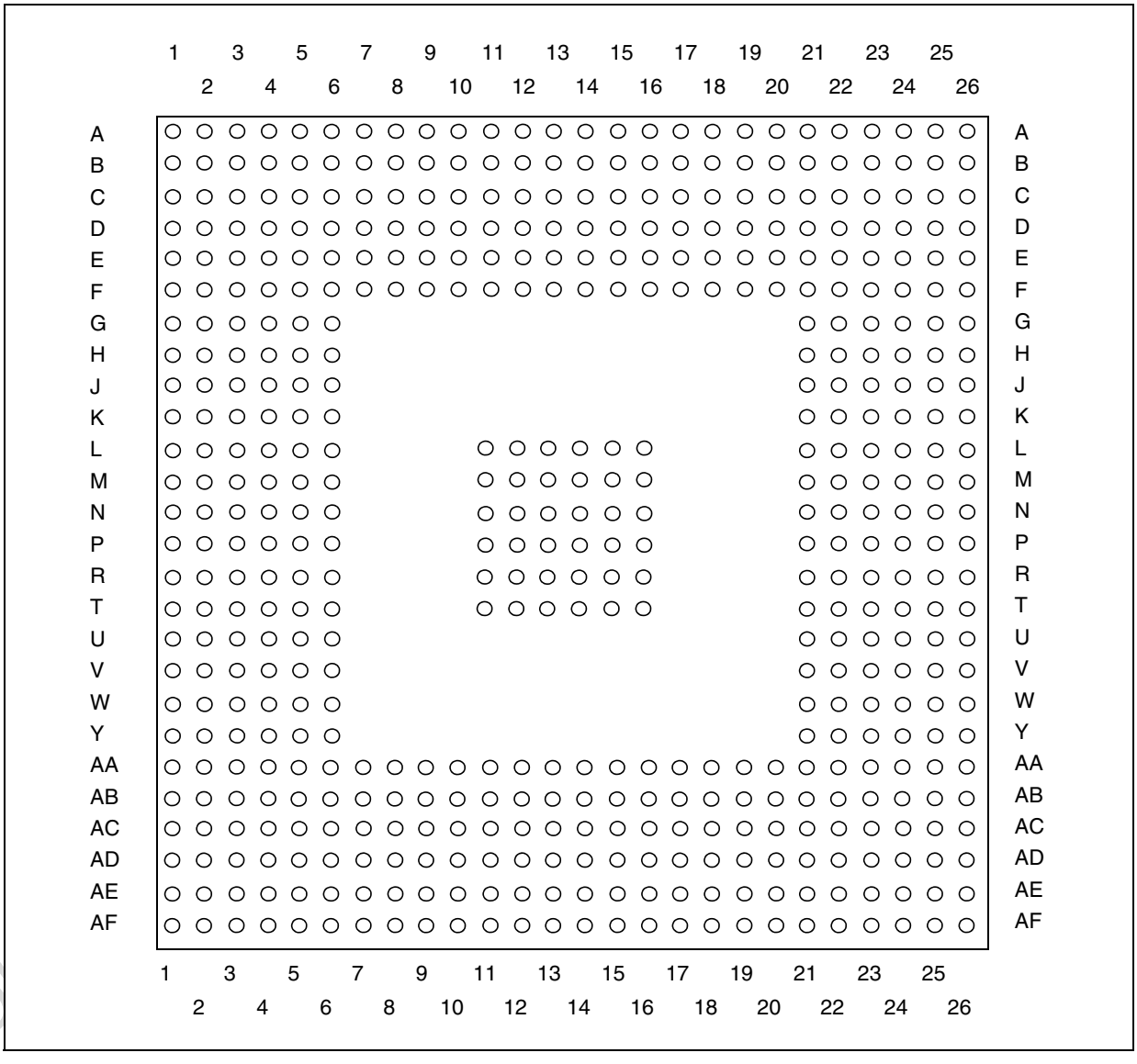
5 MECHANICAL DATA

5.1. 516-PIN PACKAGE DIMENSION

The pin numbering for the STPC 516-pin Plastic BGA package is shown in Figure 5-1.

Dimensions are shown in Figure 5-2, Table 5-1. and Figure 5-3, Table 5-2..

Figure 5-1. 516-Pin PBGA Package - Top View

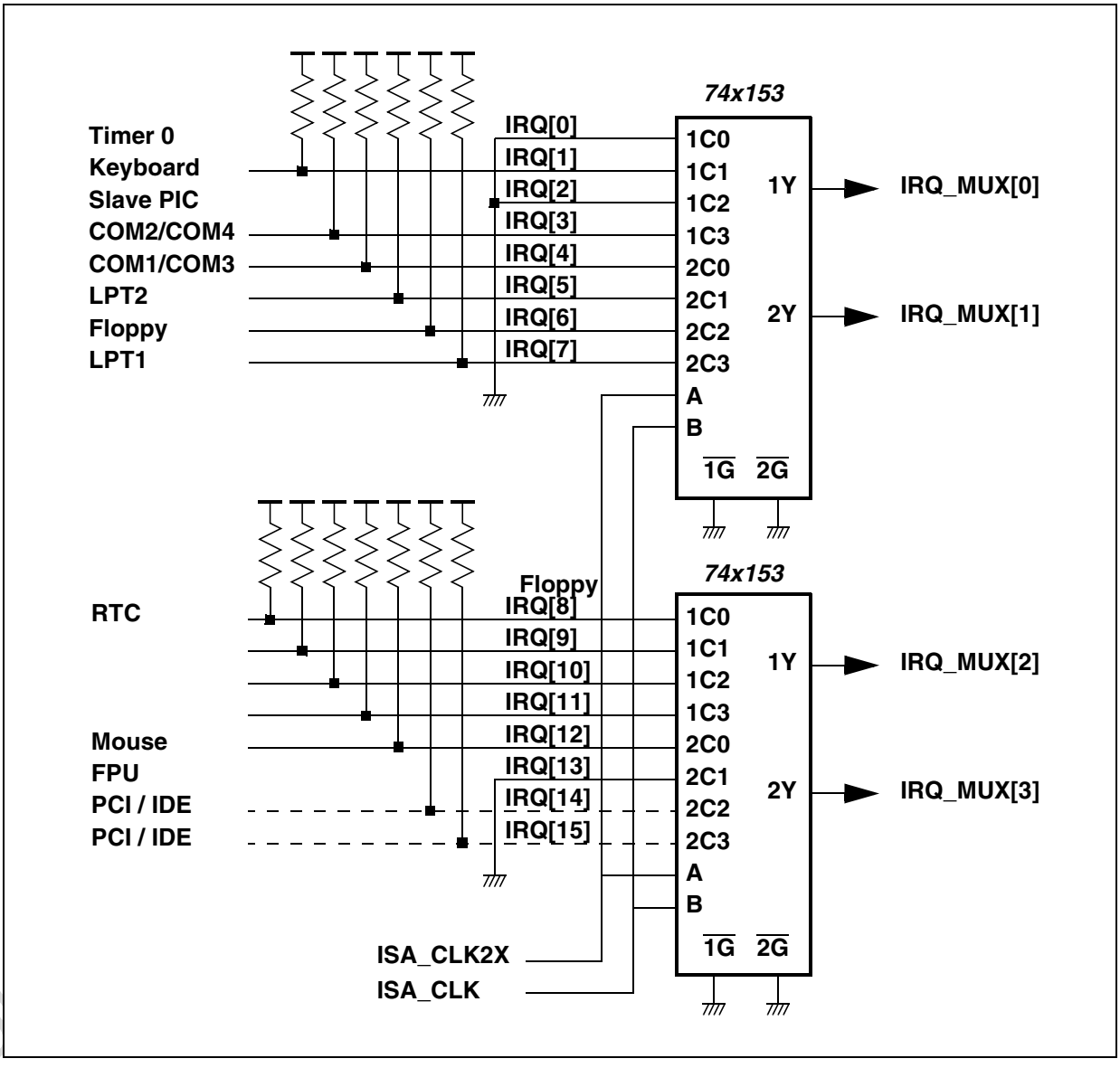


6.3.6. IPC

Most of the IPC signals are multiplexed: Interrupt inputs, DMA Request inputs, DMA Acknowledge outputs. The figure below describes a complete implementation of the IRQ[15:0] time-multiplexing.

When an interrupt line is used internally, the corresponding input can be grounded. In most of the embedded designs, only few interrupts lines are necessary and the glue logic can be simplified.

Figure 6-11. Typical IRQ multiplexing



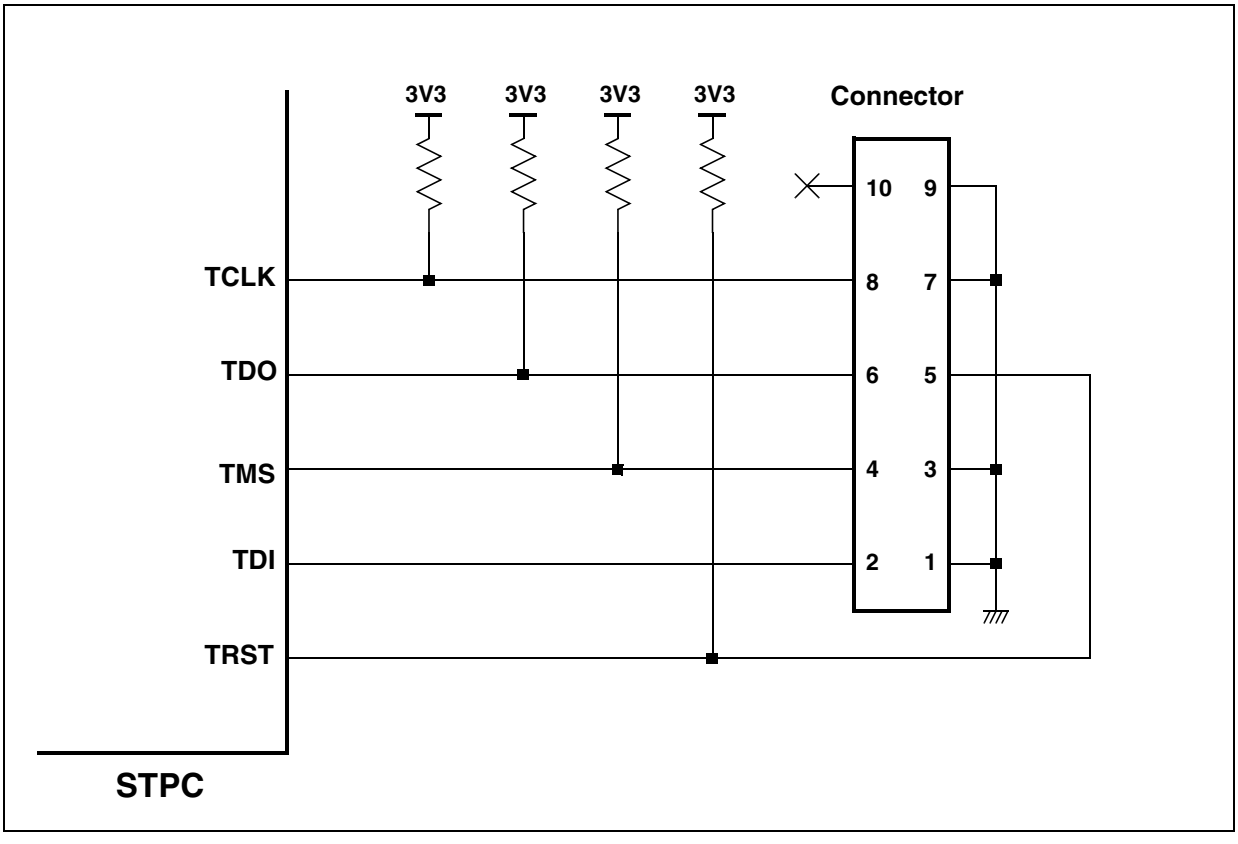
When the interface is integrated into the STPC, the corresponding interrupt line can be grounded as it is connected internally.

For example, if the integrated IDE controller is activated, the IRQ[14] and IRQ[15] inputs can be grounded.

6.3.13. JTAG INTERFACE

The STPC integrates a JTAG interface for scan-chain and on-board testing. The only external device needed are the pull up resistors. Figure 6-19 describes a typical implementation using these devices.

Figure 6-19. Typical JTAG implementation



6.4. PLACE AND ROUTE RECOMMENDATIONS

6.4.1. GENERAL RECOMMENDATIONS

Some STPC Interfaces run at high speed and need to be carefully routed or even shielded like:

1) Memory Interface
2) PCI bus
3) Graphics and video interfaces
4) 14 MHz oscillator stage

All clock signals have to be routed first and shielded for speeds of 27MHz or higher. The high speed signals follow the same constraints, as for the memory and PCI control signals.

The next interfaces to be routed are Memory, PCI, and Video/graphics.

All the analog noise-sensitive signals have to be routed in a separate area and hence can be routed indepedently.

6.4.2. PLL DEFINITION AND IMPLIMENTATION

PLLs are analog cells which supply the internal STPC Clocks. To get the cleanest clock, the jitter on the power supply must be reduced as much as possible. This will result in a more stable system.

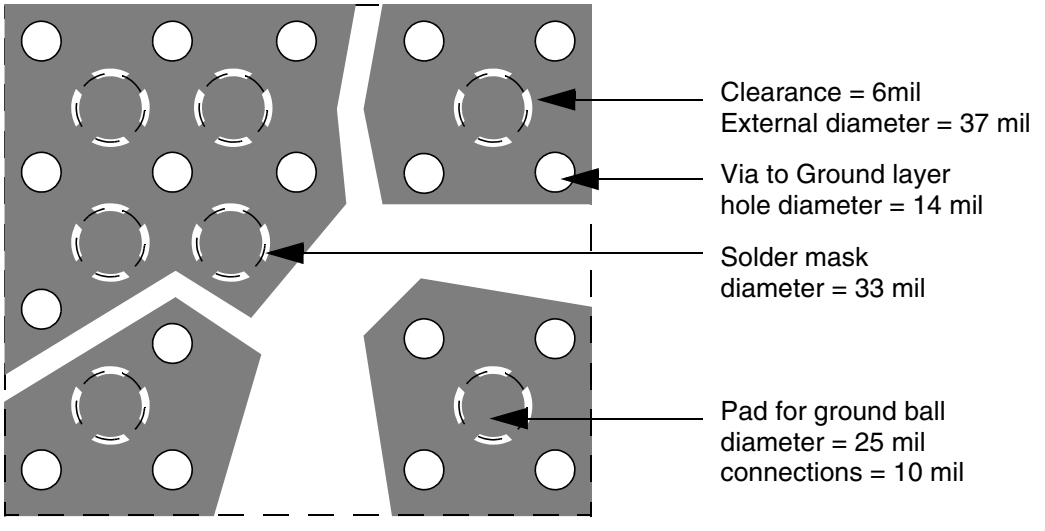
Each of the integrated PLL has a dedicated power pin so a single power plane for all of these PLLs, or one wire for each, or any solution in between which help the layout of the board can be used.

Powering these pins with one Ferrite + capacitances is enough. We recommend at least 2 capacitances: one 'big' (few uF) for power storage, and one or 2 smalls (100nF + 1nF) for noise filtering.

To avoid solder wicking over to the via pads during soldering, it is important to have a solder mask of 4 mil around the pad (NSMD pad). This gives a diameter of 33 mil for a 25 mil ground pad.

To obtain the optimum ground layout, place the vias directly under the ball pads. In this case no local board distortion is tolerated.

Figure 6-34. Optimum Layout for Central Ground Ball - top layer



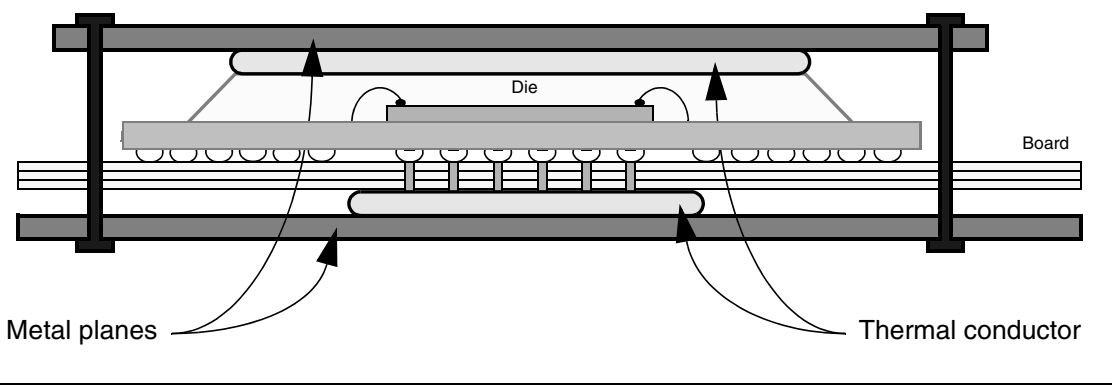
6.5.2.3. Heat dissipation

The thickness of the copper on PCB layers is typically 34 µm for external layers and 17 µm for internal layers. This means that thermal dissipation is not good; high board temperatures are concentrated around the devices and these fall quickly with increased distance.

Where possible, place a metal layer inside the PCB; this improves dramatically the spread of heat and hence the thermal dissipation of the board.

The possibility of using the whole system box for thermal dissipation is very useful in cases of high internal temperatures and low outside temperatures. Bottom side of the PBGA should be thermally connected to the metal chassis in order to propagate the heat flow through the metal. Thermally connecting also the top side will improve furthermore the heat dissipation. Figure 6-35 illustrates such an implementation.

Figure 6-35. Use of Metal Plate for Thermal Dissipation



6.6.3.3. POST code

Once the 16 first bytes are fetched and decoded, the CPU core continue its execution depending on the content of these first data. Usually, it corresponds to a JUMP instruction and the code fetching continues, generating read cycles on the ISA bus.

Most of the BIOS and boot loaders are reading the content of the flash, decompressing it in SDRAM, and then continue the execution by jumping to the entry point in RAM. This boot process ends with a JUMP to the entry point of the OS launcher.
These various steps of the booting sequence are codified by the so-called POST codes (Power-On Self-Test). A 8-bit code is written to the port 80H at the beginning of each stage of the booting process (I/O write to address 0080H) and can be displayed on two 7-segment display, enabling a fast visual check of the booting completion level.
Usually, the last POST code is 0x00 and corresponds to the jump into the OS launcher.

When the execution fails or hangs, the lastest written code stays visible on that display, indicating either the piece of code to analyse, either the area of the hardware not working properly.

6.6.4. LOCAL BUS MODE

As the Local Bus controller is located into the Host interface, there is no access to the cycles on the PCI, reducing the amount of signals to check.

6.6.4.1. First code fetches

When booting on the Local Bus, the key signal to check at the very beginning is FCS0#. This signal is a Chip Select for the boot flash and should toggle together with PRD# to fetch the first 16 bytes of code. This corresponds to the loading of the first line of the CPU cache.
In case FCS0# does not toggle, then one of the previous steps has not been done properly, like HCLK speed and CPU clock multiplier (x1, x2).

6.6.4.2. Boot Flash size

The Local Bus support 8-bit and 16-bit boot memory devices only.

6.6.4.3. POST code

Like in ISA mode, POST codes can be implemented on the Local Bus. The difference is that an IOCS# must be programmed at I/O address 80H prior to writing these code, the POST display being connected to this IOCS# and to the lower 8 bits of the bus.

6.6.5. SUMMARY

Here is a check-list for the STPC board debug from power-on to CPU execution.

For each step, in case of failure, verify first the corresponding balls of the STPC:
- check if the voltage or activity is correct
- search for potential shortcuts.

For troubleshooting in steps 5 to 10, verify the related strap options:
- value & connection. Refer to Section 3.
- see Figure 4-3 for timing constraints

Steps 8a and 9a are for debug in ISA mode while steps 8b and 9b are for Local Bus mode.

6.6.6. PCMCIA mode

As the STPC uses the RMRTCCS# signal for booting in that mode, the methodology is the same as for the ISA bus. The PCMCIA cards being 3.3V or 5V, the boot flash device must be 5V tolerant when directly connected on the address and data busses. An other solution is to isolate the flash from the PCMCIA lines using 5V tolerant LVTTL buffers.

	Check:	How?	Troubleshooting
1	Power supplies	Verify that voltage is within specs: - this must include HF & LF noise - avoid full range sweep Refer to Table 4-1 for values	Measure voltage near STPC balls: - use very low GND connection. Add some decoupling capacitor: - the smallest, the nearest to STPC balls.
2	14.318 MHz	Verify OSC14M speed	The 2 capacitors used with the quartz must match with the capacitance of the crystal. Try other values.
3	SYSRSTI# (Power Good)	Measure SYSRSTI# of STPC See Figure 4-3 for waveforms.	Verify reset generation circuit: - device reference - components value