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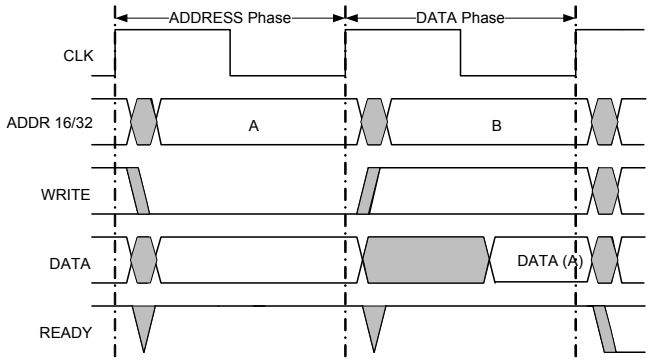
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

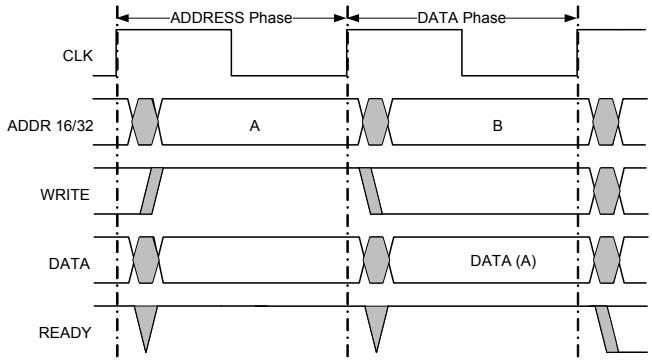
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5666axi-lp004

Figure 4-2. DMA Timing Diagram



Basic DMA Read Transfer without wait states



Basic DMA Write Transfer without wait states

4.3.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.3.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.3.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.3.4.5 Indexed DMA

In an indexed DMA case, an external master requires access to locations on the system bus as if those locations were shared memory. As an example, a peripheral may be configured as an SPI or I^2C slave where an address is received by the external master. That address becomes an index or offset into the internal system bus memory space. This is accomplished with an initial “address fetch” TD that reads the target address location from the peripheral and writes that value into a subsequent TD in the chain. This modifies the TD chain on the fly. When the “address fetch” TD completes it moves on to the next TD, which has the new address information embedded in it. This TD then carries out the data transfer with the address location required by the external master.

4.3.4.6 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.3.4.7 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.3.4.8 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

The central timewheel can be programmed to wake the system periodically and optionally issue an interrupt. This enables flexible, periodic wakeups from low power modes or coarse timing applications. Systems that require accurate timing should use Real Time Clock capability instead of the central timewheel.

The 100-kHz clock (CLK100K) can be used as a low power system clock to run the CPU. It can also generate time intervals using the fast timewheel.

The fast timewheel is a 5-bit counter, clocked by the 100-kHz clock. It features programmable settings and automatically resets when the terminal count is reached. An optional interrupt can be generated each time the terminal count is reached. This enables flexible, periodic interrupts of the CPU at a higher rate than is allowed using the central timewheel.

The 33 kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768 kHz ECO clock with no need for a crystal.

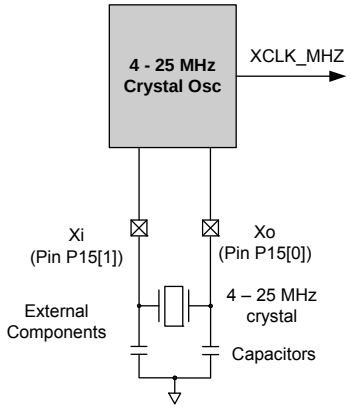
6.1.2 External Oscillators

Figure 6-1 shows that there are two external oscillators. They can be routed directly or divided. The direct routes may not have a 50% duty cycle. Divided clocks have a 50% duty cycle.

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports a wide variety of crystal types, in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see Phase-Locked Loop on page 24). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

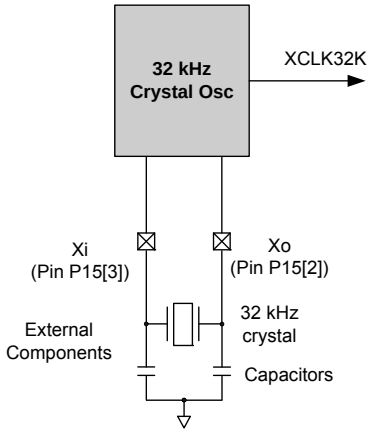


6.1.2.2 32.768 kHz ECO

The 32.768 kHz External Crystal Oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768 kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the Real Time Clock (RTC). The RTC uses a 1 second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the “GPIO” section on page 75.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

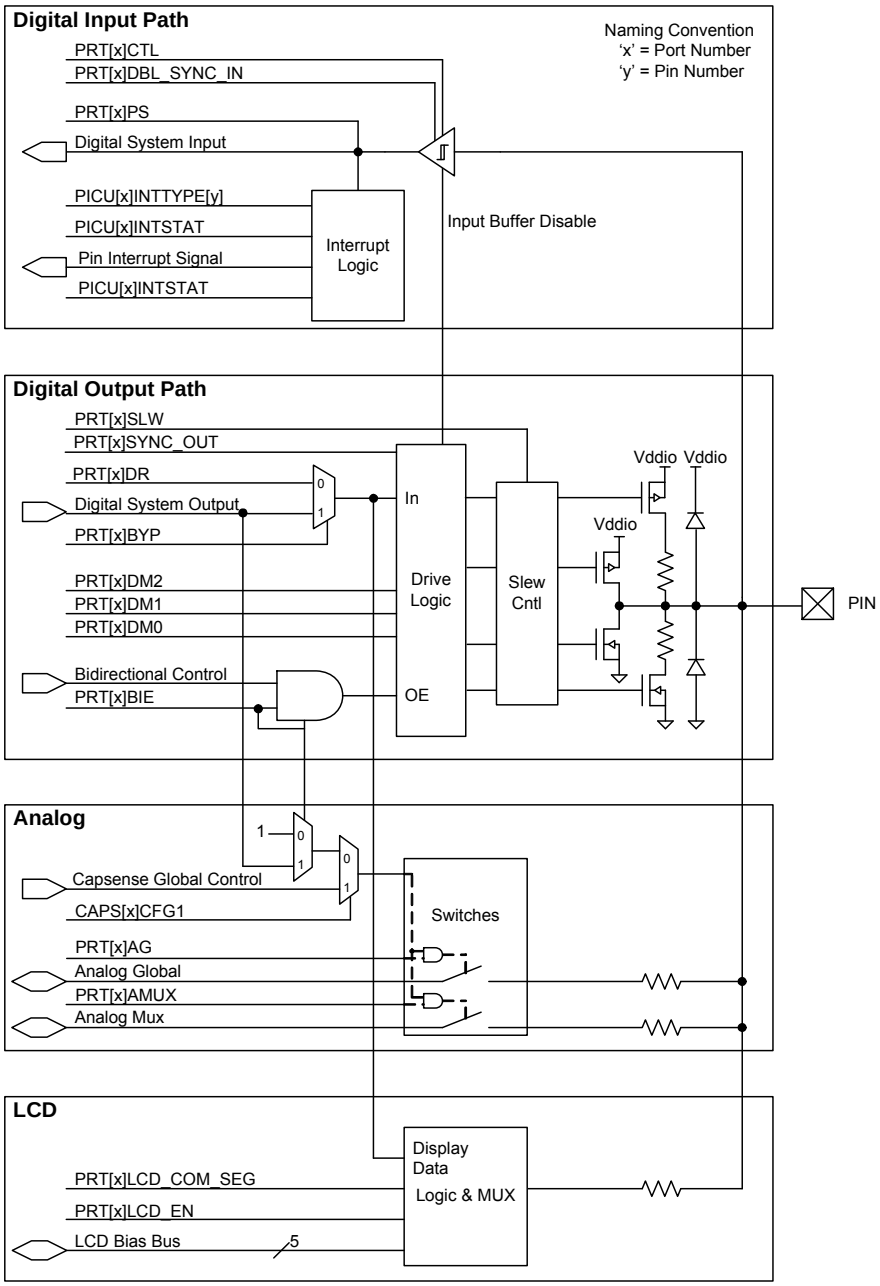
While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design’s requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus Clock 16-bit divider uses the system clock to generate the system’s bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design’s requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function Timer/Counter/PWMs can also generate clocks.

Figure 6-9. GPIO Block Diagram



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in Figure 6-10 on page 34 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating VDD.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's VIH and VIL levels are determined by the associated VDDIO supply pin.

The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See Figure 6-12 for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull down or pull up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low Power Functionality

In all low power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in "Pinouts" on page 6. The special features are:

- Digital
  - 4 to 25 MHz crystal oscillator
  - 32.768 kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - TRACEPORT interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all pins for board level test.

7. Digital Subsystem

The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- Universal Digital Blocks (UDB) - These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal Digital Block array - UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.

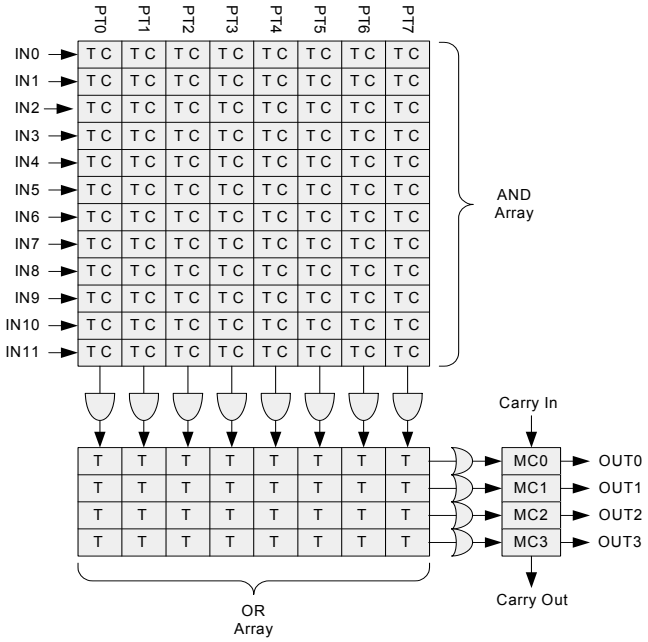
The main component blocks of the UDB are:

- PLD blocks - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module - This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, look up tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

8.1 Analog Routing

The PSoC 5LP family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs.

8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 Analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- 8 Analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the PSoC 5LP family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in PSoC 5LP, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2.

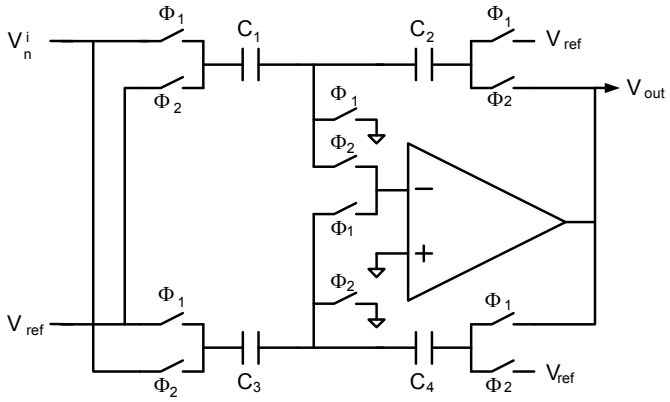
Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in PSoC 5LP, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

8.12 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I). PSoC Creator offers a sample and hold component to support this function.

Figure 8-14. Sample and Hold Topology (Φ1 and Φ2 are opposite phases of a clock)



8.12.1 Down Mixer

The S+H can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.12.2 First Order Modulator - SC Mode

A first order modulator is constructed by placing the switched capacitor block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement

9. Programming, Debug Interfaces, Resources

The Cortex-M3 has internal debugging components, tightly integrated with the CPU, providing the following features:

- JTAG or SWD access
- Flash Patch and Breakpoint (FPB) block for implementing breakpoints and code patches
- Data Watchpoint and Trigger (DWT) block for implementing watchpoints, trigger resources, and system profiling
- Embedded Trace Macrocell (ETM) for instruction trace
- Instrumentation Trace Macrocell (ITM) for support of printf-style debugging

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Four interfaces are available: JTAG, SWD, SWV, and TRACEPORT. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection. The SWV and TRACEPORT provide trace output from the DWT, ETM, and ITM. TRACEPORT is faster but uses more pins. SWV is slower but uses only one pin.

For more information on PSoC 5 programming, refer to the application note PSoC 5 Device Programming Specifications.

Cortex-M3 debug and trace functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

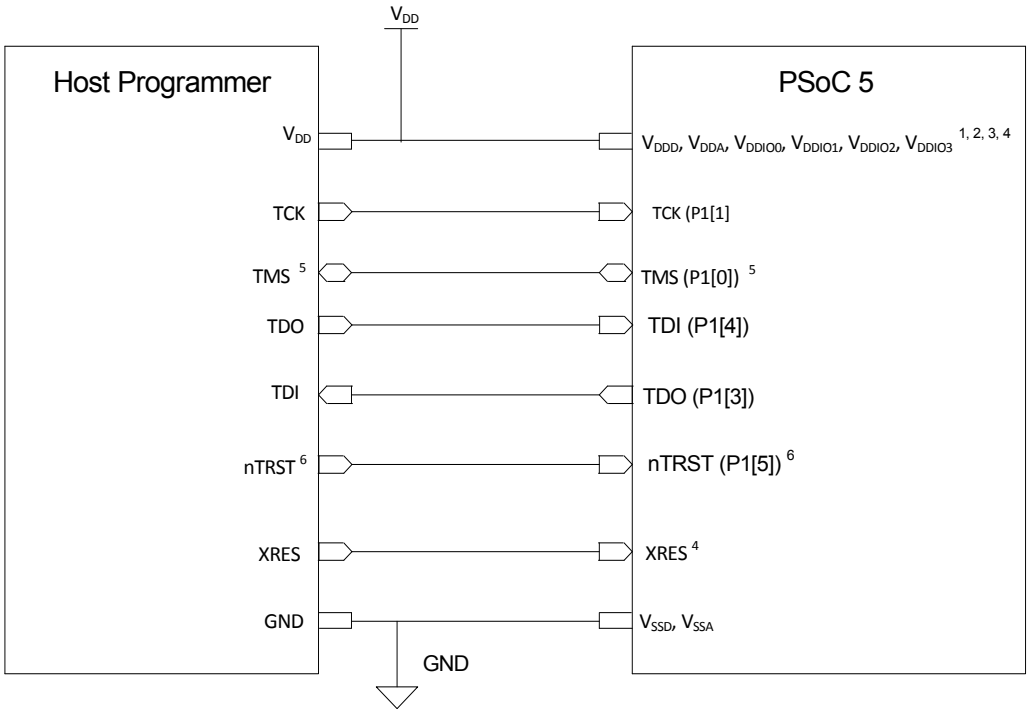
The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All Cortex-M3 debug and trace modules are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables them. Disabling debug and trace features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because the designer then cannot access the device later. Because all programming, debug, and test interfaces are disabled when Device Security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG clock frequency can be up to 12 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers, whichever is least. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as General Purpose I/O (GPIO) instead. The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

Figure 9-1. JTAG Interface Connections between PSoC 5LP and Programmer



[1] The voltage levels of Host Programmer and the PSoC 5 voltage domains involved in Programming should be same. The Port 1 JTAG pins and XRES pin are powered by V_{DDIO1}. So, V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD}. Rest of PSoC 5 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 5.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS,TCK,TDI, TDO pins of PSoC 5, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

[5] By default, PSoC 5 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 5 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

[6] nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controlller during first time programming of PSoC 5 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

Table 11-2. DC Specifications (continued)

Parameter	Description	Conditions		Min	Typ	Max	Units
I_{DD}[22]	**Sleep Mode**[23]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz)[24] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5–5.5 V	T = –40 °C	–	1.9	3.1	µA
			T = 25 °C	–	2.4	3.6	
			T = 85 °C	–	5	16	
			T = 105 °C	–	5	16	
		$V_{DD} = V_{DDIO}$ = 2.7–3.6 V	T = –40 °C	–	1.7	3.1	
			T = 25 °C	–	2	3.6	
			T = 85 °C	–	4.2	16	
			T = 105 °C	–	4.2	16	
		$V_{DD} = V_{DDIO}$ = 1.71–1.95 V	T = –40 °C	–	1.6	3.1	
			T = 25 °C	–	1.9	3.6	
			T = 85 °C	–	4.2	16	
			T = 105 °C	–	4.2	16	
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7–3.6 V[25]	T = 25 °C	–	3	4.2	µA
	I2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7–3.6 V[25]	T = 25 °C	–	1.7	3.6	µA

Notes
22. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
23. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.
24. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
25. Based on device characterization (Not production tested).

Table 11-11. SIO AC Specifications[39]

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	60	ns
Fsioout	SIO output operating frequency					
	2.7 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 2.7 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	2.7 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

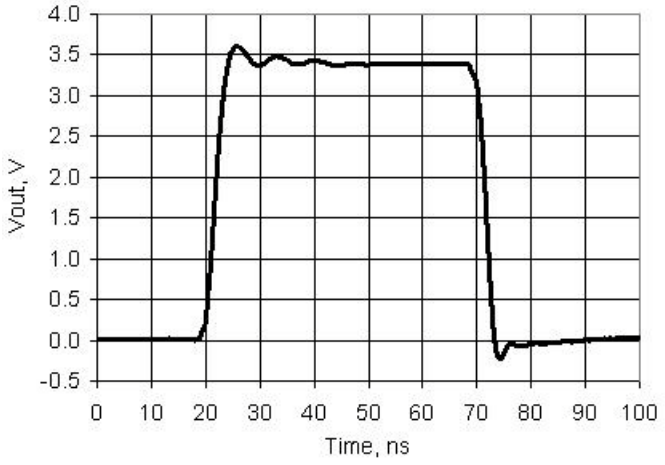
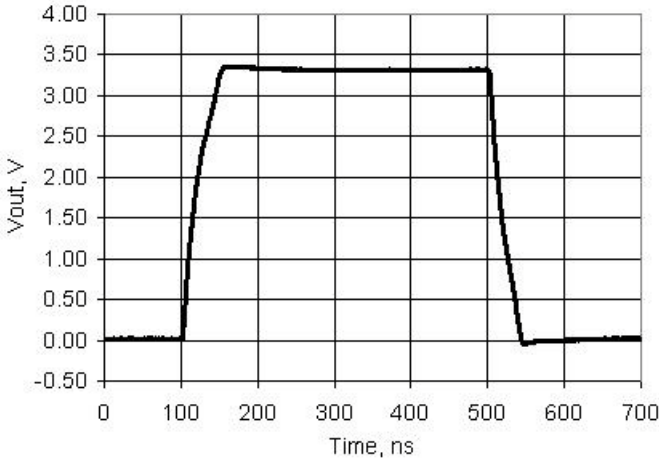


Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



Note
39. Based on device characterization (Not production tested).

11.5.5 Analog Globals

Table 11-26. Analog Globals DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through P2[4], AGL0, DSM INP, AGL1, P2[5][50]	V_{DDA} = 3.0 V	–	1500	2200	Ω
		V_{DDA} = 1.71 V	–	1200	1700	Ω
Rppmuxbus	Resistance pin-to-pin through P2[3], amuxbusL, P2[4][50]	V_{DDA} = 3.0 V	–	700	1100	Ω
		V_{DDA} = 1.71 V	–	600	900	Ω

Table 11-27. Analog Globals AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Inter-pair crosstalk for analog routes[51, 52]		106	–	–	dB
BWag	Analog globals 3 db bandwidth[52]	V_{DDA} = 3.0 V, 25 °C	–	26	–	MHz

11.5.6 Comparator

Table 11-28. Comparator DC Specifications[53]

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, V_{DDA} > 2.7 V, $V_{IN} \geq$ 0.5 V	–		10	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		9	mV
V_{OS}	Input offset voltage in fast mode	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[53]	Custom trim	–	–	4	mV
V_{OS}	Input offset voltage in ultra low power mode		–	±12	–	mV
TCVos	Temperature coefficient, input offset voltage	V_{CM} = V_{DDA} / 2, fast mode	–	63	85	µV/°C
		V_{CM} = V_{DDA} / 2, slow mode	–	15	20	
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA}	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode	V_{SSA}	–	V_{DDA} – 1.15	V
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode		–	–	400	µA
	Low current mode/slow mode		–	–	100	µA
	Ultra low power mode		–	6	–	µA

Table 11-29. Comparator AC Specifications[53]

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low power mode	50 mV overdrive, measured pin-to-pin	–	55	–	µs

Notes
50. Based on device characterization (Not production tested).
51. This value is calculated, not measured.
52. Pin P6[4] to del-sig ADC input; calculated, not measured.
53. The recommended procedure for using a custom trim value for the on-chip comparators are found in the TRM.

Table 11-30. IDAC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
DNL	Differential nonlinearity	Sink mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 31.875 µA, Rload = 20 kΩ, Cload = 15 pF[55]	–	±0.2	±1	LSB
		Sink mode, range = 31.875 µA, Rload = 20 kΩ, Cload = 15 pF[55]	–	±0.2	±1	LSB
		Source mode, range = 2.0 4 mA, Rload = 600 Ω, Cload = 15 pF[55]	–	±0.2	±1	LSB
		Sink mode, range = 2.0 4 mA, Rload = 600 Ω, Cload = 15 pF[55]	–	±0.2	±1	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to V_{DDA} or Rload to V_{SSA}, Vdiff from V_{DDA}	1	–	–	V
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	44	100	µA
		Slow mode, source mode, range = 255 µA,	–	33	100	µA
		Slow mode, source mode, range = 2.04 mA	–	33	100	µA
		Slow mode, sink mode, range = 31.875 µA	–	36	100	µA
		Slow mode, sink mode, range = 255 µA	–	33	100	µA
		Slow mode, sink mode, range = 2.04 mA	–	33	100	µA
		Fast mode, source mode, range = 31.875 µA	–	310	500	µA
		Fast mode, source mode, range = 255 µA	–	305	500	µA
		Fast mode, source mode, range = 2.04 mA	–	305	500	µA
		Fast mode, sink mode, range = 31.875 µA	–	310	500	µA
		Fast mode, sink mode, range = 255 µA	–	300	500	µA
		Fast mode, sink mode, range = 2.04 mA	–	300	500	µA

Note
55. Based on device characterization (Not production tested).

Table 11-50. Fixed I²C AC Specifications[67]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		–	–	1	Mbps

11.6.5 Controller Area Network

Table 11-51. CAN DC Specifications[67, 68]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Block current consumption		–	–	200	µA

Table 11-52. CAN AC Specifications[67, 68]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate	Minimum 8 MHz clock	–	–	1	Mbit

11.6.6 Digital Filter Block

Table 11-53. DFB DC Specifications[68]

Parameter	Description	Conditions	Min	Typ	Max	Units
	DFB operating current	64-tap FIR at F_{DFB}				
		500 kHz (6.7 ksps)	–	0.16	0.27	mA
		1 MHz (13.4 ksps)	–	0.33	0.53	mA
		10 MHz (134 ksps)	–	3.3	5.3	mA
		48 MHz (644 ksps)	–	15.7	25.5	mA
		80 MHz (1.07 Msps)	–	26.0	42.5	mA

Table 11-54. DFB AC Specifications[68]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DFB}	DFB operating frequency		DC	–	80.01	MHz

11.6.7 USB

Table 11-55. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[69]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

Notes
67. Based on device characterization (Not production tested).
68. Refer to ISO 11898 specification for details.
69. Rise/fall time matching (TR) not guaranteed, see Table 11-15 on page 82.

11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-57. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-58. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	15	20	ms
T_{ERASE}	Row erase time		–	10	13	ms
	Row program time		–	5	7	ms
T_{BULK}	Bulk erase time (256 KB)		–	–	140	ms
	Sector erase time (16 KB)		–	–	15	ms
T_{PROG}	Total device programming time	No overhead[71]	–	5	7.5	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Average ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	
		Ambient temp. T_A ≤ 105 °C, 10 K erase/program cycles, ≤ one year at T_A ≥ 75 °C [72]	10	–	–	

11.7.2 EEPROM

Table 11-59. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

Table 11-60. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	10	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, T_A ≤ 25 °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	
		Average ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	
		Ambient temp. T_A ≤ 105 °C, 10K erase/program cycles, ≤ one year at T_A ≥75 °C [72]	10	–	–	

Notes
71. See PSoC 5 Device Programming Specifications for a description of a low-overhead method of programming PSoC 5 flash.
72. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.

11.9.3 MHz External Crystal Oscillator

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-79. MHzECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[91]	13.56 MHz crystal	–	3.8	–	mA

Table 11-80. MHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency range		4	–	25	MHz

11.9.4 kHz External Crystal Oscillator

Table 11-81. kHzECO DC Specifications[91]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	Low power mode; CL = 6 pF	–	0.25	1.0	µA
DL	Drive level		–	–	1	µW

Table 11-82. kHzECO AC Specifications[91]

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T_{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-83. External Clock Reference AC Specifications[91]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase–Locked Loop

Table 11-84. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 80 MHz	–	650	–	µA
		In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-85. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[92]		1	–	48	MHz
	PLL intermediate frequency[93]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[92]		24	–	80	MHz
	Lock time at startup		–	–	250	µs
Jperiod–rms	Jitter (rms)[91]		–	–	250	ps

Notes
91. Based on device characterization (Not production tested).
92. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
93. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C56LP device includes: up to 256K flash, 64K SRAM, 2K EEPROM, a precision on–chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I^2C, JTAG/SWD programming and debug, external memory interface, boost, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C56LP derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C56LP Family with ARM Cortex-M3 CPU

Part Number	MCU Core				Analog							Digital				I/O[96]				Package	JTAG ID[97]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADCs	DAC	Comparators	SC/CT Analog Blocks[94]	Opamps	DFB	CapSense	UDBs[95]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
CY8C5668AXI-LP010	67	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E10A069
CY8C5668AXI-LP013	67	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E10D069
CY8C5668LTI-LP014	67	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E10E069
CY8C5667AXI-LP006	67	128	32	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E106069
CY8C5667LTI-LP008	67	128	32	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E108069
CY8C5667LTI-LP009	67	128	32	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E109069
CY8C5666AXI-LP001	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	–	–	70	62	8	0	100-TQFP	0x2E101069
CY8C5666AXI-LP004	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-TQFP	0x2E104069
CY8C5666AXQ-LP004	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-TQFP	0x2E104069
CY8C5666LTI-LP005	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-QFN	0x2E105069
CY8C5667AXI-LP040	67	128	32	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E128069
CY8C5667AXQ-LP040	67	128	32	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E128069
CY8C5668AXI-LP034	67	256	64	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E122069
CY8C5667LTI-LP041	67	128	32	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E129069
CY8C5688AXI-LP099	80	256	64	2	4	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E163069
CY8C5688LTI-LP086	80	256	64	2	4	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E156069
CY8C5688FNI-LP211	80	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	99-WLCSP	0x2E1D3069

Notes

94. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See Example Peripherals on page 39 for more information on how analog blocks can be used.
95. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See Example Peripherals on page 39 for more information on how UDBs can be used.
96. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See I/O System and Routing on page 32 for details on the functionality of each of these types of I/O.
97. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	105	°C
T_J	Operating junction temperature		–40	–	120	°C
T_{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T_{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T_{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T_{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt
T_A	Operating ambient temperature	For CSP parts	–40	25	85	°C
T_J	Operating junction temperature	For CSP parts	–40	–	100	°C
T_{JA}	Package θ_{JA} (99-ball CSP)			16.5		°C/Watt
T_{Jc}	Package θ_{JC} (99-ball CSP)		–	0.1	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
99-pin CSP	255 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
99-pin CSP	MSL 1

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration datasheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SIO	special input/output, GPIO with advanced features. See GPIO.
SNR	signal-to-noise ratio
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset pin
XTAL	crystal

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C56LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84935				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H (cont.)	4698847	AVER / MKEA / GJV	03/24/2015	Updated Electrical Specifications: Updated Memory: Updated Flash: Updated Table 11-58: Updated details in “Conditions” column corresponding to “Flash data retention time” parameter. Added Note 72 and referred the same note in last condition corresponding to “Flash data retention time” parameter. Updated EEPROM: Updated Table 11-60: Updated details in “Conditions” column corresponding to “EEPROM data retention time” parameter. Added Note 72 and referred the same note in last condition corresponding to “EEPROM data retention time” parameter. Updated Nonvolatile Latches (NVL): Updated Table 11-62: Updated details in “Conditions” column corresponding to “NVL data retention time” parameter. Added Note 73 and referred the same note in last condition corresponding to “NVL data retention time” parameter. Updated Clocking: Updated Internal Main Oscillator: Updated Table 11-76: Replaced 85 °C with 105 °C. Updated Figure 11-78. Updated Ordering Information: Updated Part Numbering Conventions: Added “Q: Extended” as sub bullet under “g: Temperature Range”. Updated Packaging: Updated Table 13-1: Changed maximum value of T_A parameter from 85 °C to 105 °C. Changed maximum value of T_J parameter from 100 °C to 120 °C. Updated : Updated : spec 001-88034 – Changed revision from ** to *A.
*I	4839323	MKEA	07/15/2015	Added reference to code examples in More Information. Updated typ value of T_{WRITE} from 2 to 10 in EEPROM AC specs table. Changed “Device supply for USB operation" to "Device supply (V_{DDD}) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for V_{DDA} and V_{DDD}. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Delta-sigma ADC DC Specifications

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*J	5030641	MKEA	11/30/2015	Added Table 2-1. Removed the configurable XRES information. Updated *Section 5.6* Updated *Section 6.3.1.1*. Updated values for DSI Fmax, Fgpioin max, and Fsioin max. Corrected the web link for the PSoC 5 Device Programming Specifications in *Section 9.* Updated CSP Package Bootloader section. Added MHzECO DC Specifications. Updated 99-WLCSP and 100-pin TQFP package drawings. Added a footnote reference for the "CY8C5287AXI-LP095" part in Table 12-1 clarifying that it has 256 KB flash. Added the CY8C5667AXQ-LP040 part in Table 12-1.
*K	5478402	MKEA	10/25/2016	Updated More Information. Add Links to CAD Libraries in *Section 2.* Corrected typos in External Electrical Connections.
*L	5703770	GNKK	04/20/2017	Updated the Cypress logo and copyright information.