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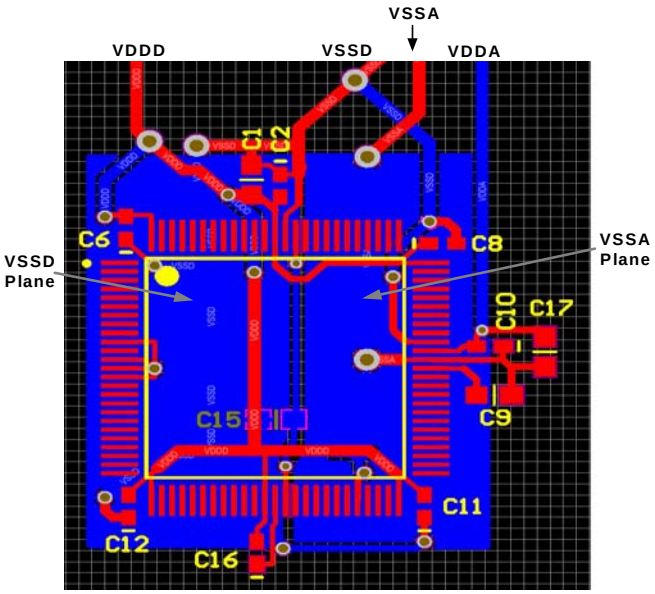
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5667axi-lp006

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3

Low resistance output pin for high current DACs (IDAC).

Opamp0out, Opamp1out, Opamp2out, Opamp3out

High current output of uncommitted opamp[7].

Extref0, Extref1

External reference input to the analog system.

SAR0 EXTREF, SAR1 EXTREF

External references for SAR ADCs

Opamp0–, Opamp1–, Opamp2–, Opamp3–

Inverting input to uncommitted opamp.

Opamp0+, Opamp1+, Opamp2+, Opamp3+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[7].

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

Ind

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4 to 25 MHz crystal oscillator pin.

nTRST

Optional JTAG Test Reset programming and debug port connection to reset the JTAG connection.

SIO. Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial Wire Debug Clock programming and debug port connection.

SWDIO

Serial Wire Debug Input and Output programming and debug port connection.

TCK

JTAG Test Clock programming and debug port connection.

TDI

JTAG Test Data In programming and debug port connection.

TDO

JTAG Test Data Out programming and debug port connection.

TMS

JTAG Test Mode Select programming and debug port connection.

TRACECLK

Cortex-M3 TRACEPORT connection, clocks TRACEDATA pins.

TRACEDATA[3:0].

Cortex-M3 TRACEPORT connections, output data.

SWV.

Single Wire Viewer output.

USBIO, D+

Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

Note
7. GPIOs with opamp outputs are not recommended for use with CapSense.

5. Memory

5.1 Static RAM

CY8C56LP Static RAM (SRAM) is used for temporary data storage. Code can be executed at full speed from the portion of SRAM that is located in the code space. This process is slower from SRAM above 0x20000000. The device provides up to 64 KB of SRAM. The CPU or the DMA controller can access all of SRAM. The SRAM can be accessed simultaneously by the Cortex-M3 CPU and the DMA controller if accessing different 32 KB blocks.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 256 KB of user program space.

Up to an additional 32 KB of flash space is available for Error Correcting Codes (ECC). If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected. The flash output is 9 bytes wide with 8 bytes of data and 1 byte of ECC data.

The CPU or DMA controller read both user code and bulk data located in flash through the cache controller. This provides higher CPU performance. If ECC is enabled, the cache controller also performs error checking and correction.

Flash programming is performed through a special interface and preempts code execution out of flash. Code execution may be done out of SRAM during flash programming.

The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I^2C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the "Device Security" section on page 64). For more information on how to take full advantage of the security features in PSoC, see the PSoC 5 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte addressable nonvolatile memory. The CY8C56LP has 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The factory default values of all EEPROM bytes are 0.

Because the EEPROM is mapped to the Cortex-M3 Peripheral region, the CPU cannot execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

It can take as much as 20 milliseconds to write to EEPROM or flash. During this time the device should not be reset, or unexpected changes may be made to portions of EEPROM or flash. Reset sources (see *Section 6.3.1*) include XRES pin, software reset, and watchdog; care should be taken to make sure that these are not inadvertently activated. In addition, the low voltage detect circuits should be configured to generate an interrupt instead of a reset.

6. System Integration

6.1 Clocking System

The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 80 MHz clock, accurate to ±1% over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. All of the system clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows designers to build clocking systems with minimal input. The designer can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent in PSoC.

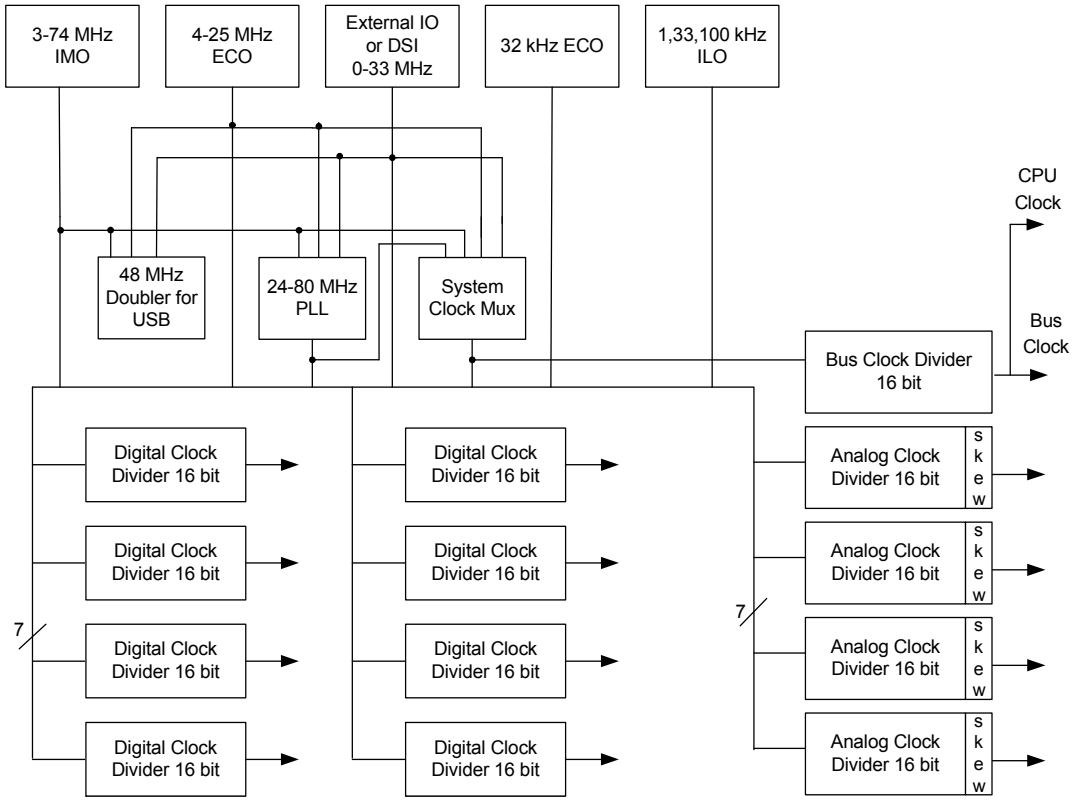
Key features of the clocking system include:

- Seven general purpose clock sources
  - 3- to 74-MHz IMO, ±1% at 3 MHz
  - 4- to 25-MHz External Crystal Oscillator (MHzECO)
  - Clock doubler provides a doubled clock frequency output for the USB block, see USB Clock Domain on page 26
  - DSI signal from an external I/O pin or other logic
  - 24- to 80-MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, or DSI
  - Clock Doubler
  - 1-kHz, 33-kHz, 100-kHz ILO for Watch Dog Timer (WDT) and Sleep Timer
  - 32.768-kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- IMO has a USB mode that auto locks to USB bus clock requiring no external crystal for USB. (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the CPU bus and CPU clock
- Automatic clock configuration in PSoC Creator

Table 6-1. Oscillator Summary

Source	Fmin	Tolerance at Fmin	Fmax	Tolerance at Fmax	Startup Time
IMO	3 MHz	±1% over voltage and temperature	74 MHz	±7%	13 µs max
MHzECO	4 MHz	Crystal dependent	25 MHz	Crystal dependent	5 ms typ, max is crystal dependent
DSI	0 MHz	Input dependent	33 MHz	Input dependent	Input dependent
PLL	24 MHz	Input dependent	80 MHz	Input dependent	250 µs max
Doubler	12 MHz	Input dependent	48 MHz	Input dependent	1 µs max
ILO	1 kHz	–50%, +100%	100 kHz	–55%, +100%	15 ms max in lowest power mode
kHzECO	32 kHz	Crystal dependent	32 kHz	Crystal dependent	500 ms typ, max is crystal dependent

Figure 6-1. Clocking Subsystem



6.1.1 Internal Oscillators

Figure 6-1 shows that there are two internal oscillators. They can be routed directly or divided. The direct routes may not have a 50% duty cycle. Divided clocks have a 50% duty cycle.

6.1.1.1 Internal Main Oscillator

In most designs the IMO is the only clock source required, due to its ±1% accuracy. The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ±1% at 3 MHz, up to ±7% at 74 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency (see Phase-Locked Loop)

The IMO provides clock outputs at 3, 6, 12, 24, 48, and 74 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works for input frequency ranges of 6 to 24 MHz (providing 12 to 48 MHz at the output). It can be configured to use a clock from the IMO, MHzECO, or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 Phase-Locked Loop

The PLL allows low frequency, high accuracy clocks to be multiplied to higher frequencies. This is a tradeoff between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 80 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 µs (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low power modes.

6.1.1.4 Internal Low Speed Oscillator

The ILO provides clock frequencies for low power consumption, including the watchdog timer, and sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1 kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to low power supervisory operations such as the watchdog timer and long sleep intervals using the central timewheel (CTW).

The central timewheel is a 1 kHz, free running, 13-bit counter clocked by the ILO. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low power mode. Firmware can reset the central timewheel.

vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt. While level sensitive interrupts are not directly supported; Universal Digital Blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin. The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[11]. See the "CapSense" section on page 59 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the "LCD Direct Drive" section on page 58 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO's respective VDDIO. SIO pins are individually configurable to output either the standard V_{DDIO} level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see Figure 6-13). The "DAC" section on page 59 has more details on VDAC use and reference routing to the SIO pins. Resistive pull up and pull down drive modes are not available with SIO in regulated output mode.

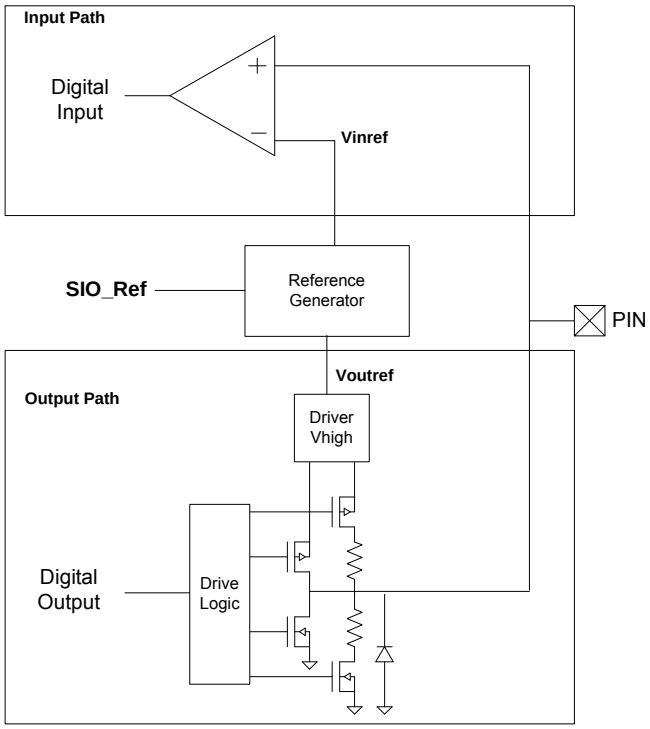
6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see Figure 6-13). Available input thresholds are:

- 0.5 × VDDIO
- 0.4 × VDDIO
- 0.5 × VREF
- VREF

Typically a voltage DAC (VDAC) generates the VREF reference. "DAC" section on page 59 has more details on VDAC use and reference routing to the SIO pins.

Figure 6-13. SIO Reference for Input and Output



Note
11. GPIOs with opamp outputs are not recommended for use with CapSense.

6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in Figure 6-10 on page 34 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating VDD.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's VIH and VIL levels are determined by the associated VDDIO supply pin.

The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See Figure 6-12 for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull down or pull up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low Power Functionality

In all low power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in "Pinouts" on page 6. The special features are:

- Digital
  - 4 to 25 MHz crystal oscillator
  - 32.768 kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - TRACEPORT interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all pins for board level test.

7. Digital Subsystem

The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

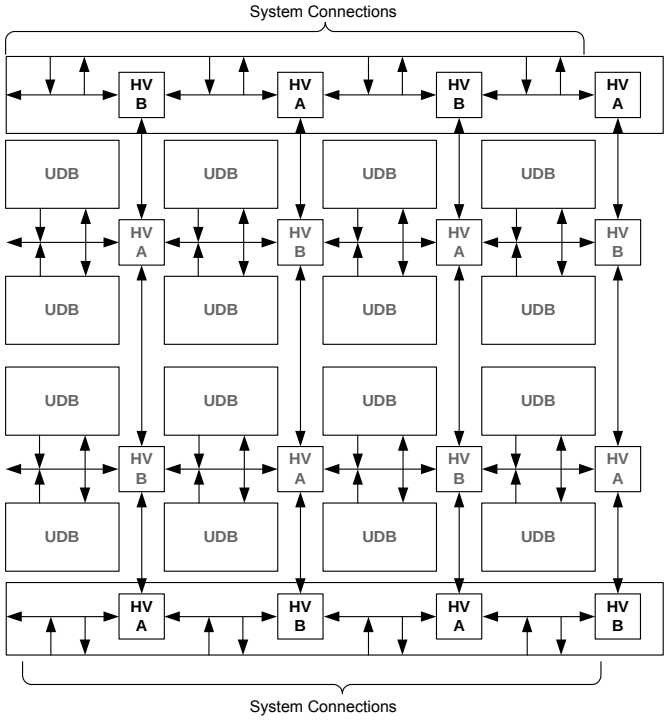
The main components of the digital programmable system are:

- Universal Digital Blocks (UDB) - These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal Digital Block array - UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.

7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-7. Digital System Interface Structure

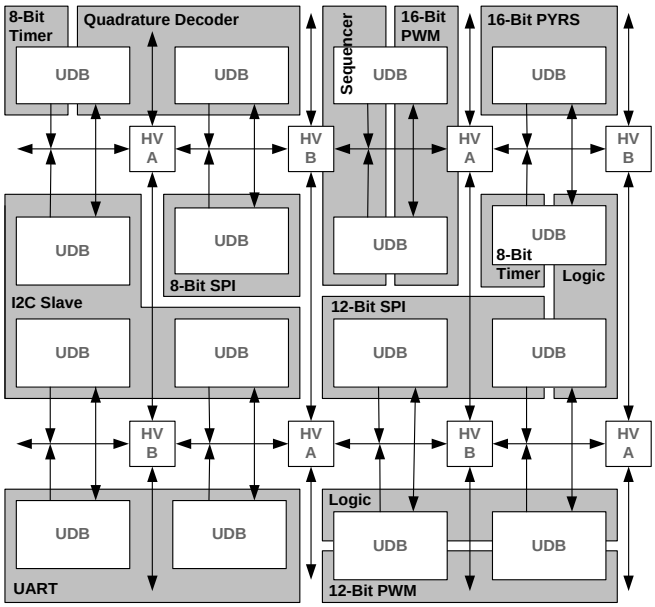


7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-8. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

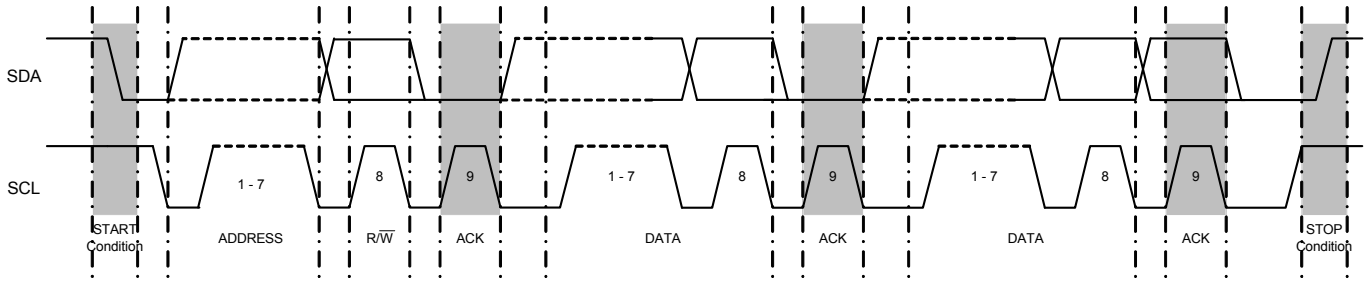
The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

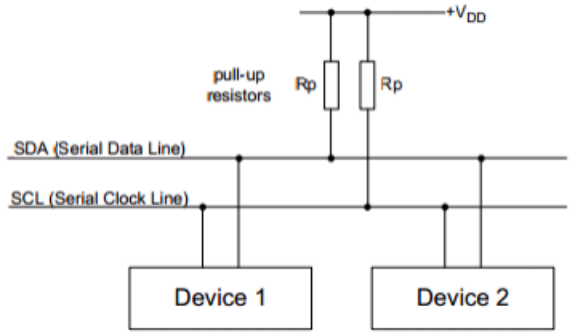
Figure 7-18. I²C Complete Transfer Timing



7.8.1 External Electrical Connections

As Figure 7-19 shows, the I²C bus requires external pull-up resistors (R_P). These resistors are primarily determined by the supply voltage, bus speed, and bus capacitance. For detailed information on how to calculate the optimum pull-up resistor value for your design, we recommend using the UM10204 I2C-bus specification and user manual Rev 6, or newer, available from the NXP website at www.nxp.com.

Figure 7-19. Connection of Devices to the I²C Bus



For most designs, the default values in Table 7-2 will provide excellent performance without any calculations. The default values were chosen to use standard resistor values between the minimum and maximum limits. The values in Table 7-2 work for designs with 1.8 V to 5.0V V_{DD}, less than 200-pF bus capacitance (C_B), up to 25 µA of total input leakage (I_{IL}), up to 0.4 V output voltage level (V_{OL}), and a max V_{IH} of 0.7 * V_{DD}. Standard Mode and Fast Mode can use either GPIO or SIO PSoC pins. Fast Mode Plus requires use of SIO pins to meet the V_{OL} spec at 20 mA. Calculation of custom pull-up resistor values is required; if your design does not meet the default assumptions, you use series resistors (RS) to limit injected noise, or you need to maximize the resistor value for low power consumption.

Table 7-2. Recommended default Pull-up Resistor Values

	R_P	Units
Standard Mode – 100 kbps	4.7 k, 5%	Ω
Fast Mode – 400 kbps	1.74 k, 1%	Ω
Fast Mode Plus – 1 Mbps	620, 5%	Ω

Calculation of the ideal pull-up resistor value involves finding a value between the limits set by three equations detailed in the NXP I²C specification. These equations are:

Equation 1:

$$R_{PMIN} = (V_{DD}(max) - V_{OL}(max))/(I_{OL}(min))$$

Equation 2:

$$R_{PMAX} = T_R(max)/0.8473 \times C_B(max)$$

Equation 3:

$$R_{PMAX} = V_{DD}(min) - V_{IH}(min) + V_{NH}(min)/I_{IH}(max)$$

Equation parameters:

V_{DD} = Nominal supply voltage for I²C bus

V_{OL} = Maximum output low voltage of bus devices.

I_{OL}= Low-level output current from I²C specification

T_R = Rise Time of bus from I²C specification

C_B = Capacitance of each bus line including pins and PCB traces

V_{IH} = Minimum high-level input voltage of all bus devices

V_{NH} = Minimum high-level input noise margin from I²C specification

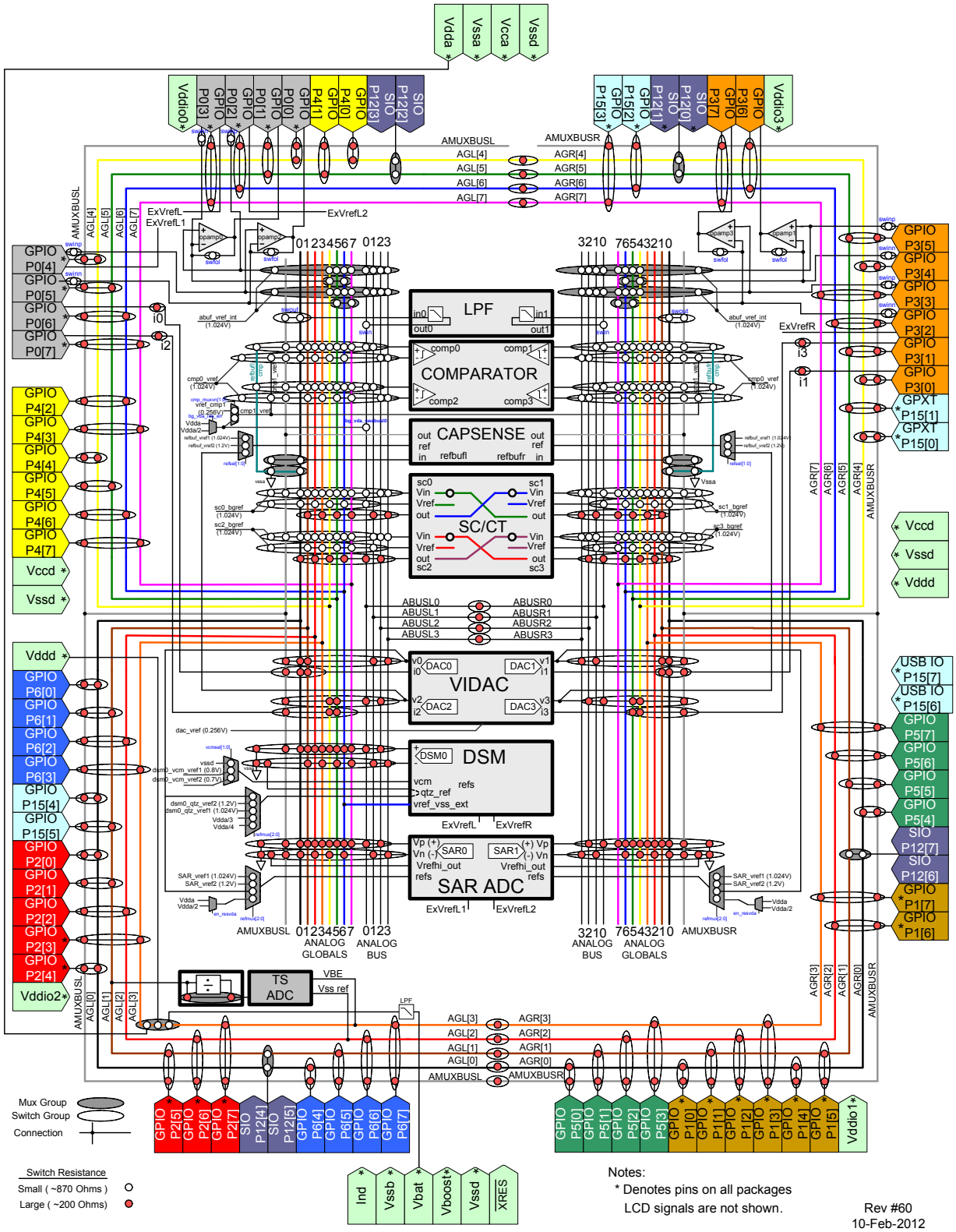
IIH = Total input leakage current of all devices on the bus

The supply voltage (V_{DD}) limits the minimum pull-up resistor value due to bus devices maximum low output voltage (V_{OL}) specifications. Lower pull-up resistance increases current though the pins and can, therefore, exceed the spec conditions of V_{OH}. Equation 1 is derived using Ohm's law to determine the minimum resistance that will still meet the V_{OL} specification at 3 mA for standard and fast modes, and 20 mA for fast mode plus at the given V_{DD}.

Equation 2 determines the maximum pull-up resistance due to bus capacitance. Total bus capacitance is comprised of all pin, wire, and trace capacitance on the bus. The higher the bus capacitance, the lower the pull-up resistance required to meet the specified bus speeds rise time due to RC delays. Choosing a pull-up resistance higher than allowed can result in failing timing requirements resulting in communication errors. Most designs with five or less I²C devices and up to 20 centimeters of bus trace length have less than 100 pF of bus capacitance.

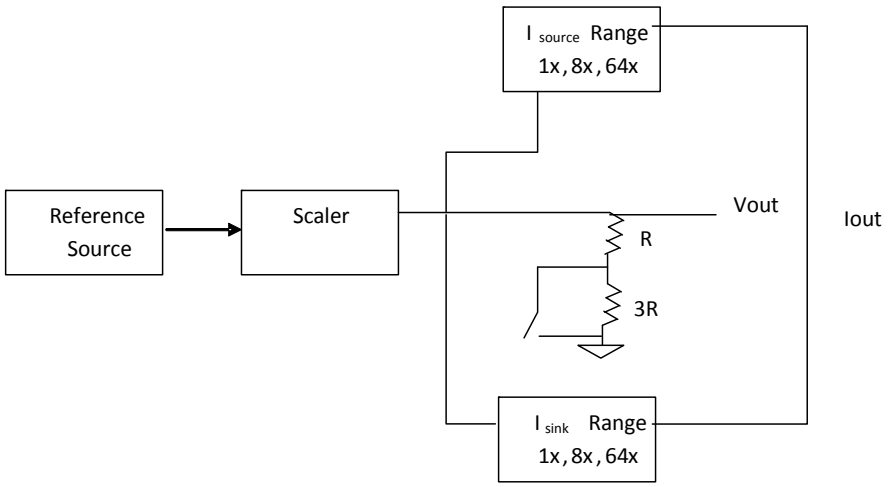
A secondary effect that limits the maximum pull-up resistor value is total bus leakage calculated in Equation 3. The primary source of leakage is I/O pins connected to the bus. If leakage is too high, the pull-ups will have difficulty maintaining an acceptable V_{IH} level causing communication errors. Most designs with five or less I²C devices on the bus have less than 10 µA of total leakage current.

Figure 8-2. CY8C56LP Analog Interconnect



To preserve detail of this image, this image is best viewed with a PDF display program or printed on 11” × 17” paper.

Figure 8-12. DAC Block Diagram



8.10.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.10.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.11 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk - Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-13. Mixer Configuration

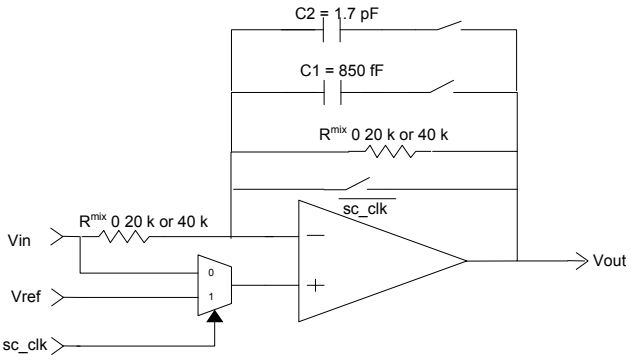


Figure 11-15. GPIO Output High Voltage and Current

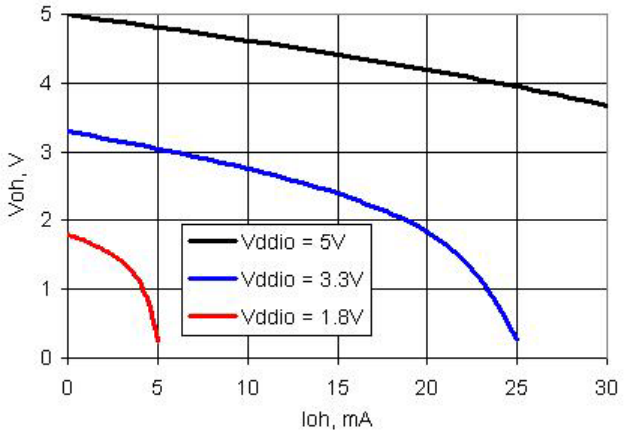


Figure 11-16. GPIO Output Low Voltage and Current

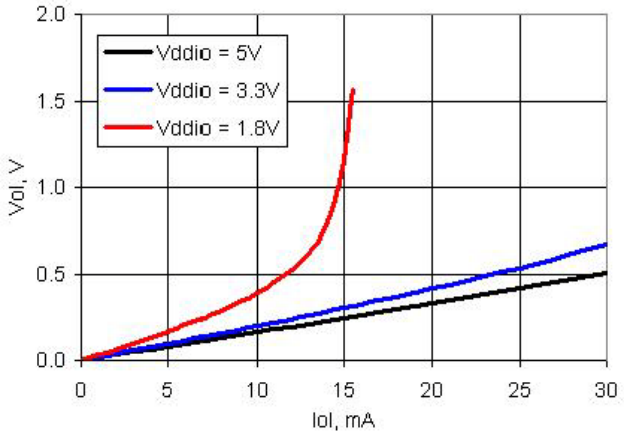


Table 11-9. GPIO AC Specifications[36]

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode	3.3 V V_{DDIO} Cload = 25 pF	–	–	6	ns
TfallF	Fall time in Fast Strong Mode	3.3 V V_{DDIO} Cload = 25 pF	–	–	6	ns
TriseS	Rise time in Slow Strong Mode	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
TfallS	Fall time in Slow Strong Mode	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
Fgpioout	GPIO output operating frequency					
	2.7 V ≤ V_{DDIO} ≤ 5.5 V, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V ≤ V_{DDIO} < 2.7 V, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	20	MHz
	3.3 V ≤ V_{DDIO} ≤ 5.5 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	7	MHz
	1.71 V ≤ V_{DDIO} < 3.3 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	3.5	MHz
Fgpioin	GPIO input operating frequency	90/10% V_{DDIO}	–	–	33	MHz

Note
36. Based on device characterization (Not production tested).

Table 11-11. SIO AC Specifications[39]

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	60	ns
Fsioout	SIO output operating frequency					
	2.7 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 2.7 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	2.7 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

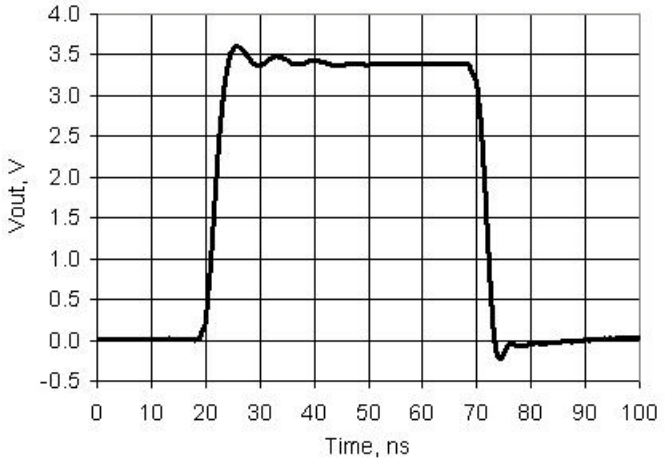
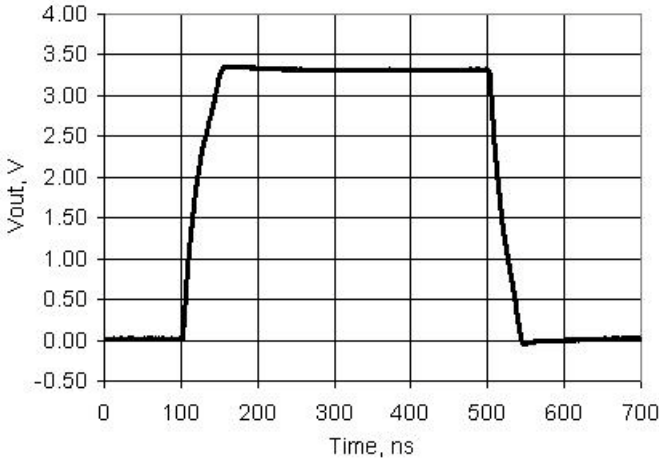


Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



Note
39. Based on device characterization (Not production tested).

Figure 11-24. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load

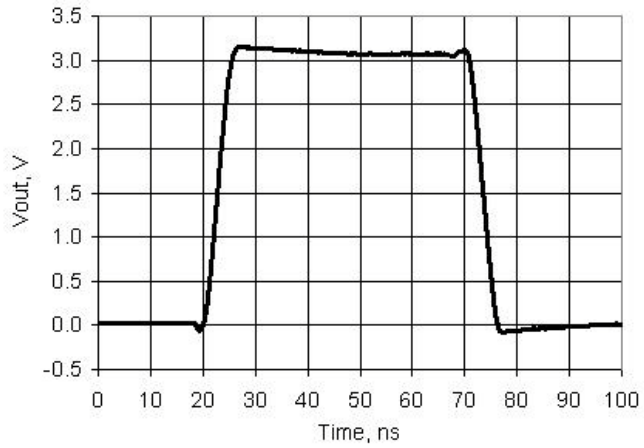


Table 11-15. USB Driver AC Specifications[42]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5}, $V_{USB\_3.3}$, see USB DC Specifications on page 106	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

11.4.4 XRES

Table 11-16. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
V_{IL}	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
Rpullup	Pull up resistor		3.5	5.6	8.5	kΩ
C_{IN}	Input capacitance		–	3		pF
V_H	Input voltage hysteresis (Schmitt-trigger)		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA

Table 11-17. XRES AC Specifications[42]

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	µs

Note
42. Based on device characterization (Not production tested).

Figure 11-30. Opamp Noise vs Frequency, Power Mode = High, V_{DDA} = 5 V

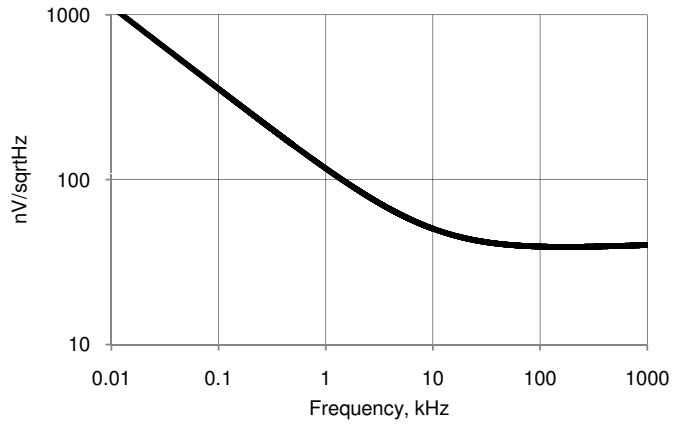


Figure 11-31. Opamp Step Response, Rising

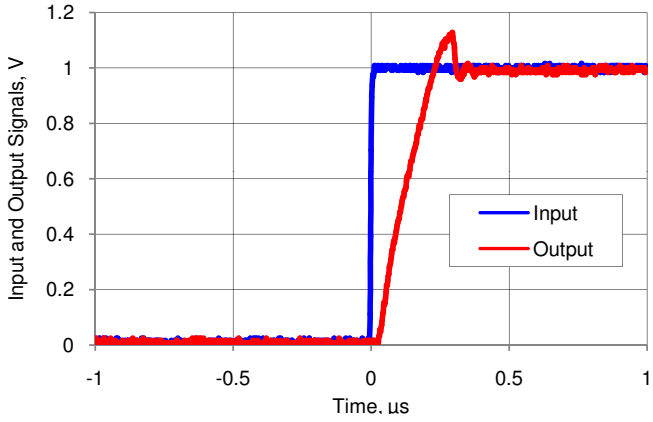


Figure 11-32. Opamp Step Response, Falling

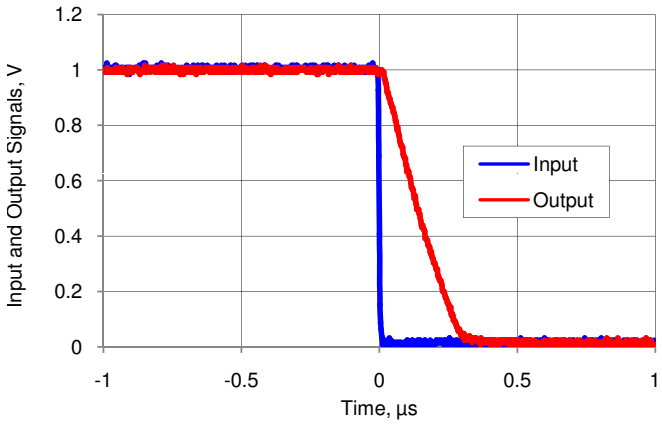


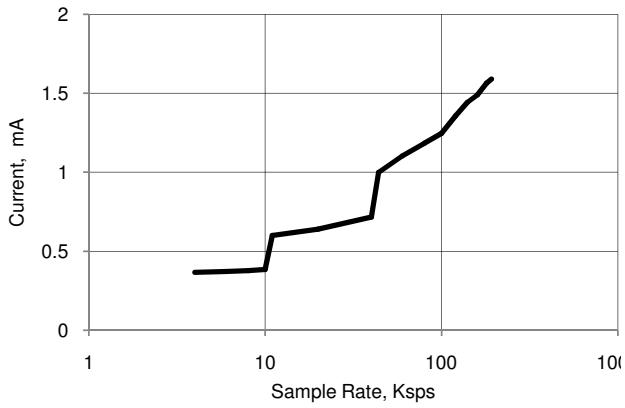
Table 11-21. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion[44]	Buffer gain = 1, 12-bit, Range = ±1.024 V	–	–	0.0032	%
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power[44]	Range = ±1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate[44]	Range = ±1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference[44]	Range = ±1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power[44]	Range = ±1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate[44]	Range = ±1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference[44]	Range = ±1.024 V, unbuffered	43	–	–	dB

Table 11-22. Delta-sigma ADC Sample Rates, Range = ±1.024 V

Resolution, Bits	Continuous		Multi-Sample	
	Min	Max	Min	Max
8	8000	384000	1911	91701
9	6400	307200	1543	74024
10	5566	267130	1348	64673
11	4741	227555	1154	55351
12	4000	192000	978	46900

Figure 11-33. Delta-sigma ADC IDD vs sps, Range = ±1.024 V, Continuous Sample Mode, Input Buffer Bypassed



Note
44. Based on device characterization (Not production tested).

11.8.3 Interrupt Controller

Table 11-71. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from main line code[80]		–	–	12	Tcy CPU
	Delay from interrupt signal input to ISR code execution from ISR code (tail-chaining)[80]		–	–	6	Tcy CPU

11.8.4 JTAG Interface

Figure 11-74. JTAG Interface Timing

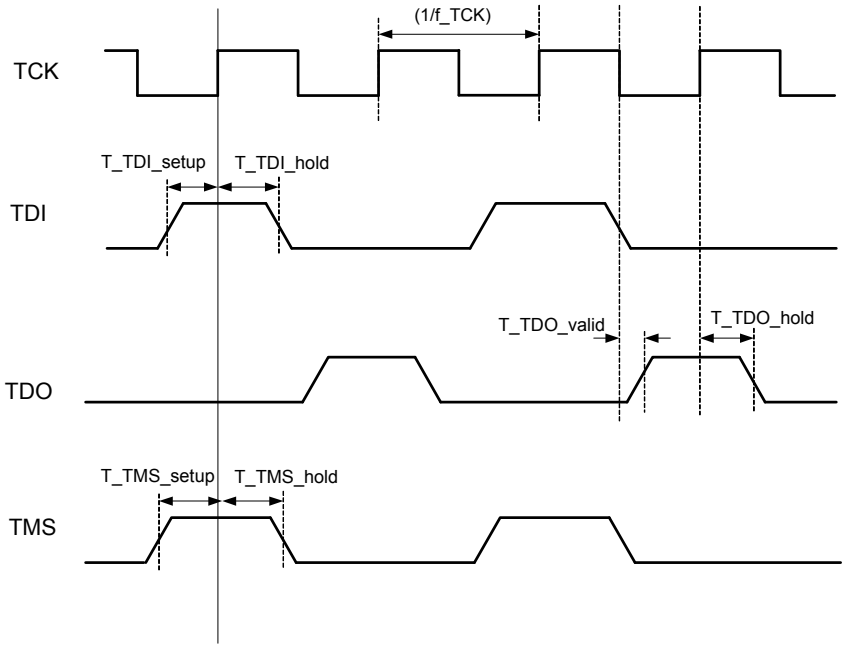


Table 11-72. JTAG Interface AC Specifications[81]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	12[82]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[82]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_nTRST	Minimum nTRST pulse width	f_TCK = 2 MHz	8	–	–	ns

Notes
80. ARM Cortex-M3 NVIC spec. Visit www.arm.com for detailed documentation about the Cortex-M3 CPU.
81. Based on device characterization (Not production tested).
82. f_TCK must also be no more than 1/3 CPU clock frequency.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C56LP device includes: up to 256K flash, 64K SRAM, 2K EEPROM, a precision on–chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I^2C, JTAG/SWD programming and debug, external memory interface, boost, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C56LP derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

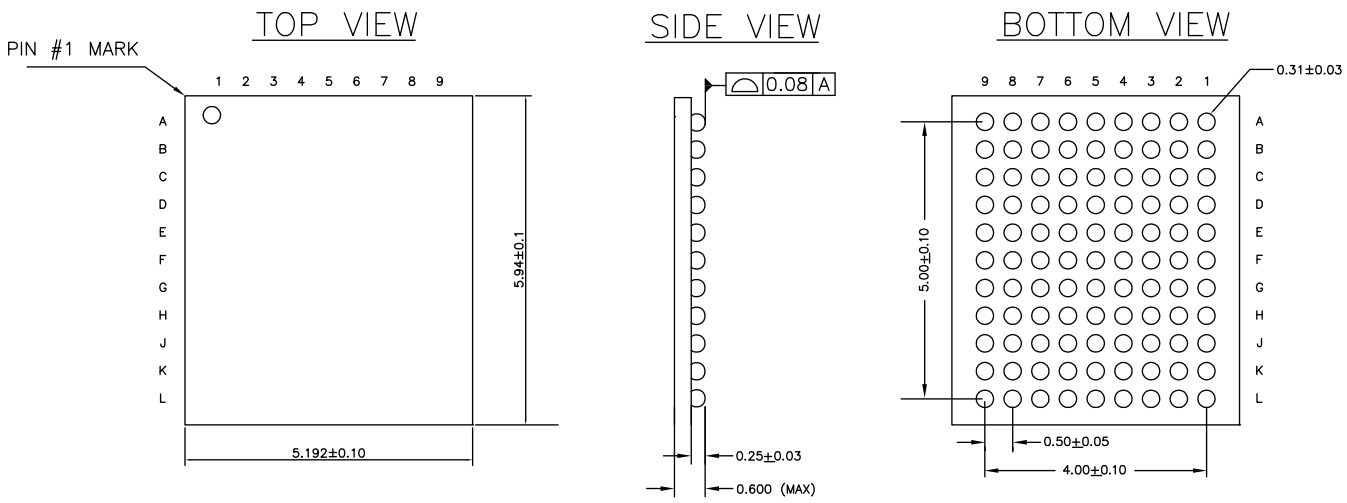
Table 12-1. CY8C56LP Family with ARM Cortex-M3 CPU

Part Number	MCU Core				Analog							Digital				I/O[96]				Package	JTAG ID[97]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADCs	DAC	Comparators	SC/CT Analog Blocks[94]	Opamps	DFB	CapSense	UDBs[95]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
CY8C5668AXI-LP010	67	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E10A069
CY8C5668AXI-LP013	67	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E10D069
CY8C5668LTI-LP014	67	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E10E069
CY8C5667AXI-LP006	67	128	32	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E106069
CY8C5667LTI-LP008	67	128	32	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E108069
CY8C5667LTI-LP009	67	128	32	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E109069
CY8C5666AXI-LP001	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	–	–	70	62	8	0	100-TQFP	0x2E101069
CY8C5666AXI-LP004	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-TQFP	0x2E104069
CY8C5666AXQ-LP004	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-TQFP	0x2E104069
CY8C5666LTI-LP005	67	64	16	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-QFN	0x2E105069
CY8C5667AXI-LP040	67	128	32	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E128069
CY8C5667AXQ-LP040	67	128	32	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E128069
CY8C5668AXI-LP034	67	256	64	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E122069
CY8C5667LTI-LP041	67	128	32	2	✔	12-bit Del-Sig, 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E129069
CY8C5688AXI-LP099	80	256	64	2	4	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E163069
CY8C5688LTI-LP086	80	256	64	2	4	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E156069
CY8C5688FNI-LP211	80	256	64	2	✔	2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	99-WLCSP	0x2E1D3069

Notes

94. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See Example Peripherals on page 39 for more information on how analog blocks can be used.
95. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See Example Peripherals on page 39 for more information on how UDBs can be used.
96. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See I/O System and Routing on page 32 for details on the functionality of each of these types of I/O.
97. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Figure 2. WLCSP Package (5.192 × 5.940 × 0.6 mm)



NOTES:

1. REFERENCE JEDEC Publication 95: Design Guide 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-88034 *B

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration datasheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SIO	special input/output, GPIO with advanced features. See GPIO.
SNR	signal-to-noise ratio
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset pin
XTAL	crystal

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C56LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84935				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	5030641	MKEA	11/30/2015	Added Table 2-1. Removed the configurable XRES information. Updated *Section 5.6* Updated *Section 6.3.1.1*. Updated values for DSI Fmax, Fgpioin max, and Fsioin max. Corrected the web link for the PSoC 5 Device Programming Specifications in *Section 9.* Updated CSP Package Bootloader section. Added MHzECO DC Specifications. Updated 99-WLCSP and 100-pin TQFP package drawings. Added a footnote reference for the "CY8C5287AXI-LP095" part in Table 12-1 clarifying that it has 256 KB flash. Added the CY8C5667AXQ-LP040 part in Table 12-1.
*K	5478402	MKEA	10/25/2016	Updated More Information. Add Links to CAD Libraries in *Section 2.* Corrected typos in External Electrical Connections.
*L	5703770	GNKK	04/20/2017	Updated the Cypress logo and copyright information.