Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5667axi-lp040

Figure 2-4. 100-pin TQFP Part Pinout

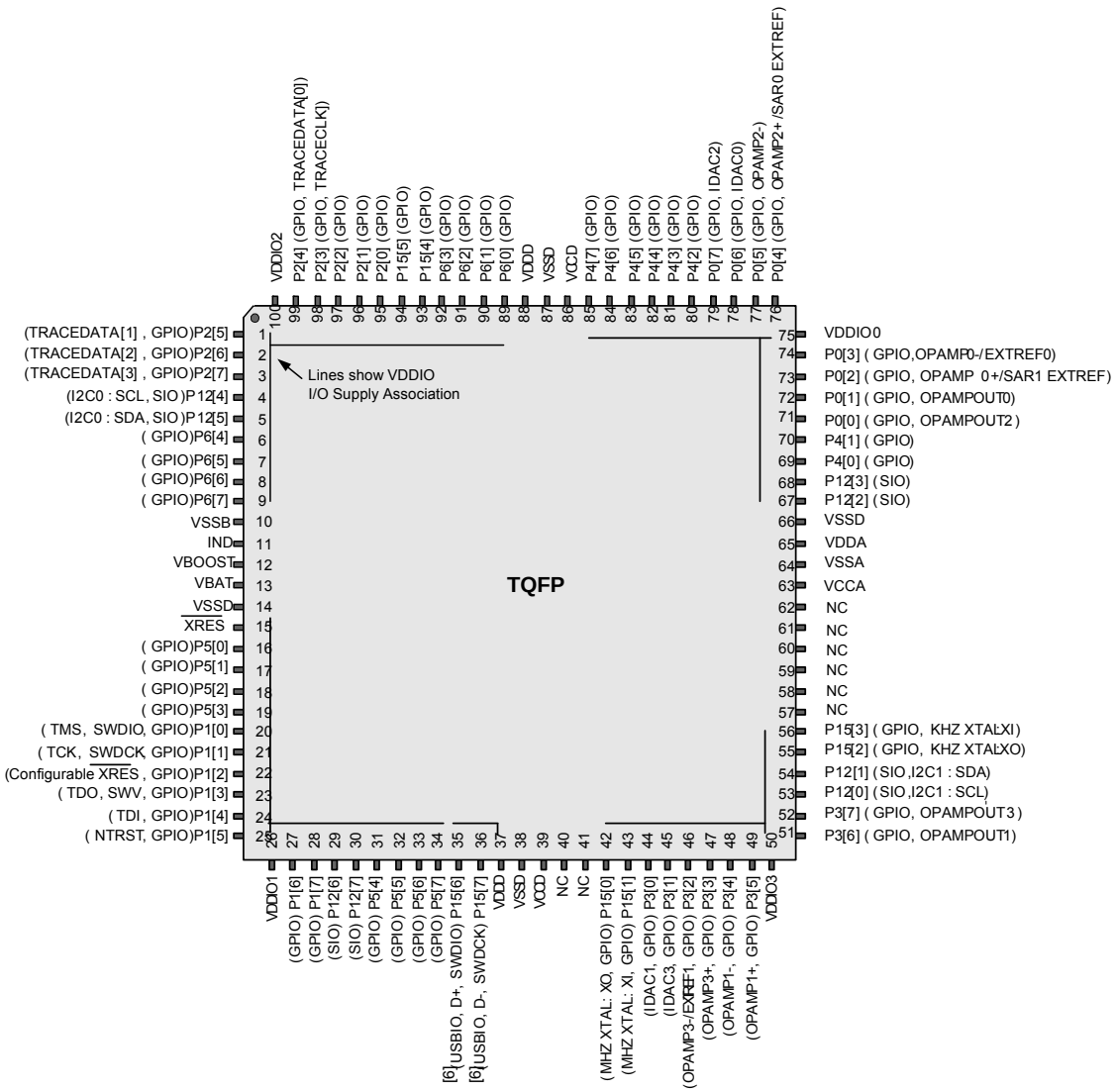


Table 2-1. V_{DDIO} and Port Pin Associations

VDDIO	Port Pins
VDDIO0	P0[7:0], P4[7:0], P12[3:2]
VDDIO1	P1[7:0], P5[7:0], P12[7:6]
VDDIO2	P2[7:0], P6[7:0], P12[5:4], P15[5:4]
VDDIO3	P3[7:0], P12[1:0], P15[3:0]
VDDD	P15[7:6] (USB D+, D-)

Note
6. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Table 2-2 shows the pinout for the 99-pin CSP package. Since there are four V_{DDIO} pins, the set of I/O pins associated with any V_{DDIO} may sink up to 100 mA total, same as for the 100-pin and 68-pin devices.

Table 2-2. CSP Pinout

Ball	Name	Ball	Name	Ball	Name	Ball	Name
E5	P2[5]	L2	VIO1	B2	P3[6]	C8	VIO0
G6	P2[6]	K2	P1[6]	B3	P3[7]	D7	P0[4]
G5	P2[7]	C9	P4[2]	C3	P12[0]	E7	P0[5]
H6	P12[4]	E8	P4[3]	C4	P12[1]	B9	P0[6]
K7	P12[5]	K1	P1[7]	E3	P15[2]	D8	P0[7]
L8	P6[4]	H2	P12[6]	E4	P15[3]	D9	P4[4]
J6	P6[5]	F4	P12[7]	A1	NC	F8	P4[5]
H5	P6[6]	J1	P5[4]	A9	NC	F7	P4[6]
J5	P6[7]	H1	P5[5]	L1	NC	E6	P4[7]
L7	VSSB	F3	P5[6]	L9	NC	E9	VCCD
K6	Ind	G1	P5[7]	A3	VCCA	F9	VSSD
L6	VBOOST	G2	P15[6]	A4	VSSA	G9	VDDD
K5	VBAT	F2	P15[7]	B7	VSSA	H9	P6[0]
L5	VSSD	E2	VDDD	B8	VSSA	G8	P6[1]
L4	XRES	F1	VSSD	C7	VSSA	H8	P6[2]
J4	P5[0]	E1	VCCD	A5	VDDA	J9	P6[3]
K4	P5[1]	D1	P15[0]	A6	VSSD	G7	P15[4]
K3	P5[2]	D2	P15[1]	B5	P12[2]	F6	P15[5]
L3	P5[3]	C1	P3[0]	A7	P12[3]	F5	P2[0]
H4	P1[0]	C2	P3[1]	C5	P4[0]	J7	P2[1]
J3	P1[1]	D3	P3[2]	D5	P4[1]	J8	P2[2]
H3	P1[2]	D4	P3[3]	B6	P0[0]	K9	P2[3]
J2	P1[3]	B4	P3[4]	C6	P0[1]	H7	P2[4]
G4	P1[4]	A2	P3[5]	A8	P0[2]	K8	VIO2
G3	P1[5]	B1	VIO3	D6	P0[3]		

Figure 2-5 and Figure 2-6 on page 11 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a 2-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 on page 10 and Power System on page 26. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled VSSD must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

4.3 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.3.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight multi-layer AHB bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

Table 4-3. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, I^2C, CAN, Timers, Counters, and PWMs
5	DFB
6	UDBs group 1
7	UDBs group 2

4.3.2 DMA Features

- 24 DMA channels
- Each channel has one or more Transaction Descriptors (TDs) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64k bytes
- Large transactions may be broken into smaller bursts of 1 to 127 bytes
- TDs may be nested and/or chained for complex transactions

4.3.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100% of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-4 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-4. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

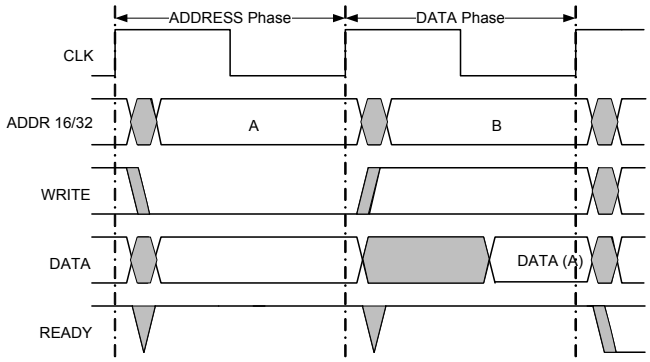
4.3.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

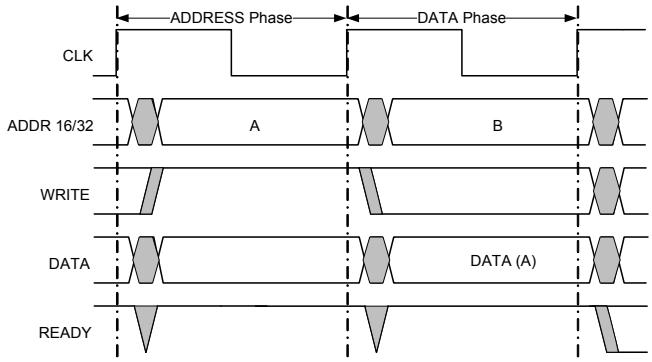
4.3.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in Figure 4-2. For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-2. DMA Timing Diagram



Basic DMA Read Transfer without wait states



Basic DMA Write Transfer without wait states

4.3.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.3.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.3.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.3.4.5 Indexed DMA

In an indexed DMA case, an external master requires access to locations on the system bus as if those locations were shared memory. As an example, a peripheral may be configured as an SPI or I^2C slave where an address is received by the external master. That address becomes an index or offset into the internal system bus memory space. This is accomplished with an initial “address fetch” TD that reads the target address location from the peripheral and writes that value into a subsequent TD in the chain. This modifies the TD chain on the fly. When the “address fetch” TD completes it moves on to the next TD, which has the new address information embedded in it. This TD then carries out the data transfer with the address location required by the external master.

4.3.4.6 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.3.4.7 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.3.4.8 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

5.5 Nonvolatile Latches (NVLs)

PSoC has a 4-byte array of nonvolatile latches (NVLs) that are used to configure the device at reset. The NVL register map is shown in Table 5-3.

Table 5-2. Device Configuration NVL Register Map

Register Address	7	6	5	4	3	2	1	0
0x00	PRT3RDM[1:0]		PRT2RDM[1:0]		PRT1RDM[1:0]		PRT0RDM[1:0]	
0x01	PRT12RDM[1:0]		PRT6RDM[1:0]		PRT5RDM[1:0]		PRT4RDM[1:0]	
0x02	XRESMEN	DBGEN					PRT15RDM[1:0]	
0x03	DIG_PHS_DLY[3:0]				ECCEN	DPS[1:0]		CFGSPEED

The details for individual fields and their factory default settings are shown in Table 5-3:.

Table 5-3. Fields and Factory Default Settings

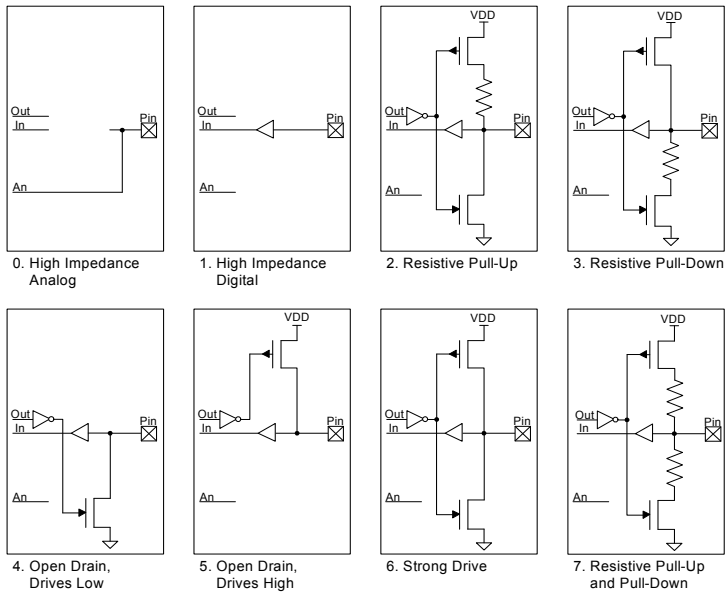
Field	Description	Settings
PRTxRDM[1:0]	Controls reset drive mode of the corresponding I/O port. See "Reset Configuration" on page 38. All pins of the port are set to the same mode.	00b (default) - high impedance analog 01b - high impedance digital 10b - resistive pull up 11b - resistive pull down
XRESMEN	Controls whether pin P1[2] is used as a GPIO or as an external reset. P1[2] is generally used as a GPIO, and not as an external reset.	0 (default) - GPIO 1 - external reset
DBGEN	Debug Enable allows access to the debug system, for third-party programmers.	0 - access disabled 1 (default) - access enabled
CFGSPEED	Controls the speed of the IMO-based clock during the device boot process, for faster boot or low-power operation	0 (default) - 12 MHz IMO 1 - 48 MHz IMO
DPS[1:0]	Controls the usage of various P1 pins as a debug port. See "Programming, Debug Interfaces, Resources" on page 61.	00b - 5-wire JTAG 01b (default) - 4-wire JTAG 10b - SWD 11b - debug ports disabled
ECCEN	Controls whether ECC flash is used for ECC or for general configuration and data storage. See "Flash Program Memory" on page 19.	0 - ECC disabled 1 (default) - ECC enabled
DIG_PHS_DLY[3:0]	Selects the digital clock phase delay.	See the TRM for details.

Although PSoC Creator provides support for modifying the device configuration NVLs, the number of NVL erase/write cycles is limited – see "Nonvolatile Latches (NVL)" on page 109.

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-12 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-12. Drive Mode



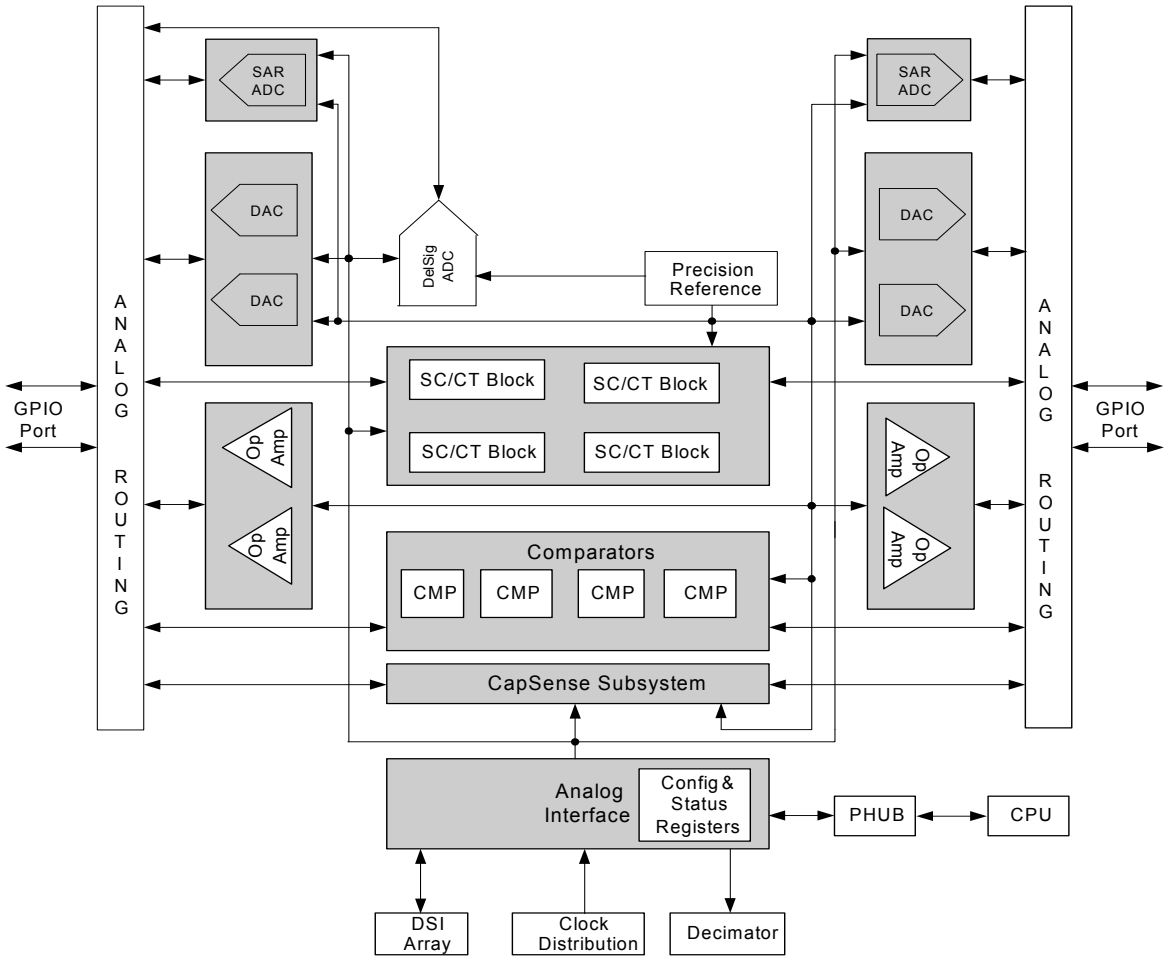
The 'Out' connection is driven from either the Digital System (when the Digital Output terminal is connected) or the Data Register (when HW connection is disabled).
The 'In' connection drives the Pin State register, and the Digital System if the Digital Input terminal is enabled and connected.
The 'An' connection connects to the Analog System.

Table 6-6. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High-impedance analog	0	0	0	High Z	High Z
1	High-impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up[10]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[10]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull up and pull down[10]	1	1	1	Res High (5K)	Res Low (5K)

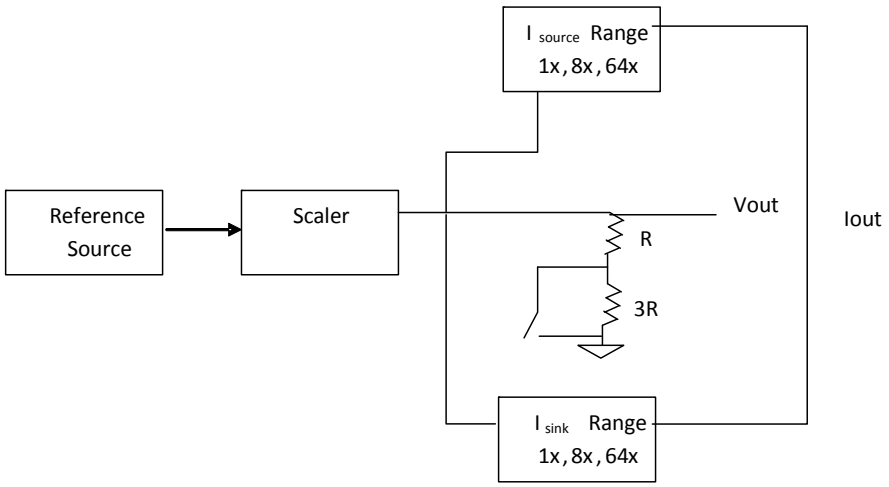
Note
10. Resistive pull up and pull down are not available with SIO in regulated output mode.

Figure 8-1. Analog Subsystem Block Diagram



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and also connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

Figure 8-12. DAC Block Diagram



8.10.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.10.2 Voltage DAC

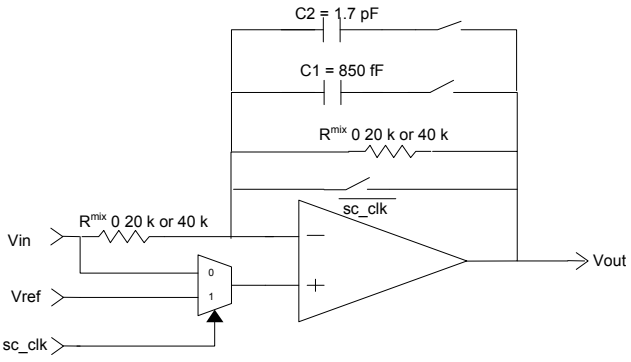
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.11 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk - Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

Figure 8-13. Mixer Configuration



If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via Serial Wire Debug (SWD) port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 5 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

9.8 CSP Package Bootloader

A factory-installed bootloader program is included in all devices with CSP packages. The bootloader is compatible with PSoC Creator 3.0 bootloadable project files, and has the following features:

- I2C-based
- SCLK and SDAT available at P1[6] and P1[7], respectively
- External pull-up resistors required
- I2C slave, address 4, data rate = 100 kbps
- Single application
- Wait 2 seconds for bootload command
- Other bootloader options are as set by the PSoC Creator 3.0 Bootloader Component default
- Occupies the bottom 9 Kbytes of flash

For more information on this bootloader, see the following Cypress application notes:

- AN73854, PSoC 3 and PSoC 5 LP Introduction to Bootloaders
- AN60317, PSoC 3 and PSoC 5 LP I2C Bootloader

Note that a PSoC Creator bootloadable project must be associated with .hex and .elf files for a bootloader project that is configured for the target device. Bootloader .hex and .elf files can be found at www.cypress.com/go/PSoC5LPdatasheet.

The factory-installed bootloader can be overwritten using JTAG or SWD programming.

10. Development Support

The CY8C56LP family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, to ensure that you can find answers to your questions quickly, supports the CY8C56LP family. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: PSoC Creator makes designing with PSoC as easy as dragging a peripheral onto a schematic, but, when low level details of the PSoC device are required, use the technical reference manual (TRM) as your guide.

Note Visit www.arm.com for detailed documentation about the Cortex-M3 CPU.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C56LP family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 11-7. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor	4.7 µH nominal	3.7	4.7	5.7	µH
		10 µH nominal	8.0	10.0	12.0	µH
		22 µH nominal	17.0	22.0	27.0	µH
C_{BOOST}	Total capacitance sum of V_{DDD}, V_{DDA}, V_{DDIO}[32]		17.0	26.0	31.0	µF
C_{BAT}	Battery filter capacitor		17.0	22.0	27.0	µF
I_F	Schottky diode average forward current		1.0	–	–	A
V_R	Schottky reverse voltage		20.0	–	–	V

Figure 11-8. T_A range over V_{BAT} and V_{OUT}

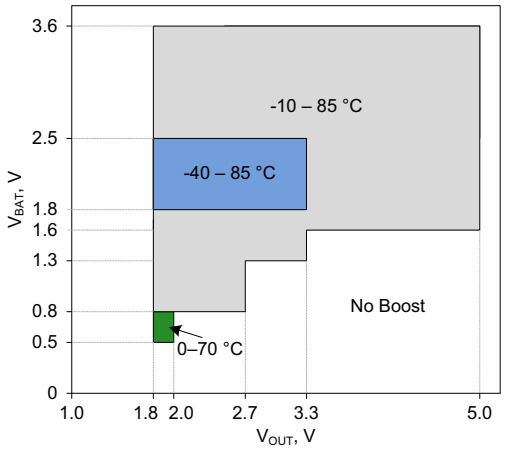


Figure 11-9. I_{OUT} range over V_{BAT} and V_{OUT}

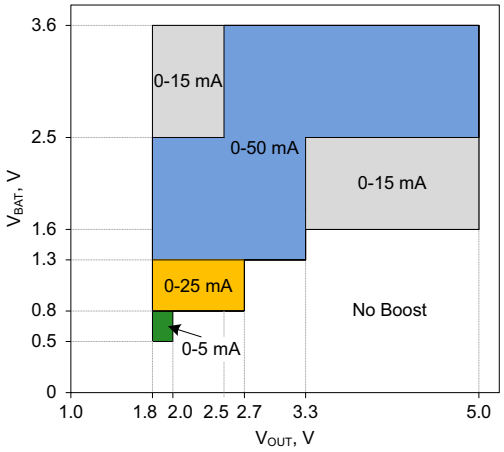
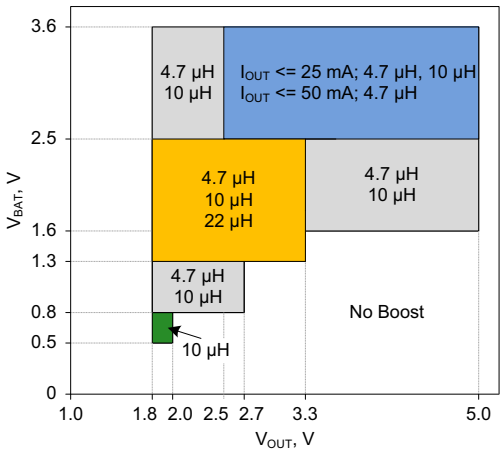


Figure 11-10. L_{BOOST} values over V_{BAT} and V_{OUT}



Note
32. Based on device characterization (Not production tested).

Table 11-11. SIO AC Specifications[39]

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%)	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	60	ns
Fsioout	SIO output operating frequency					
	2.7 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 2.7 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	2.7 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

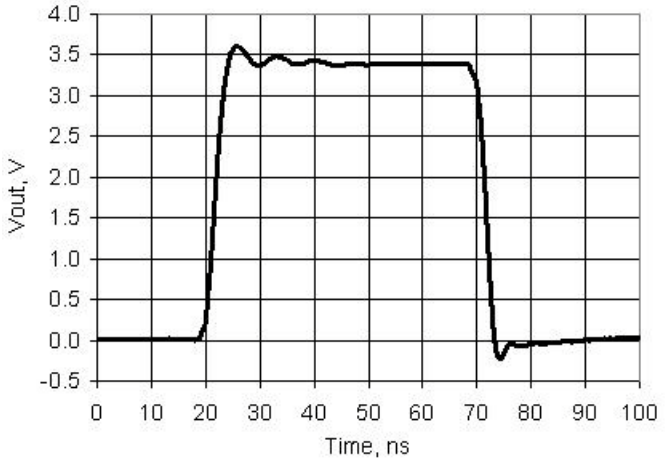
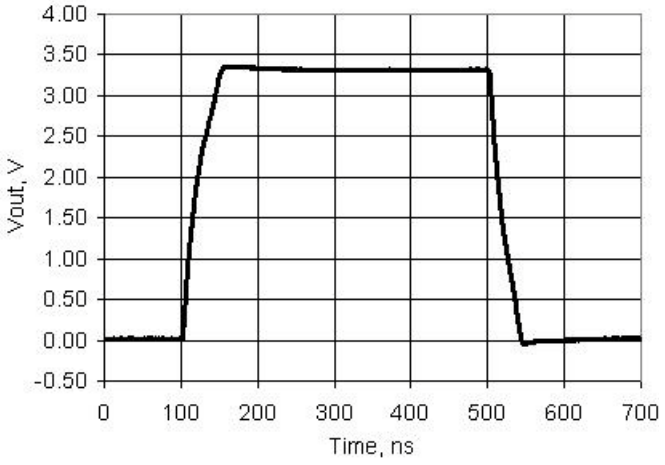


Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



Note
39. Based on device characterization (Not production tested).

Figure 11-27. Opamp Vos vs Vcommon and V_{DDA}, 25 °C

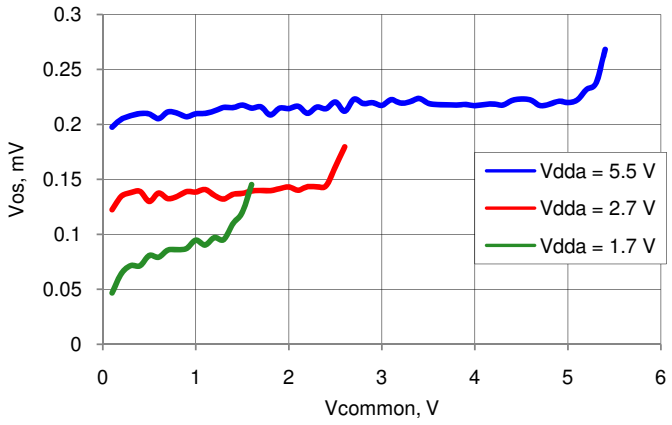


Figure 11-28. Opamp Output Voltage vs Load Current and Temperature, High Power Mode, 25 °C, V_{DDA} = 2.7 V

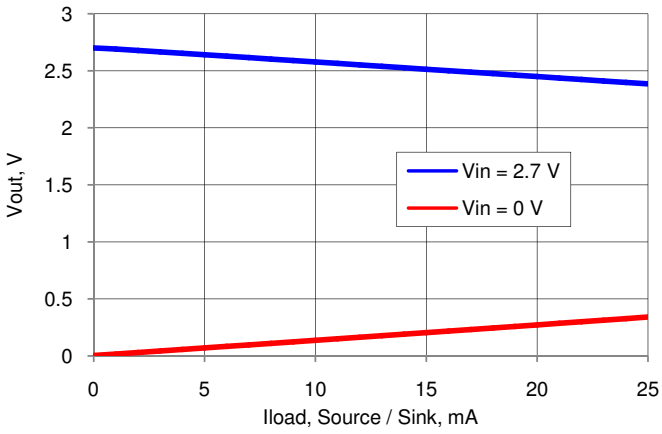


Figure 11-29. Opamp Operating Current vs V_{DDA} and Power Mode

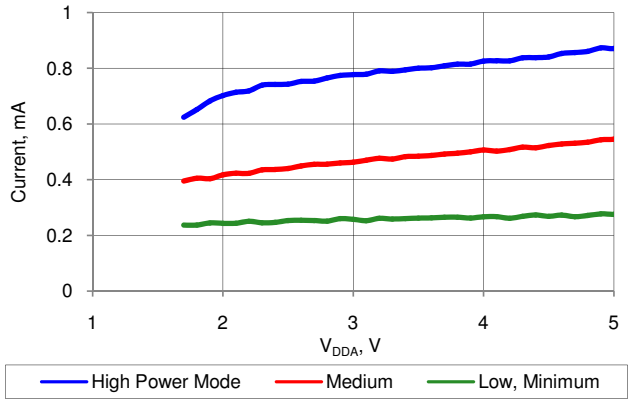


Table 11-19. Opamp AC Specifications[40]

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 15 pF load	1	–	–	MHz
		Power mode = low, 15 pF load	2	–	–	MHz
		Power mode = medium, 200 pF load	1	–	–	MHz
		Power mode = high, 200 pF load	3	–	–	MHz
SR	Slew rate, 20% - 80%	Power mode = minimum, 15 pF load	1.1	–	–	V/µs
		Power mode = low, 15 pF load	1.1	–	–	V/µs
		Power mode = medium, 200 pF load	0.9	–	–	V/µs
		Power mode = high, 200 pF load	3	–	–	V/µs
e_n	Input noise density	Power mode = high, V_{DDA} = 5 V, at 100 kHz	–	45	–	nV/sqrtHz

Note
40. Based on device characterization (Not production tested).

Figure 11-30. Opamp Noise vs Frequency, Power Mode = High, V_{DDA} = 5 V

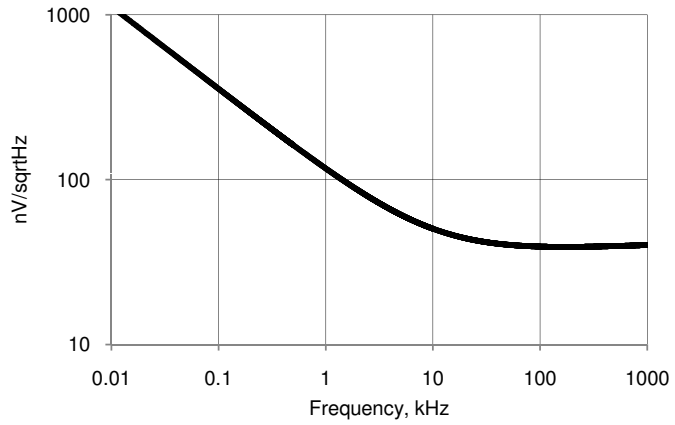


Figure 11-31. Opamp Step Response, Rising

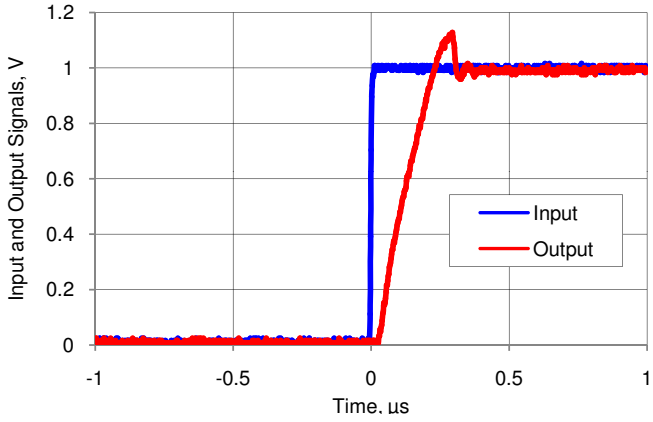


Figure 11-32. Opamp Step Response, Falling

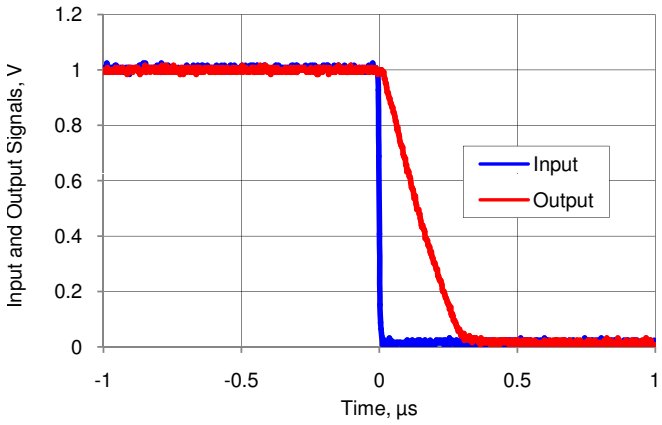


Figure 11-42. IDAC INL vs Input Code, Range = 255 µA, Source Mode

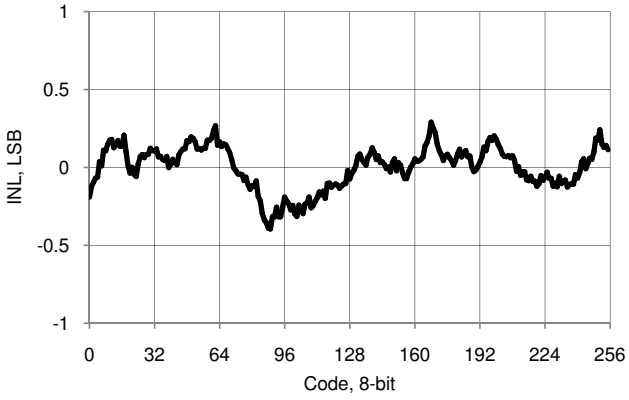


Figure 11-43. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

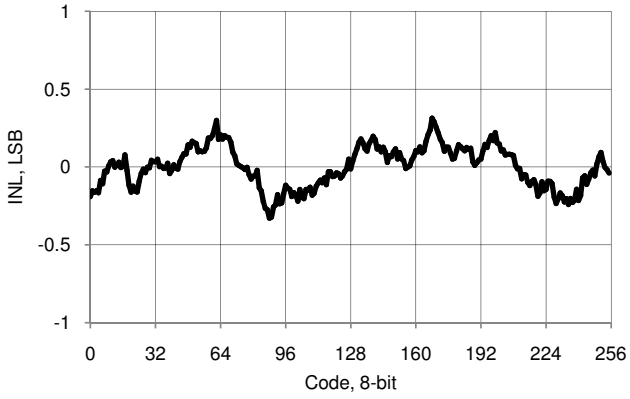


Figure 11-44. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

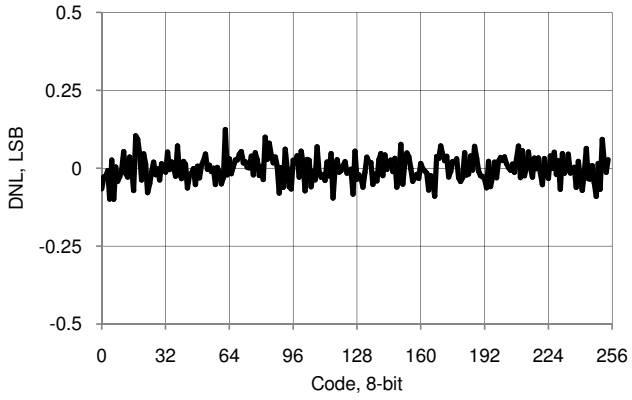


Figure 11-45. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

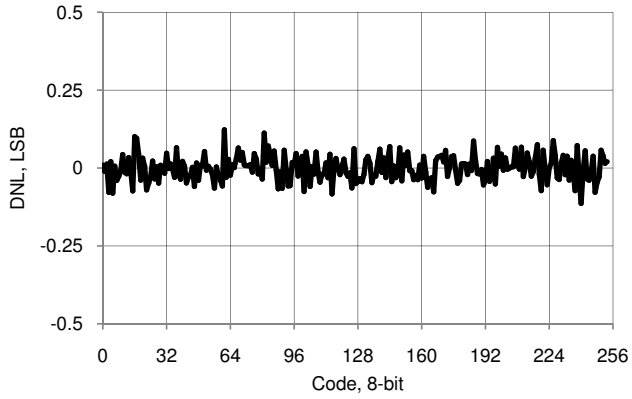


Figure 11-46. IDAC INL vs Temperature, Range = 255 µA, Fast Mode

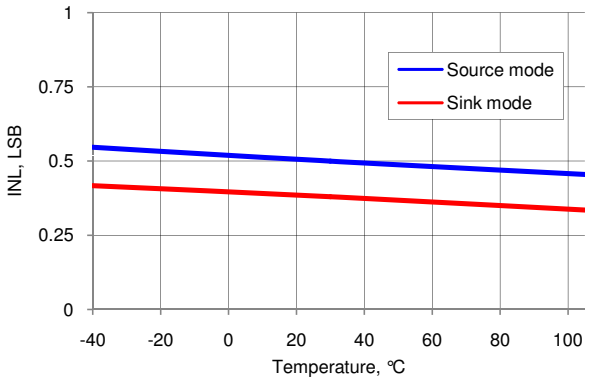
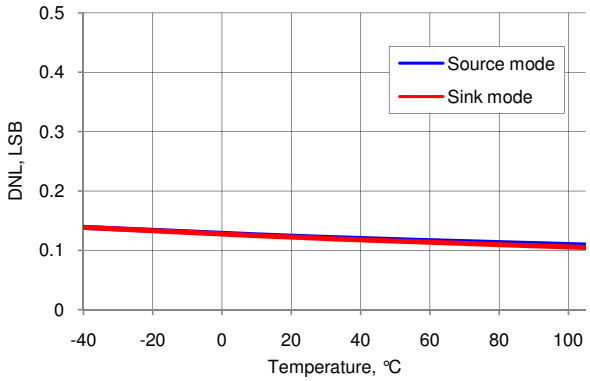


Figure 11-47. IDAC DNL vs Temperature, Range = 255 µA, Fast Mode



11.9 Clocking

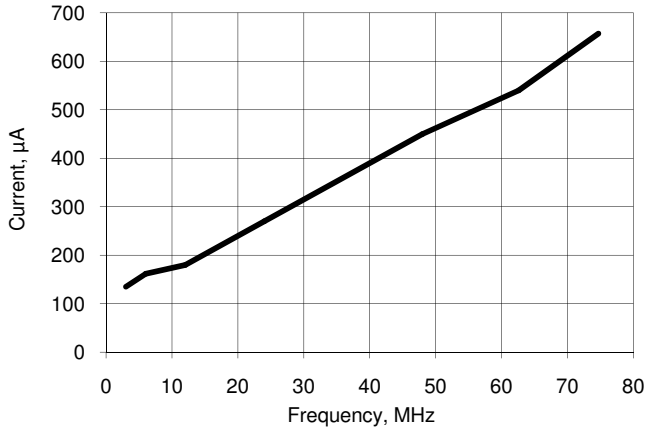
Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 Internal Main Oscillator

Table 11-75. IMO DC Specifications[86]

Parameter	Description	Conditions	Min	Typ	Max	Units
Icc_imo	Supply current					
	74.7 MHz		–	–	730	µA
	62.6 MHz		–	–	600	µA
	48 MHz		–	–	500	µA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Figure 11-76. IMO Current vs. Frequency



Note
86. Based on device characterization (Not production tested).

Table 11-76. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}[87]	IMO frequency stability (with factory trim)					
	74.7 MHz		–7	–	7	%
	62.6 MHz		–7	–	7	%
	48 MHz		–5	–	5	%
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz	0 °C to 70 °C	–1	–	1	%
		–40 °C to 105 °C	–1.5	–	1.5	%
	3 MHz frequency stability after typical PCB assembly post-reflow	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.	–	±2%	–	%
Tstart_imo	Startup time[88]	From enable (during normal system operation)	–	–	13	µs
Jp–p	Jitter (peak to peak)[88]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term)[88]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

Figure 11-77. IMO Frequency Variation vs. Temperature

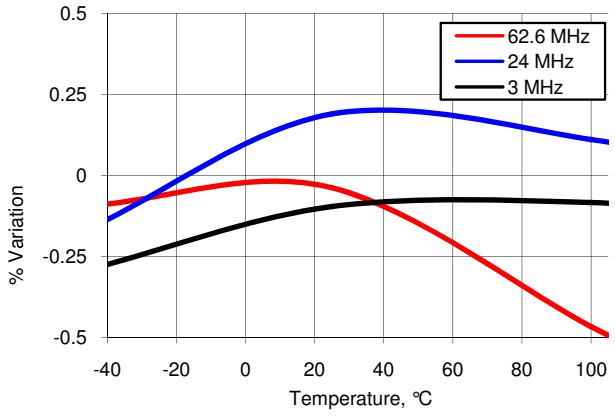
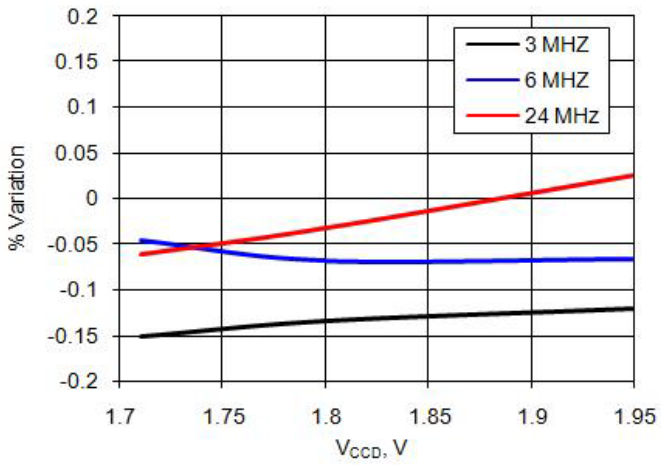
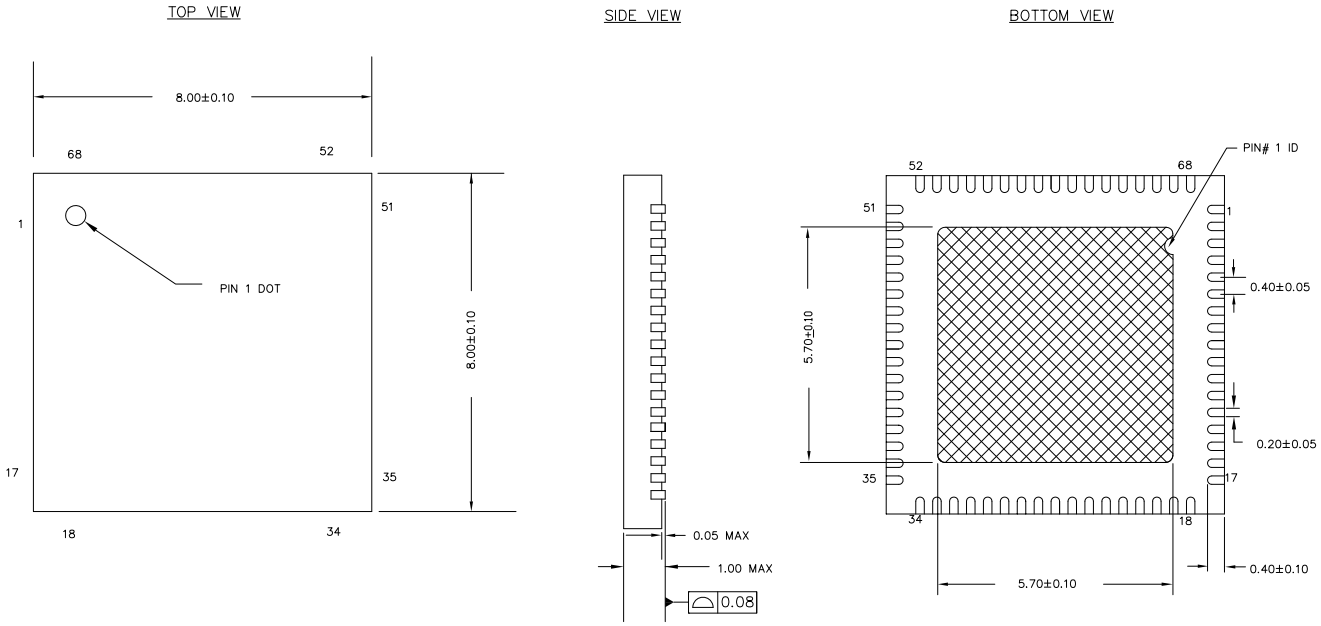


Figure 11-78. IMO Frequency Variation vs. V_{CC}



Notes
87. F_{IMO} is measured after packaging, and thus accounts for substrate and die attach stresses.
88. Based on device characterization (Not production tested).

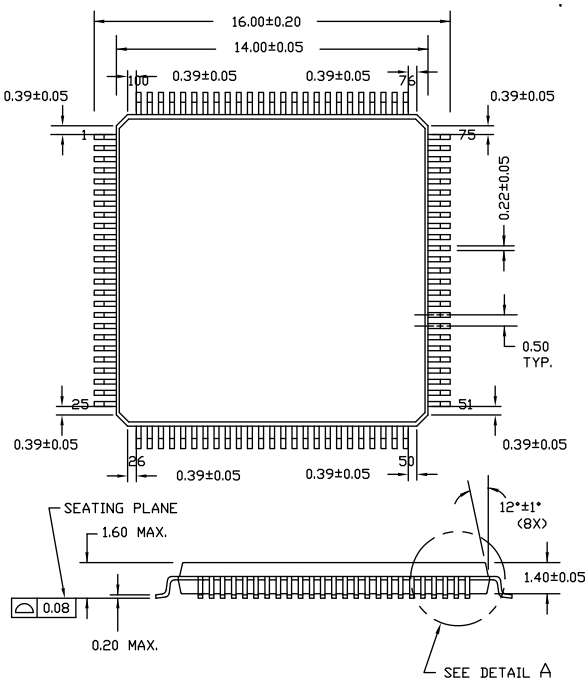
Figure 13-1. 68-pin QFN 8 × 8 with 0.4 mm Pitch Package Outline (Sawn Version)



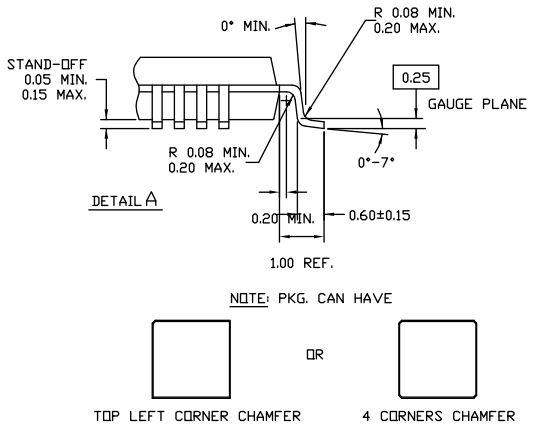
NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 13-2. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline



NOTE:
1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



51-85048 *J

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C56LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84935				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	4698847	AVER / MKEA / GJV	03/24/2015	Updated Features: Added “Extended temperature parts: –40 to 105 °C” as indented under “Temperature range (ambient)” under “Operating characteristics”. Updated System Integration: Updated Power System: Updated Boost Converter: Updated entire section. Updated Electrical Specifications: Replaced “Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.” with “Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted.” in all instances. Updated Device Level Specifications: Updated Table 11-2: Added details of I_{DD} parameter corresponding to “T = 105 °C”. Updated Figure 11-3 and Figure 11-4. Updated Power Regulators: Updated Inductive Boost Regulator: Updated Table 11-6: Updated details of V_{BAT}, I_{OUT}, V_{OUT}, Reg_{LOAD}, Reg_{LINE} parameters. Removed V_{OUT}: V_{BAT} parameter and its details. Removed Table “Inductive Boost Regulator AC Specifications”. Updated Table 11-7: Updated details of L_{BOOST}, C_{BOOST} parameters. Added C_{BAT} parameter and its details. Added Figure 11-8, Figure 11-9, Figure 11-10, Figure 11-11, Figure 11-12, Figure 11-13, Figure 11-14. Removed Figure “Efficiency vs I_{OUT} V_{BOOST} = 3.3 V, L_{BOOST} = 10 µH”. Removed Figure “Efficiency vs I_{OUT} V_{BOOST} = 3.3 V, L_{BOOST} = 22 µH”. Updated Analog Peripherals: Updated Opamp: Updated Figure 11-26. Updated Voltage Reference: Updated Table 11-23: Added details of V_{REF} parameter corresponding to condition “105 °C”. Updated Figure 11-34. Updated Current Digital-to-analog Converter (IDAC): Updated Figure 11-46, Figure 11-47, Figure 11-48, Figure 11-49, Figure 11-50, Figure 11-51. Updated Voltage Digital to Analog Converter (VDAC): Updated Figure 11-58, Figure 11-59, Figure 11-60, Figure 11-61, Figure 11-62, Figure 11-63. Updated Programmable Gain Amplifier: Updated Table 11-39: Added details of BW1 parameter corresponding to condition “T_A ≤ 105 °C”. Updated Figure 11-69. Updated Temperature Sensor: Updated Table 11-40: Replaced 85 °C with 105 °C.

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C56LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84935				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H (cont.)	4698847	AVER / MKEA / GJV	03/24/2015	Updated Electrical Specifications: Updated Memory: Updated Flash: Updated Table 11-58: Updated details in “Conditions” column corresponding to “Flash data retention time” parameter. Added Note 72 and referred the same note in last condition corresponding to “Flash data retention time” parameter. Updated EEPROM: Updated Table 11-60: Updated details in “Conditions” column corresponding to “EEPROM data retention time” parameter. Added Note 72 and referred the same note in last condition corresponding to “EEPROM data retention time” parameter. Updated Nonvolatile Latches (NVL): Updated Table 11-62: Updated details in “Conditions” column corresponding to “NVL data retention time” parameter. Added Note 73 and referred the same note in last condition corresponding to “NVL data retention time” parameter. Updated Clocking: Updated Internal Main Oscillator: Updated Table 11-76: Replaced 85 °C with 105 °C. Updated Figure 11-78. Updated Ordering Information: Updated Part Numbering Conventions: Added “Q: Extended” as sub bullet under “g: Temperature Range”. Updated Packaging: Updated Table 13-1: Changed maximum value of T_A parameter from 85 °C to 105 °C. Changed maximum value of T_J parameter from 100 °C to 120 °C. Updated : Updated : spec 001-88034 – Changed revision from ** to *A.
*I	4839323	MKEA	07/15/2015	Added reference to code examples in More Information. Updated typ value of T_{WRITE} from 2 to 10 in EEPROM AC specs table. Changed “Device supply for USB operation" to "Device supply (V_{DDD}) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for V_{DDA} and V_{DDD}. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Delta-sigma ADC DC Specifications

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support