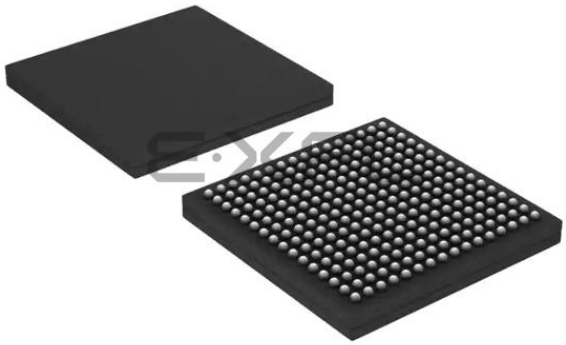

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	128
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 77x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk61fn1m0vmj15

- Communication interfaces
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB high-/full-/low-speed On-the-Go controller with ULPI interface
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect (USBDCD)
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital Host Controller (SDHC)
  - Two I2S modules

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK61 and MK61

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K61
A	Key attribute	• F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 512 = 512 KB • 1M0 = 1 MB

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{OHT_DDR}	Output high current total for DDR pins	—	—	100	mA	
	• DDR1	—	—	56	mA	
	• DDR2	—	—	39	mA	
	• LPDDR1					
V_{OH_Tamper}	Output high voltage — high drive strength	V_{BAT} – 0.5	—	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA					
	Output high voltage — low drive strength	V_{BAT} – 0.5	—	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA					
I_{OH_Tamper}	Output high current total for Tamper pins	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength		—			
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	—		0.5	V	
	Output low voltage — low drive strength		—			
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1 mA	—		0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{OLT_io60}	Output low current total for fast digital ports	—	—	100	mA	
V_{OL_DDR}	Output low voltage for DDR pins	—	—	0.37	V	
	• DDR1 (I_{OL} = 16.2 mA)	—	—	0.28	V	
	• DDR2 half strength (I_{OL} = 5.36 mA)	—	—	0.28	V	
	• DDR2 full strength (I_{OL} = 13.4 mA)	—	—	0.1 x V_{DD_DDR}	V	
	• LPDDR1 half strength (I_{OL} = 0.1 mA)	—	—	0.1 x V_{DD_DDR}	V	
	• LPDDR1 full strength (I_{OL} = 0.1 mA)					
I_{OLT_DDR}	Output low current total for DDR pins	—	—	100	mA	
	• DDR1			56	mA	
	• DDR2			39	mA	
	• LPDDR1					
V_{OL_Tamper}	Output low voltage — high drive strength	—	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA					
	Output low voltage — low drive strength	—	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA					

Table continues on the next page...

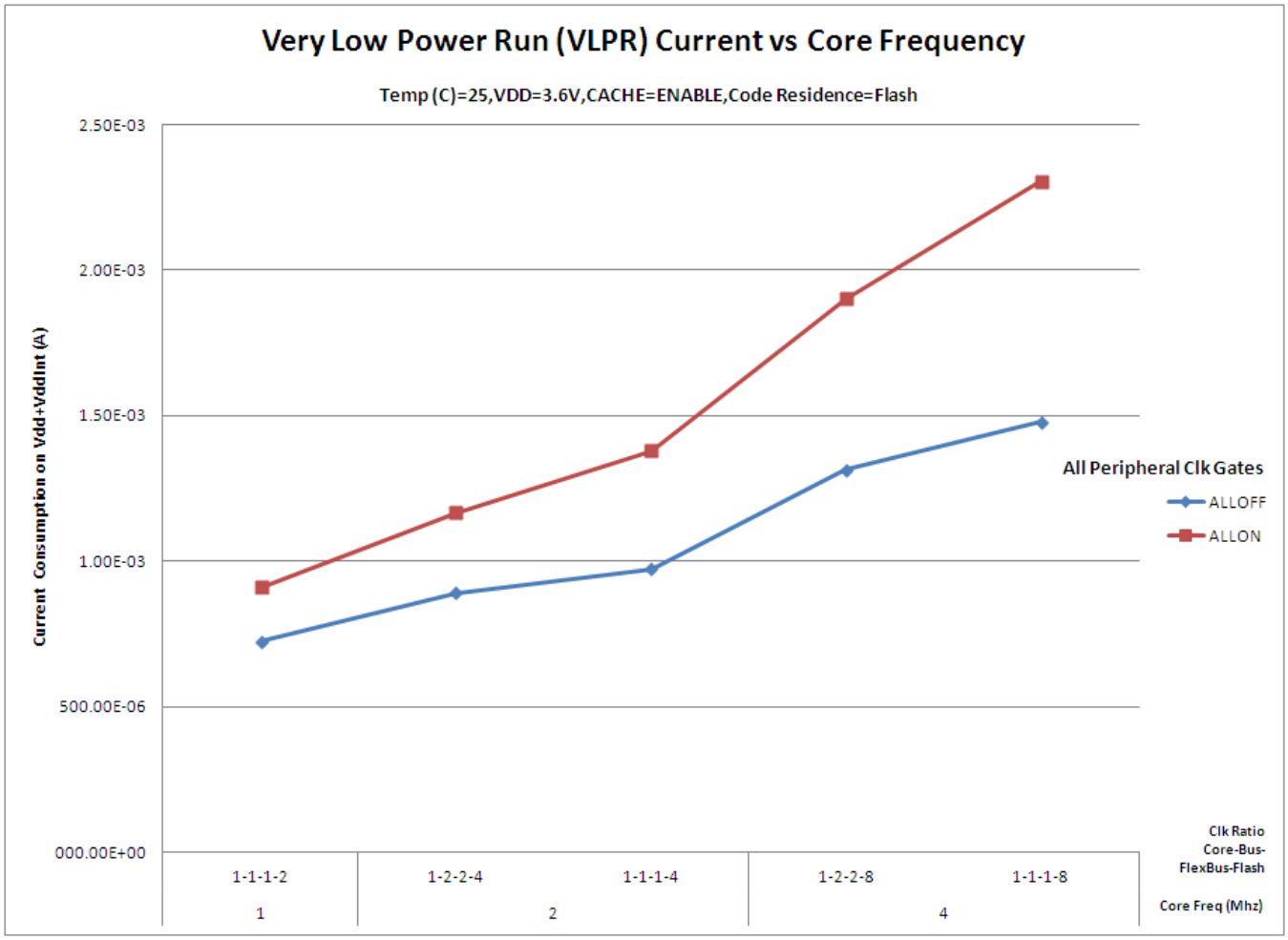

Figure 4. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 256MAPBGA

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	21	dBµV	1, 2, 3
V_{RE2}	Radiated emissions voltage, band 2	50–150	24	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	29	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	28	dBµV	

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 72 MHz, f_{BUS} = 72 MHz
3. Determined according to IEC Standard JESD78, *IC Latch-Up Test*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	150	MHz	
f_{SYS_USBFS}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{SYS_USBHS}	System and core clock when High Speed USB in operation	60	—	MHz	
f_{ENET}	System and core clock when ethernet in operation • 10 Mbps • 100 Mbps	 5 50	 — —	MHz	
f_{BUS}	Bus clock	—	75	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{DDR}	DDR clock	—	150	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					

Table continues on the next page...

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 4.5	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	180	—	ps	

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	70	150	µs	
$t_{swapx04}$	• control code 0x04	—	70	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	
	Program Partition for EEPROM execution time					
$t_{pgmpart64k}$	• 64 KB EEPROM backup	—	235	—	ms	
$t_{pgmpart256k}$	• 256 KB EEPROM backup	—	240	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	205	—	µs	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.6	2.5	ms	
$t_{setram128k}$	• 128 KB EEPROM backup	—	2.7	3.8	ms	
$t_{setram256k}$	• 256 KB EEPROM backup	—	4.8	6.2	ms	
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	140	225	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b64k}$	• 64 KB EEPROM backup	—	400	1700	µs	
$t_{eewr8b128k}$	• 128 KB EEPROM backup	—	450	1800	µs	
$t_{eewr8b256k}$	• 256 KB EEPROM backup	—	525	2000	µs	
$t_{eewr16bers}$	16-bit write to erased FlexRAM location execution time	—	140	225	µs	
	16-bit write to FlexRAM execution time:					
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	400	1700	µs	
$t_{eewr16b128k}$	• 128 KB EEPROM backup	—	450	1800	µs	
$t_{eewr16b256k}$	• 256 KB EEPROM backup	—	525	2000	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	180	275	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	475	1850	µs	
$t_{eewr32b128k}$	• 128 KB EEPROM backup	—	525	2000	µs	
$t_{eewr32b256k}$	• 256 KB EEPROM backup	—	600	2200	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

Table 26. DDR controller — AC timing specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• DDR2 • LPDDR	6.6	20	ns	
V_{OX-AC}	DDRCK AC differential cross point voltage • DDR1 • DDR2 • LPDDR	0.5 x V_{DD_DDR} – 0.2 V 0.5 x V_{DD_DDR} – 0.125 V 0.4 x V_{DD_DDR}	0.5 x V_{DD_DDR} + 0.2 V 0.5 x V_{DD_DDR} + 0.125 V 0.4 x V_{DD_DDR}	V V V	
t_{DDRCKH}	Pulse width high	0.45	0.55	t_{DDRCK}	3
t_{DDRCKL}	Pulse width low	0.45	0.55	t_{DDRCK}	3
t_{CMV}	Address, DDR_CKE, $\overline{\text{DDR\_CAS}}$, $\overline{\text{DDR\_RAS}}$, $\overline{\text{DDR\_WE}}$, $\overline{\text{DDR\_CSn}}$ — output setup	0.5 x t_{DDRCK} – 1	—	ns	4
t_{CMH}	Address, DDR_CKE, $\overline{\text{DDR\_CAS}}$, $\overline{\text{DDR\_RAS}}$, $\overline{\text{DDR\_WE}}$, $\overline{\text{DDR\_CSn}}$ — output hold	0.5 x t_{DDRCK} – 1	—	ns	
t_{DQSS}	DQS rising edge to CK rising edge	-0.2 x t_{DDRCK}	0.2 x t_{DDRCK}	ns	
t_{QS}	Data and data mask output setup (DQ→DQS) relative to DQS (DDR write mode)	0.25 x t_{DDRCK} – 1	—	ns	5, 6
t_{QH}	Data and data mask output hold (DQS→DQ) relative to DQS (DDR write mode)	0.25 x t_{DDRCK} – 1	—	ns	7
t_{DQSQ}	DQS-DQ skew for DQS and associated DQ signals	– (0.25 x t_{DDRCK} – 1)	0.25 x t_{DDRCK} – 1	ns	8

1. This is minimum frequency of operation according to JEDEC DDR2 specification.
2. DDR data rate = 2 x DDR clock frequency
3. Pulse width high plus pulse width low cannot exceed min and max clock period.
4. Command output setup should be 1/2 the memory bus clock (t_{DDRCK}) plus some minor adjustments for process, temperature, and voltage variations.
5. This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. DDR_DQ[15:8] is relative to DDR_DQS[1]; DDR_DQ[7:0] is relative to DDR_DQS[0].
6. The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.
7. This specification relates to the required hold time of DDR memories. DDR_DQ[15:8] is relative to DDR_DQS[1]; DDR_DQ[7:0] is relative to DDR_DQS[0]
8. Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

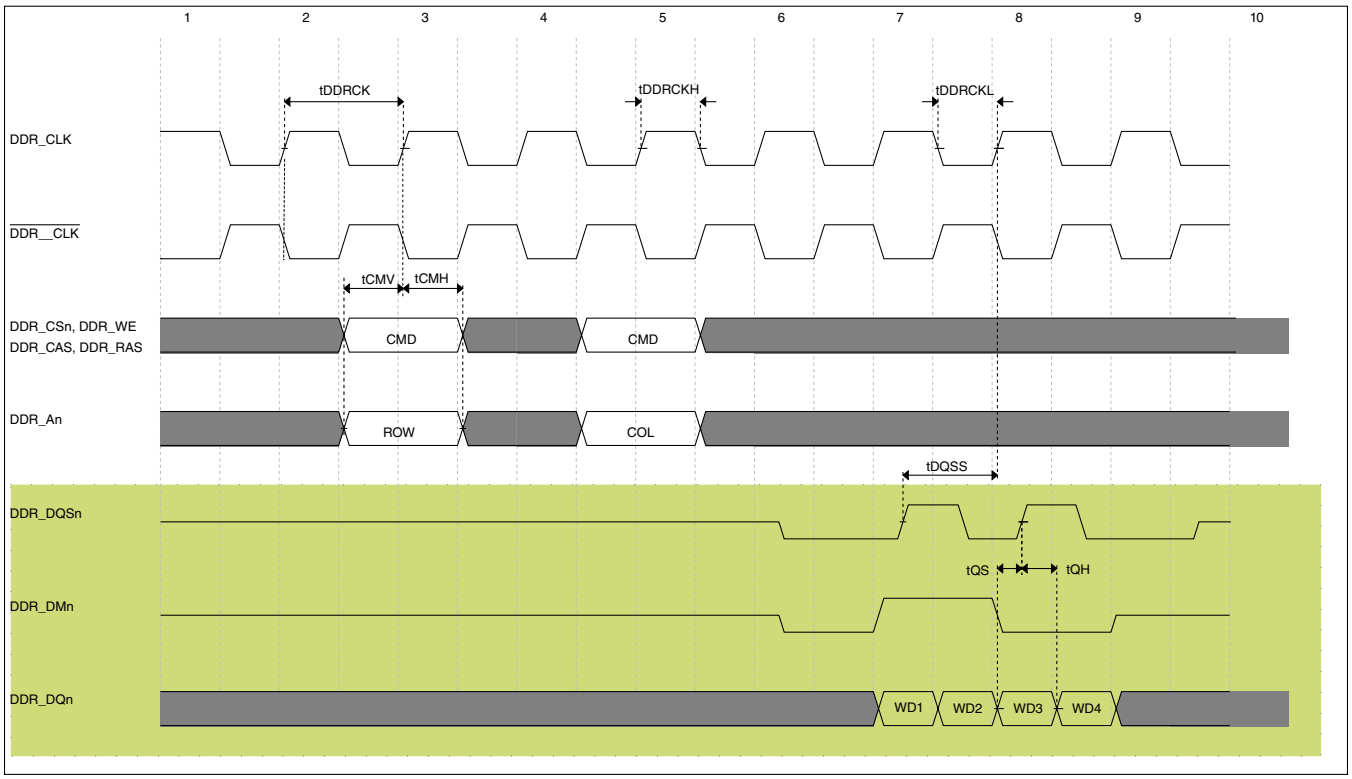

Figure 18. DDR write timing

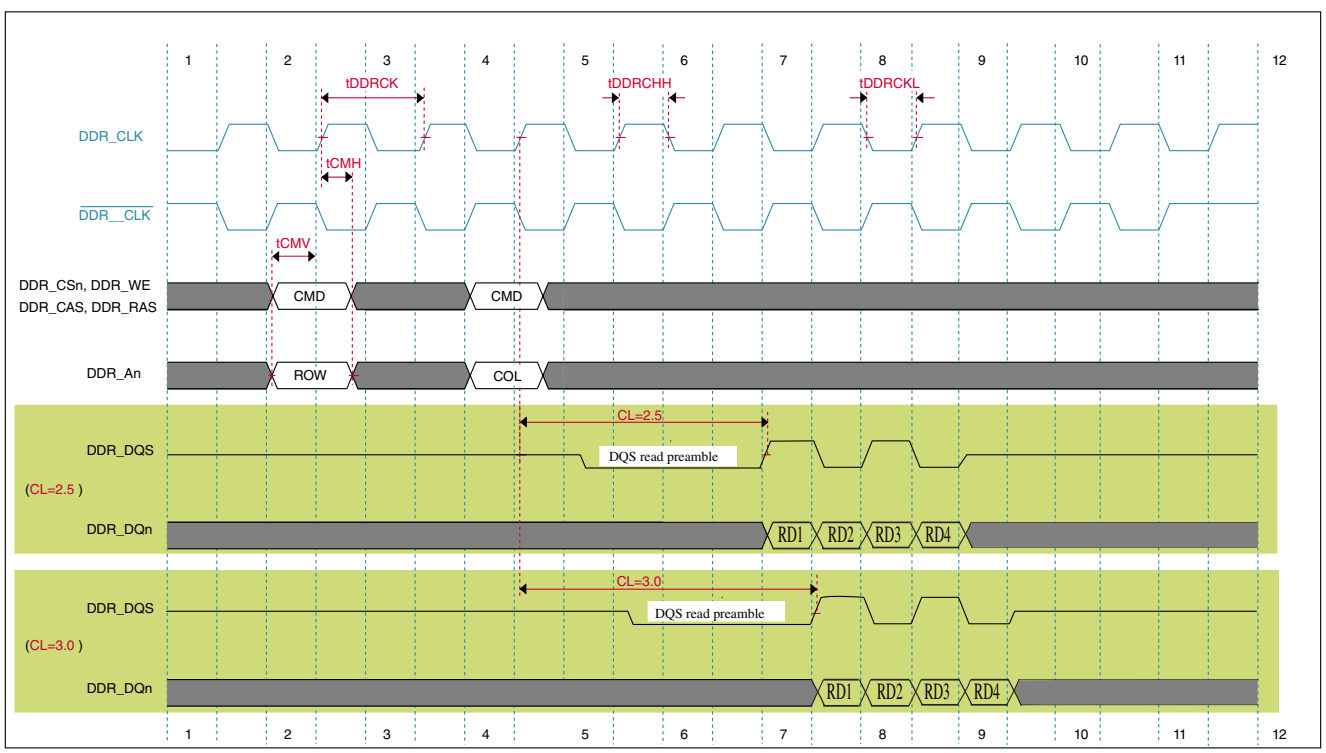

Figure 19. DDR read timing

Table 28. Flexbus full voltage range switching specifications (continued)

Num	Description	Min.	Max.	Unit	Notes
FB4	Data and FB_TA input setup	13.7	—	ns	2
FB5	Data and FB_TA input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

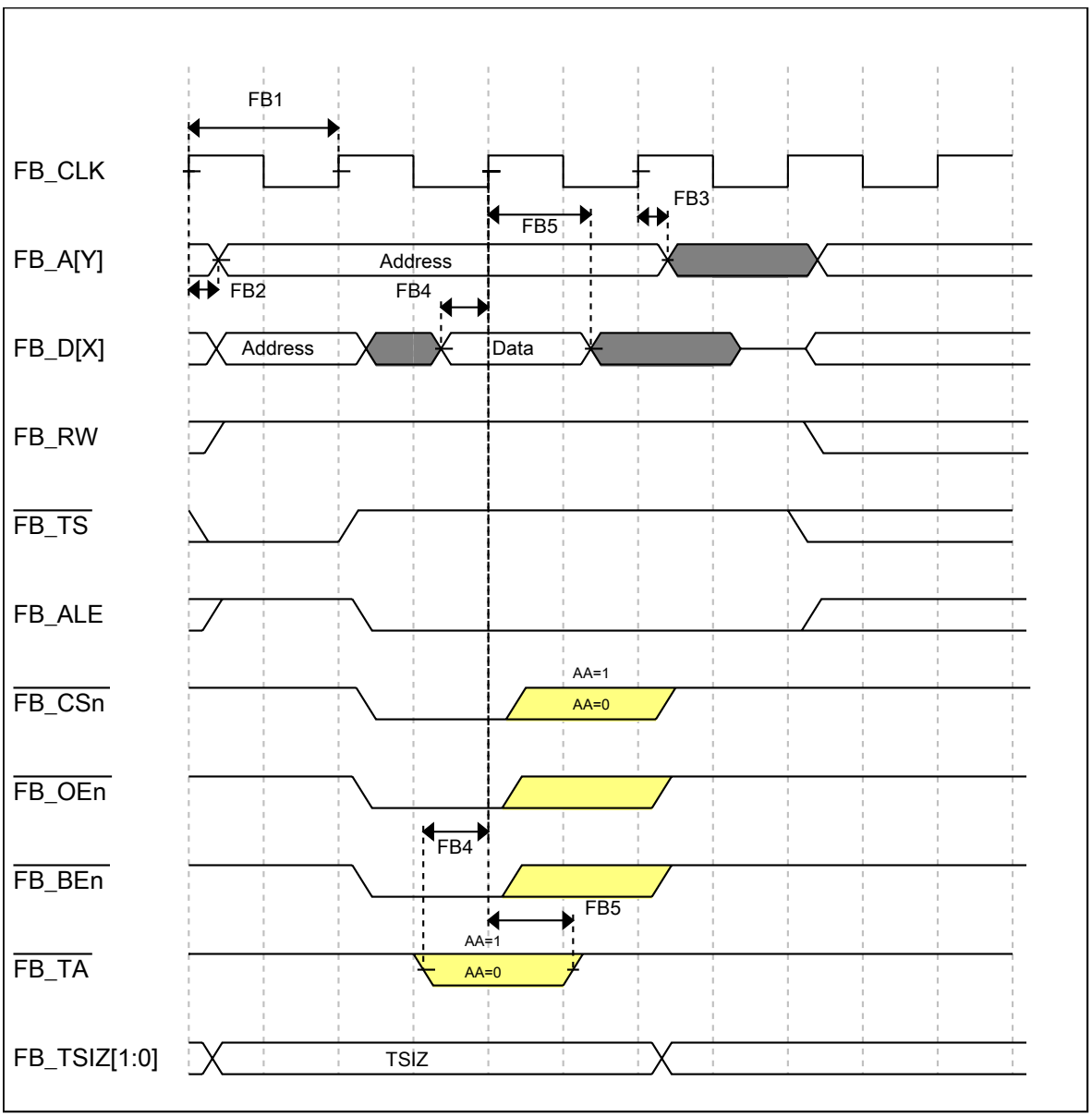

Figure 21. FlexBus read timing diagram

Table 30. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• Avg = 32					
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

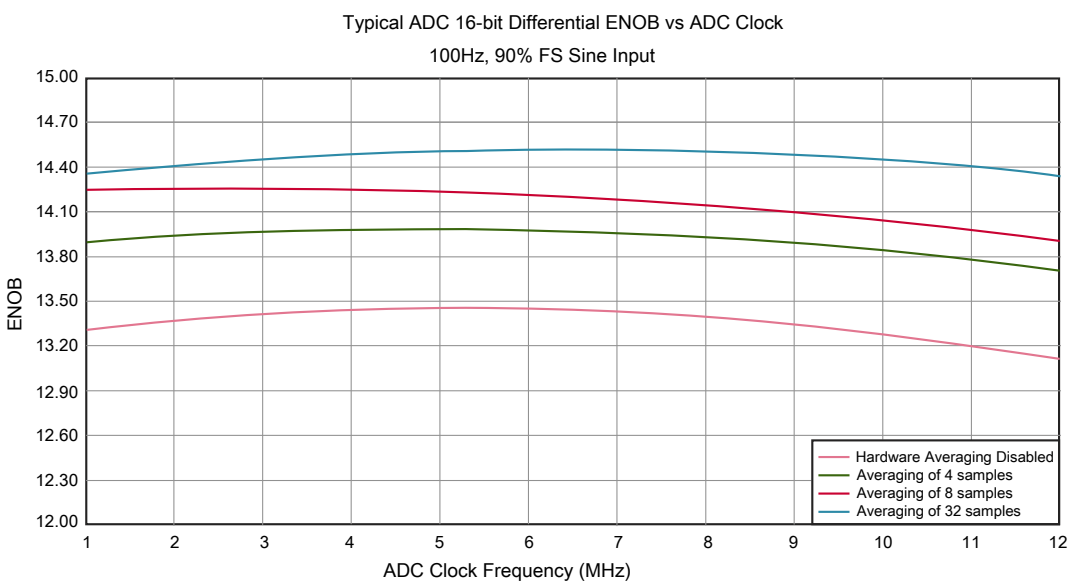

Figure 24. Typical ENOB vs. ADC_CLK for 16-bit differential mode

Table 32. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
							f_{VDDA}= 50Hz, 60Hz
CMRR	Common mode rejection ratio	• Gain=1 • Gain=64	— —	-84 -85	— —	dB dB	V_{CM}= 500mVpp, f_{VCM}= 50Hz, 100Hz
V_{OFS}	Input offset voltage	• Chopping disabled (ADC_PGA[PGACHPb] =1) • Chopping enabled (ADC_PGA[PGACHPb] =0)	— —	2.4 0.2	— —	mV mV	Output offset = V_{OFS}*(Gain+1)
T_{GSW}	Gain switching settling time		—	—	10	µs	5
dG/dT	Gain drift over full temperature range	• Gain=1 • Gain=64	— —	6 31	10 42	ppm/°C ppm/°C	
dG/dV_{DDA}	Gain drift over supply voltage	• Gain=1 • Gain=64	— —	0.07 0.14	0.21 0.31	%/V %/V	V_{DDA} from 1.71 to 3.6V
E_{IL}	Input leakage error	All modes	$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
$V_{PP,DIFF}$	Maximum differential input signal swing		$\left(\frac{(\min(V_X, V_{DDA}-V_X)-0.2)\times 4}{\text{Gain}}\right)$ where $V_X = V_{REFPGA} \times 0.583$			V	6
SNR	Signal-to-noise ratio	• Gain=1 • Gain=64	80 52	90 66	— —	dB dB	16-bit differential mode, Average=32
THD	Total harmonic distortion	• Gain=1 • Gain=64	85 49	100 95	— —	dB dB	16-bit differential mode, Average=32, f_{in}=100Hz
SFDR	Spurious free dynamic range	• Gain=1 • Gain=64	85 53	105 88	— —	dB dB	16-bit differential mode, Average=32, f_{in}=100Hz
ENOB	Effective number of bits	• Gain=1, Average=4 • Gain=1, Average=8 • Gain=64, Average=4 • Gain=64, Average=8	11.6 8.0 7.2 6.3 12.8	13.4 13.6 9.6 9.6 14.5	— — — — —	bits bits bits bits bits	16-bit differential mode,f_{in}=100Hz

Table continues on the next page...

Table 33. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

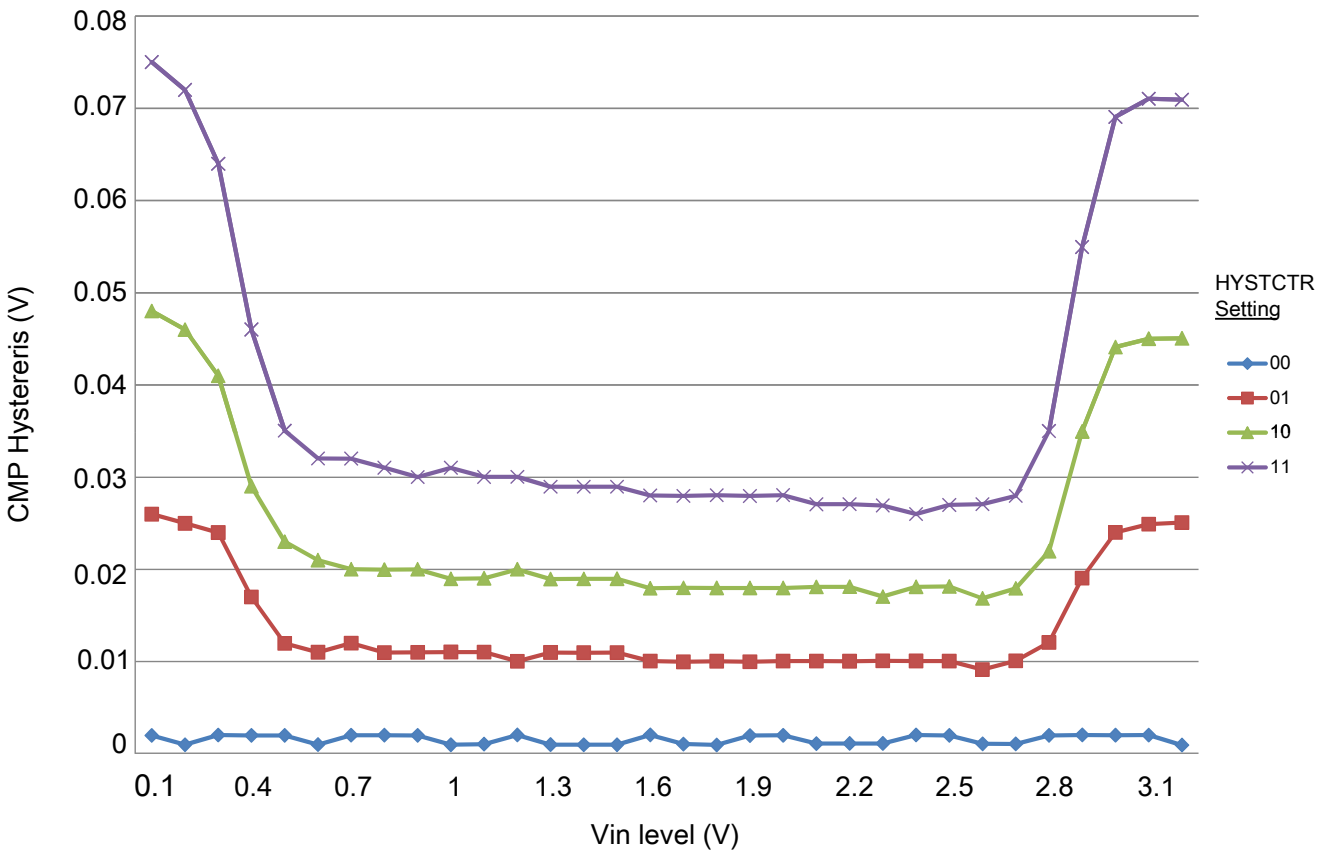

Figure 26. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

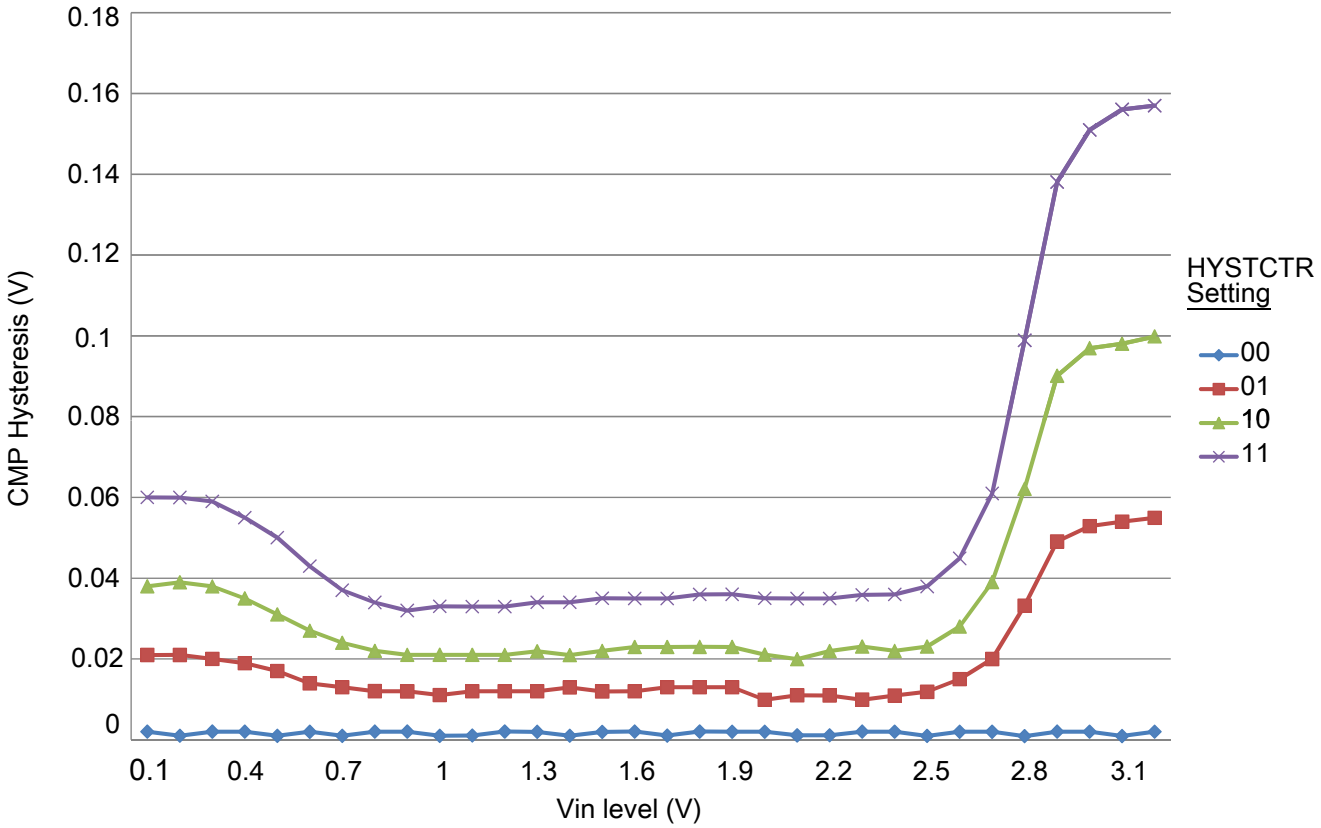

Figure 27. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 34. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

Table 51. SDHC switching specifications over the full operating voltage range

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
		Card input clock			
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
		SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)			
SD6	t_{OD}	SDHC output delay (output valid)	-5	6.5	ns
		SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)			
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	1.3	—	ns

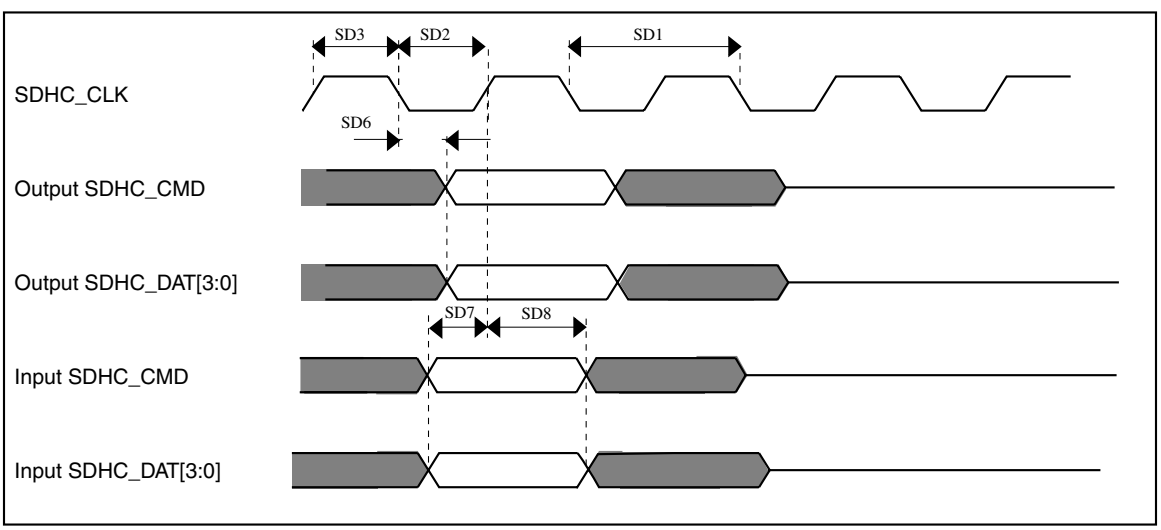

Figure 38. SDHC timing

6.8.12 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP]

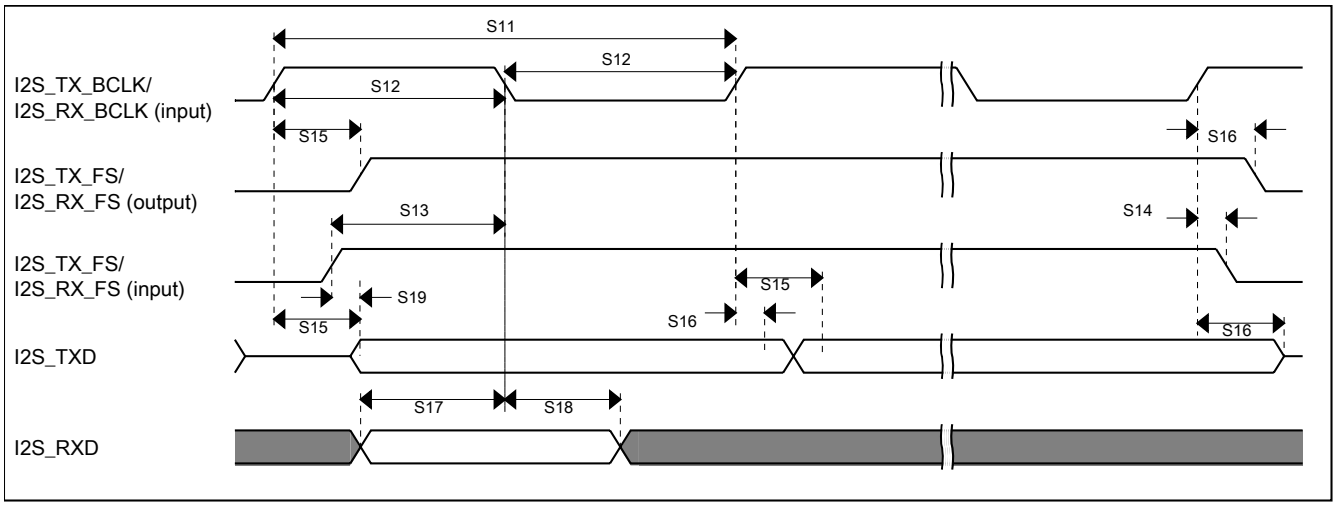

Figure 40. I2S/SAI timing — slave modes

6.8.12.2 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 54. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

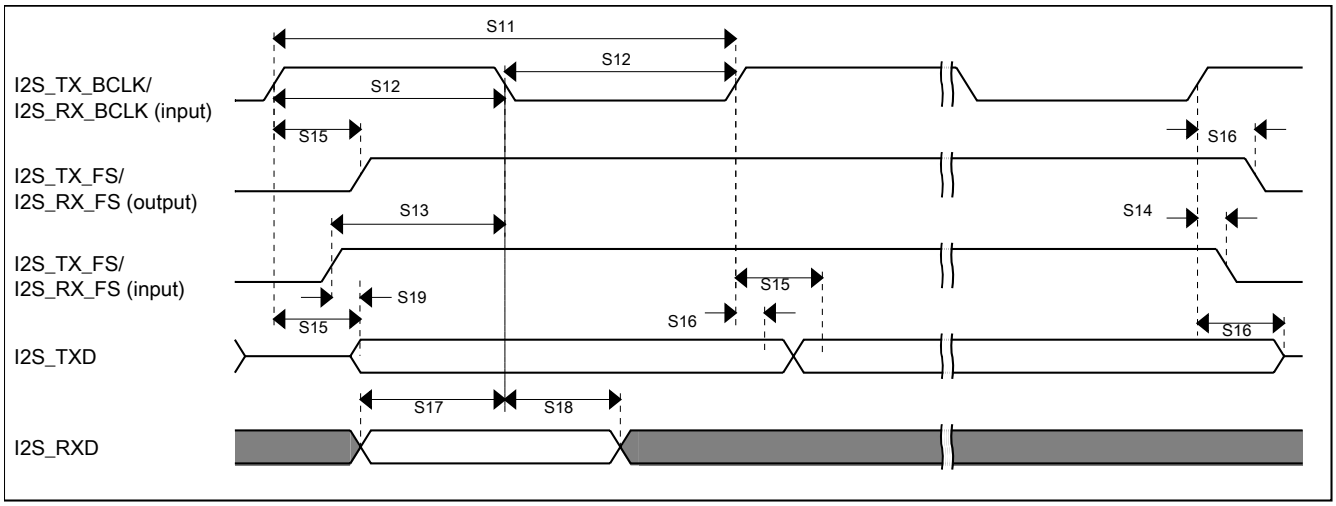

Figure 42. I2S/SAI timing — slave modes

6.8.12.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 56. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	-1.6	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

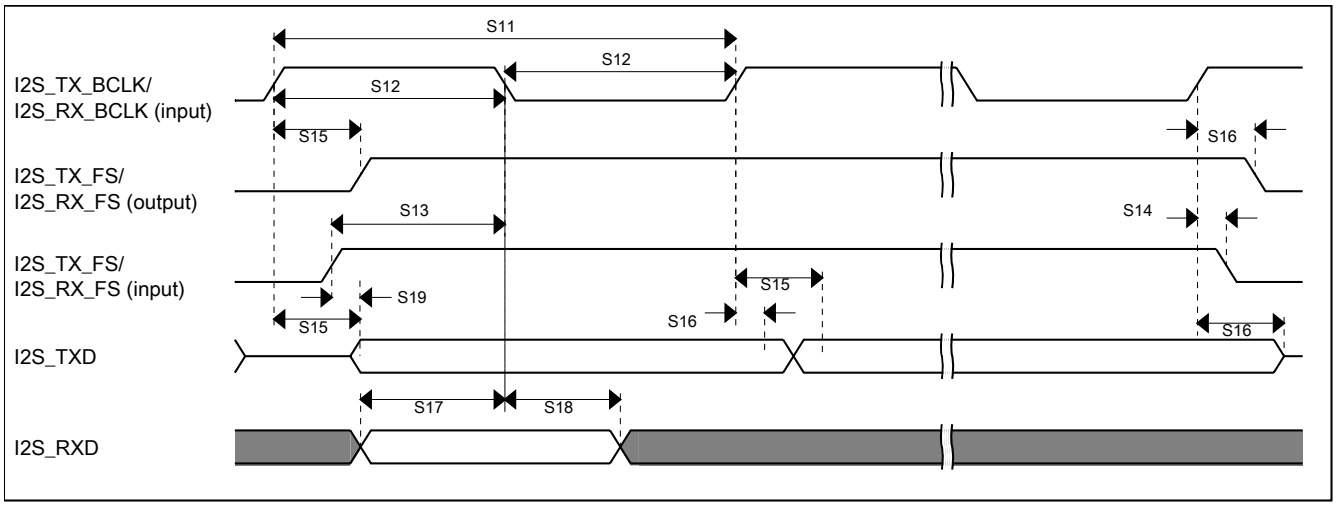

Figure 44. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 58. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f_{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C_{REF}	Internal reference capacitor	—	1	—	pF	
V_{DELTA}	Oscillator delta voltage	—	600	—	mV	2, 5
I_{REF}	Reference oscillator current source base current • 2 µA setting (REFCHRG = 0) • 32 µA setting (REFCHRG = 15)	— —	2 36	3 50	µA	2, 6
I_{ELE}	Electrode oscillator current source base current • 2 µA setting (EXTCHRG = 0) • 32 µA setting (EXTCHRG = 15)	— —	2 36	3 50	µA	2, 7
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	—	—	16	bits	
T_{Con20}	Response time @ 20 pF	8	15	25	µs	12
I_{TSI_RUN}	Current added in run mode	—	55	—	µA	
I_{TSI_LP}	Low power mode current adder	—	1.3	2.5	µA	13

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. REFCHRG = 2, EXTCHRG=0.
4. REFCHRG = 0, EXTCHRG = 10.
5. V_{DD} = 3.0 V.
6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN)

    The typical value is calculated with the following configuration:

    I_{ext} = 6 µA (EXTCHRG = 2), PS = 128, NSCN = 2, I_{ref} = 16 µA (REFCHRG = 7), C_{ref} = 1.0 pF

    The minimum value is calculated with the following configuration:

    I_{ext} = 2 µA (EXTCHRG = 0), PS = 128, NSCN = 32, I_{ref} = 32 µA (REFCHRG = 15), C_{ref} = 0.5 pF

    The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.
12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
256-pin MAPBGA	98ASA00346D

8 Pinout

8.1 Pins with active pull control after reset

The following pins are actively pulled up or down after reset:

Table 60. Revision History

Rev. No.	Date	Substantial Changes
3	3/2012	Initial public release
4	10/2012	Replaced TBDs throughout.
5	10/2013	Changes for 4N96B mask set: • Min VDD operating requirement specification updated to support operation down to 1.71V. New specifications: • Updated Vdd_ddr min specification. • Added Vodpu specification. • Removed Ioz, Ioz_ddr, and Ioz_tamper Hi-Z leakage specfications. They have been replaced by new Iina, Iind, and Zind specifications. • Fpll_ref_acc specification has been added. • I^2C module was previously covered by the general switching specifications. To provide more detail on I^2C operation a dedicated Inter-Integrated Circuit Interface (I^2C) timing section has been added. Modified specifications: • Vref_ddr max spec has been updated. • Tpor spec has been split into two specifications based on VDD slew rate. • Trd1allx and Trd1alln max have been updated. • 16-bit ADC Temp sensor slope and Temp sensor voltage (Vtemp25) have been modified. The typical values that were listed previously have been updated, and min and max specifications have been added. Corrections: • Some versions of the datasheets listed incorrect clock mode information in the "Diagram: Typical IDD_RUN operating behavior section." These errors have been corrected. • Fintf_ft specification was previously shown as a max value. It has been corrected to be shown as a typical value as originally intended. • Corrected DDR write and read timing diagrams to show the correct location of the Tcmv specification. • SDHC peripheral 50MHz high speed mode options were left out of the last datasheet. These have been added to the SDHC specifications section.
6	09/2015	• Updated Power Sequencing section • Added footnote to ambient temperature specification of Thermal Operating requirements • Updated the data and DQS waveforms in DDR read timing diagram • Removed "USB HS/LS/FS on-the-go controller with on-chip high speed transceiver" from features section • Updated Terminology and guidelines section • Updated the footnotes and the values of Power consumption operating behaviors table • Added Notes in USB electrical specification section • Updated I2C timing table