Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	16MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.25V ~ 2.75V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12t64mpke16

Table of Contents

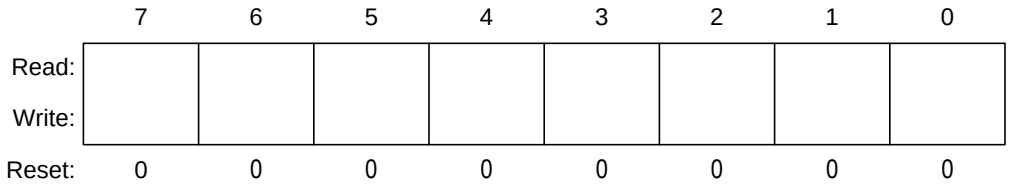

Figure 3 Accumulator A

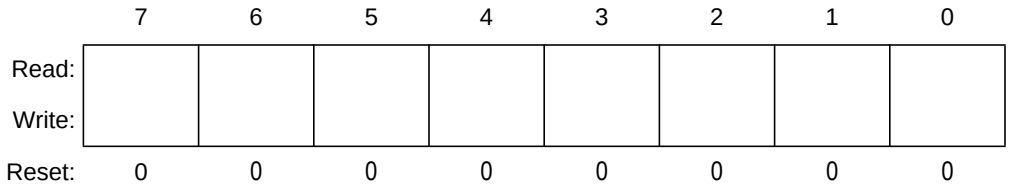

Figure 4 Accumulator B

Most operations can use accumulator A or B interchangeably. However, there are a few exceptions. Add, subtract, and compare instructions involving both A and B (ABA, SBA, and CBA) only operate in one direction, so it is important to verify that the correct operand is in the correct accumulator. The decimal adjust accumulator A (DAA) instruction is used after binary-coded decimal (BCD) arithmetic operations. There is no equivalent instruction to adjust accumulator B.

Index Registers (X and Y)

16-bit index registers X and Y are used for indexed addressing. In indexed addressing, the contents of an index register are added to a 5-bit, 9-bit, or 16-bit constant or to the contents of an accumulator to form the effective address of the instruction operand. Having two index registers is especially useful for moves and in cases where operands from two separate tables are used in a calculation.

Table 19 MC9S12T64 Register Map (Continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0	CRG
		Write:									
$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0	
		Write:									
$0036	Reserved for Factory Test	Read:	Reads to this register return unpredictable values.								
		Write:									
$0037	CRGFLG	Read:	RTIF	PORLVDRF	0	LOCKIF	LOCK	TRACK	SCMIF	SCM	
		Write:									
$0038	CRGINT	Read:	RTIE	0	0	LOCKIE	0	0	SCMIE	0	
		Write:									
$0039	CLKSEL	Read:	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI	
		Write:									
$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME	
		Write:									
$003B	RTICTL	Read:	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0	
		Write:									
$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0	
		Write:									
$003D	Reserved for Factory Test	Read:	Reads to this register return unpredictable values.								
		Write:									
$003E	Reserved for Factory Test	Read:	Reads to this register return unpredictable values.								
		Write:									
$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0	
		Write:	Bit 7	6	5	4	3	2	1	Bit 0	

Operating Modes

Contents

Introduction

Eight possible operating modes determine the operating configuration of the MC9S12T64. Each mode has an associated default memory map and external bus configuration.

Operating Modes

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (refer to Table 20).

The MODC, MODB, and MODA bits in the MODE register show current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

NOTE: *The address bit AB0 is not stored, since no byte access from this register is possible. For sector erase, the MCU address bits AB[8:0] are don't care. For mass erase, any address within the block is valid to start the command.*

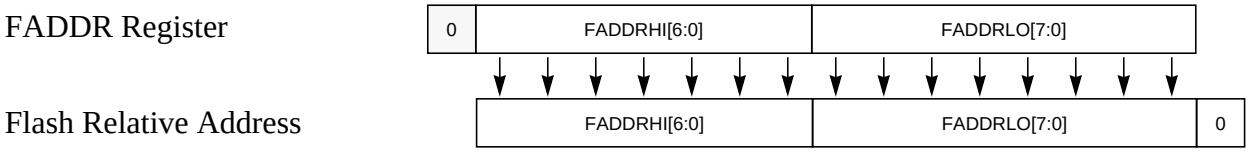

Figure 26 FADDR Address Mapping to Flash Relative Address

External Pin Descriptions

This module does not have external pins relevant for the user.

Module Memory Map

Overview

The memory data is accessible in the address range $1000 - $17FF after reset and can be re-mapped to any 2k byte boundary within the MCU address space. The CALRAM module contains a control register in the same address space INITRG +$0FC - INITRG +$0FF.

Data Memory Map

CALRAM array can be mapped to any 2K byte boundary within the 64K byte address space. The CALRAM array address can be changed anytime through the INITCRM register.

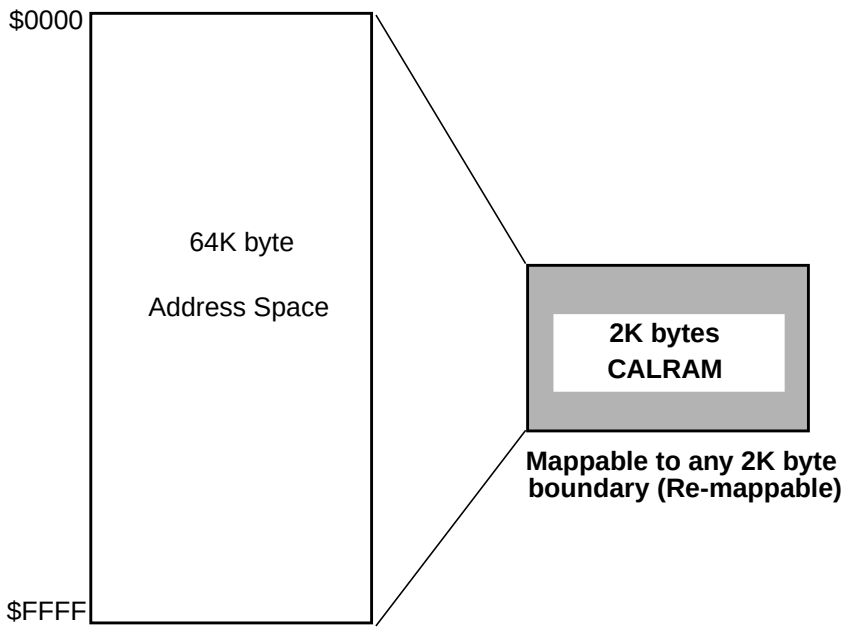

Figure 32 CALRAM Data Memory Map

Register Memory Map

Register name		Bit 7	6	5	4	3	2	1	Bit 0	Addr. Offset
CALCFG	Read:	FSUM	0	0	0	0	0	0	0	$00FC
	Write:									
Reserved	Read:	0	0	0	0	0	0	0	0	$00FD-$00FF
	Write:									

= Unimplemented or reserved

NOTE: *Register Address = Base Address (INITRG) + Address Offset*

Block Diagram

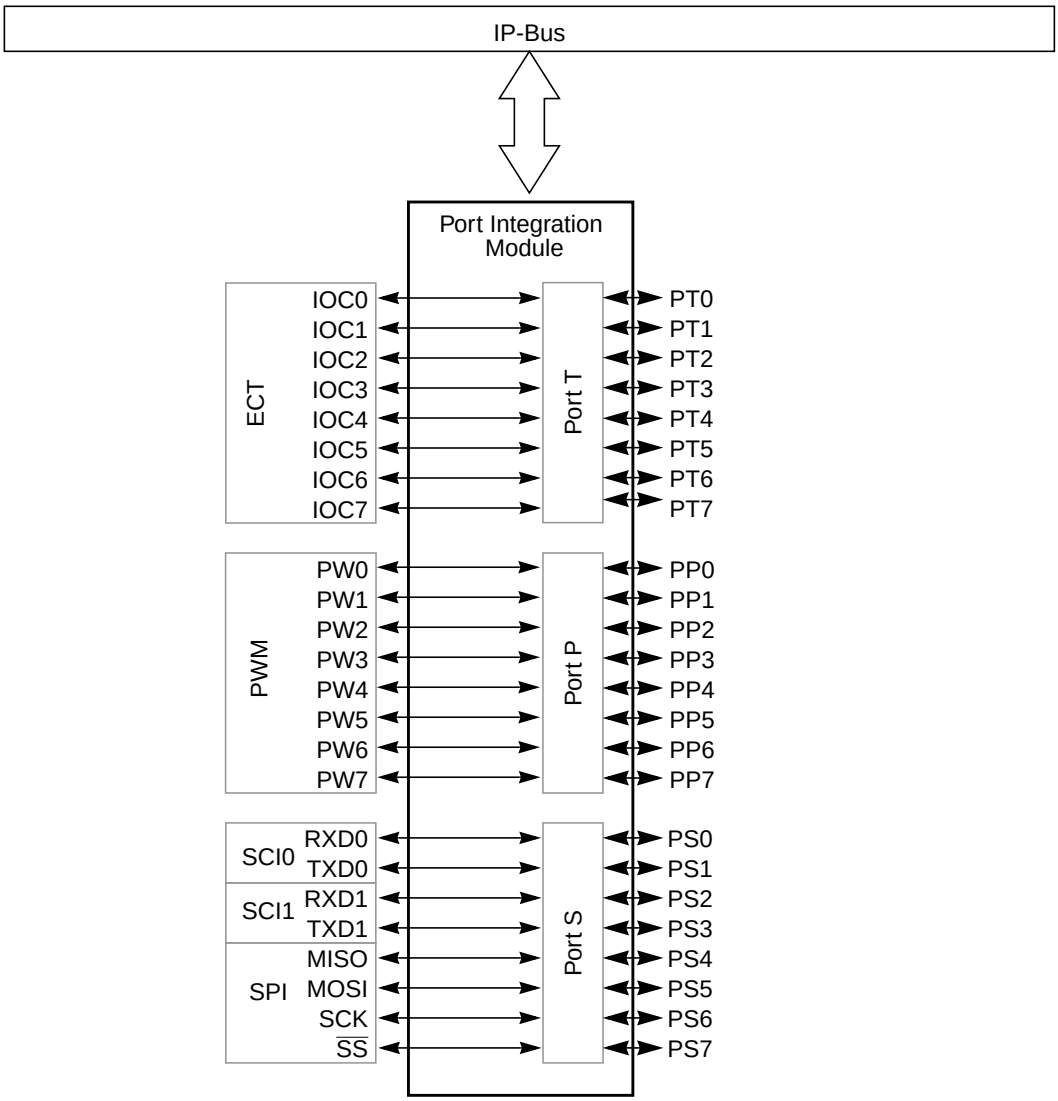

Figure 37 PIM Block Diagram

Register name		Bit 7	6	5	4	3	2	1	Bit 0	Addr. Offset
PPSS	Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0	$00ED
WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0	$00EE
Reserved	Read:	0	0	0	0	0	0	0	0	$00EF
	Write:									
PTP	Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0	$00F0
PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0	$00F1
	Write:									
DDRP	Read: Write:	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0	$00F2
RDRP	Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0	$00F3
PERP	Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0	$00F4
PPSP	Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0	$00F5
Reserved	Read:	0	0	0	0	0	0	0	0	$00F6
	Write:									
Reserved	Read:	0	0	0	0	0	0	0	0	$00F7
	Write:									

= Unimplemented or reserved

Figure 38 PIM9T64 Register Map (Continued)

NOTE: *Register Address = Base Address (INITRG) + Address Offset*

PAMOD — Pulse Accumulator Mode

This bit is active only when the Pulse Accumulator A is enabled (PAEN = 1).

1 = gated time accumulation mode
0 = event counter mode

PEDGE — Pulse Accumulator Edge Control

This bit is active only when the Pulse Accumulator A is enabled (PAEN = 1).

For PAMOD bit = 0 (event counter mode).

1 = rising edges on PT7 pin cause the count to be incremented
0 = falling edges on PT7 pin cause the count to be incremented

For PAMOD bit = 1 (gated time accumulation mode).

1 = PT7 input pin low enables bus clock divided by 64 clock to Pulse Accumulator and the trailing rising edge on PT7 sets the PAIF flag
0 = PT7 input pin high enables bus clock divided by 64 clock to Pulse Accumulator and the trailing falling edge on PT7 sets the PAIF flag.

Table 68 Pin Action

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

If the timer is not active (TEN = 0 in TSCR1), there is no divide-by-64 since the ÷64 clock is generated by the timer prescaler.

CLK1, CLK0 — Clock Select Bits

Table 69 Clock Selection

CLK1	CLK0	Clock Source
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

For the description of PACLK please refer to Figure 72 in page 412.

corresponding 8-bit pulse accumulators to be latched into the associated holding registers. The pulse accumulators will be automatically cleared when the latch action occurs.

Writing zero to this bit has no effect. Read of this bit will return always zero.

FLMC — Force Load Register into the Modulus Counter Count Register

This bit is active only when the modulus down-counter is enabled (MCEN=1).

A write one into this bit loads the load register into the modulus counter count register. This also resets the modulus counter prescaler.

Write zero to this bit has no effect.

When MODMC=0, counter starts counting and stops at $0000.

Read of this bit will return always zero.

MCEN — Modulus Down-Counter Enable

1 = Modulus counter is enabled.
0 = Modulus counter disabled.

When MCEN=0, the counter is preset to $FFFF. This will prevent an early interrupt flag when the modulus down-counter is enabled.

MCPR1, MCPR0 — Modulus Counter Prescaler select

These two bits specify the division rate of the modulus counter prescaler.

The newly selected prescaler division rate will not be effective until a load of the load register into the modulus counter count register occurs.

Table 70 Modulus Counter Prescaler Select

MCPR1	MCPR0	Prescaler division rate
0	0	1
0	1	4
1	0	8
1	1	16

OR — Overrun Flag

OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCIxSR1) with OR set and then reading SCI data register low (SCIxDRL).

1 = Overrun
0 = No overrun

NF — Noise Flag

NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1 (SCIxSR1) and then reading SCI data register low (SCIxDRL).

1 = Noise
0 = No noise

FE — Framing Error Flag

FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag, but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCIxSR1) with FE set and then reading the SCI data register low (SCIxDRL).

1 = Framing error
0 = No framing error

PF — Parity Error Flag

PF is set when the parity enable bit, PE, is set and the parity of the received data does not match its parity bit. Clear PF by reading SCI status register 1 (SCIxSR1), and then reading SCI data register low (SCIxDRL).

1 = Parity error
0 = No parity error

With the misaligned character shown in Figure 88, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 10 bit times x 16 RT cycles = 160 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is:

((154 – 160) / 154) x 100 = 3.90%

For a 9-bit data character, data sampling of the stop bit takes the receiver 10 bit times x 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in Figure 88, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 11 bit times x 16 RT cycles = 176 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is:

((170 – 176) / 170) x 100 = 3.53%

Receiver Wakeup

To enable the SCI to ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCI control register 2 (SCIxCR2) puts the receiver into a standby state during which receiver interrupts are disabled.The SCI will still load the receive data into the SCIxDRH/L registers, but it will not set the RDRF flag.

The transmitting device can address messages to selected receivers by including addressing information in the initial frame or frames of each message.

The WAKE bit in SCI control register 1 (SCIxCR1) determines how the SCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wakeup or address mark wakeup.

Idle input line wakeup (WAKE = 0)

In this wakeup method, an idle condition on the **RX input** signal clears the RWU bit and wakes up the SCI. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is

Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

SPI Control Register 1 (SPICR1)

Address Offset: $00D8

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset:	0	0	0	0	0	1	0	0

Read: anytime
Write: anytime

SPIE — SPI Interrupt Enable Bit

This bit enables SPI interrupts each time the SPIF or MODF status flag is set.

1 = SPI interrupts enabled.
0 = SPI interrupts disabled.

SPE — SPI System Enable Bit

This bit enables the SPI system and dedicates the SPI port pins to SPI system functions.

1 = SPI port pins are dedicated to SPI functions.
0 = SPI disabled. (lower power consumption)

SPTIE — SPI Transmit Interrupt Enable

This bit enables SPI interrupt generated each time the SPTEF flag is set.

1 = SPTEF interrupt enabled.
0 = SPTEF interrupt disabled.

MSTR — SPI Master/Slave Mode Select Bit

External Pin Descriptions

The ATD module has a total of 12 external pins.

AN7 / ETRIG (PAD7) This pin serves as the analog input Channel 7. It can be configured as an external trigger for the ATD conversion, or as general purpose digital input.

AN6 (PAD6) This pin serves as the analog input Channel 6. It can be configured as general purpose digital input.

AN5 (PAD5) This pin serves as the analog input Channel 5. It can be configured as general purpose digital input.

AN4 (PAD4) This pin serves as the analog input Channel 4. It can be configured as general purpose digital input.

AN3 (PAD3) This pin serves as the analog input Channel 3. It can be configured as general purpose digital input.

AN2 (PAD2) This pin serves as the analog input Channel 2. It can be configured as general purpose digital input.

AN1 (PAD1) This pin serves as the analog input Channel 1.It can be configured as general purpose digital input.

AN0 (PAD0) This pin serves as the analog input Channel 0. It can also be configured as general purpose digital input.

VRH, VRL VRH is the high reference voltage and VRL is the low reference voltage for ATD conversion.

ATD Control Register 4 (ATDCTL4)

This register selects the conversion clock frequency, the length of the second phase of the sample time and the resolution of the A/D conversion (i.e.: 8-bits or 10-bits). Writes to this register will abort current conversion sequence but will not start a new sequence.

Address Offset: $0084

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
Reset:	0	0	0	0	0	1	0	1

Unimplemented or Reserved

SRES8 — A/D Resolution Select

1 = 8-bit resolution selected.

0 = 10-bit resolution selected.

This bit selects the resolution of A/D conversion results as either 8 or 10 bits. The A/D converter has an accuracy of 10 bits. However, if low resolution is required, the conversion can be speeded up by selecting 8-bit resolution.

SMP0, SMP1 — Sample Time Select

These two bits select the length of the second phase of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). The sample time consists of two phases. The first phase is two ATD conversion clock cycles long and transfers the sample quickly (via the buffer amplifier) onto the A/D machine's storage node. The second phase attaches the external analog signal directly to the storage node for final charging and high accuracy. Table 89 lists the lengths available for the second sample phase.

Table 89 Sample Time Select

SMP1	SMP0	Length of Second Phase of Sample Time
0	0	2 A/D clock periods
0	1	4 A/D clock periods
1	0	8 A/D clock periods
1	1	16 A/D clock periods

Read: anytime

Write: anytime

SC - Special Channel Conversion Bit

If this bit is set, then special channel conversion can be selected using CC, CB, and CA of ATDCTL5 register. Table 94 lists the coding.
1 = Special channel conversions enabled
0 = Special channel conversions disabled

CAUTION: *Always write remaining bits of ATDTEST1 (Bits 7 to 1) zero when writing the SC bit. Not doing so might result in unpredictable ATD behavior.*

Table 94 Special Channel Select Coding

SC	CC	CB	CA	Analog Input Channel
1	0	X	X	Reserved
1	1	0	0	V_{RH}
1	1	0	1	V_{RL}
1	1	1	0	$(V_{RL}+V_{RH})/2$
1	1	1	1	Reserved

A/D Status Register (ATDSTAT1)

This read-only register contains the Conversion Complete Flags.

Address Offset: $008B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
Write:								
Reset:	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Read: anytime

Write: only in special modes

NOTE: *There is an errata information about the CCF flags. See MC9S12T64 Errata Sheet for details.*

Register Descriptions

There are eight 8-bit registers in the BKP module.

NOTE: *All bits of all registers in this module are completely synchronous to internal clocks during a register read.*

Breakpoint Control Register 0 (BKPCT0)

This register is used to set the breakpoint modes.

Read and write: anytime.

Address Offset $0028

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BKEN	BKFULL	BKBDM	BKTAG	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

BKEN — Breakpoint Enable

This bit enables the module.

1 = Breakpoint module on.
0 = Breakpoint module off.

BKFULL— Full Breakpoint Mode Enable

This bit controls whether the breakpoint module is in Dual Address Mode or Full Breakpoint Mode

1 = Full Breakpoint Mode enabled.
0 = Dual Address Mode enabled.

BKBDM — Breakpoint Background Debug Mode Enable

This bit determines if the breakpoint causes the system to enter Background Debug Mode (BDM) or initiate a Software Interrupt (SWI)

1 = Go to BDM on a compare.
0 = Go to Software Interrupt on a compare.

ATD Characteristics

This section describes the characteristics of the analog to digital converter.

ATD Operating Characteristics

The Table 110 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results: $V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table 110 ATD Operating Characteristics

Conditions are shown in Table 106 unless otherwise noted						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	Differential Reference Voltage(1)	$V_{RH}-V_{RL}$	4.75	5.0	5.25	V
3	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	ATD 10-Bit Conversion Period Clock Cycles(2) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	ATD 8-Bit Conversion Period Clock Cycles(2) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
5	Stop Recovery Time (V_{DDA}=5.0 Volts)	t_{SR}			20	µs
6	Reference Supply current	I_{REF}			0.75	mA

1. Full accuracy is not guaranteed when differential voltage is less than 4.75V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

Factors Influencing Accuracy

Two factors - source resistance and source capacitance - have an influence on the accuracy of the ATD.

Table 112 ATD Conversion Performance

Conditions are shown in Table 106 unless otherwise noted $V_{REF} = V_{RH} - V_{RL}$ = 5.12V. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV f_{ATDCLK} = 2.0MHz						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	10-Bit Resolution	LSB		5		mV
2	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	10-Bit Absolute Error(1)	AE	–3	±2.0	3	Counts
5	8-Bit Resolution	LSB		20		mV
6	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
7	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
8	8-Bit Absolute Error(1)	AE	–1.5	±1.0	1.5	Counts

1. These values include quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also Figure 110.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$