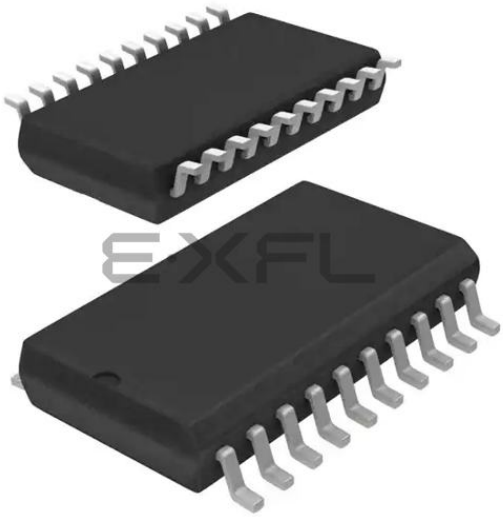

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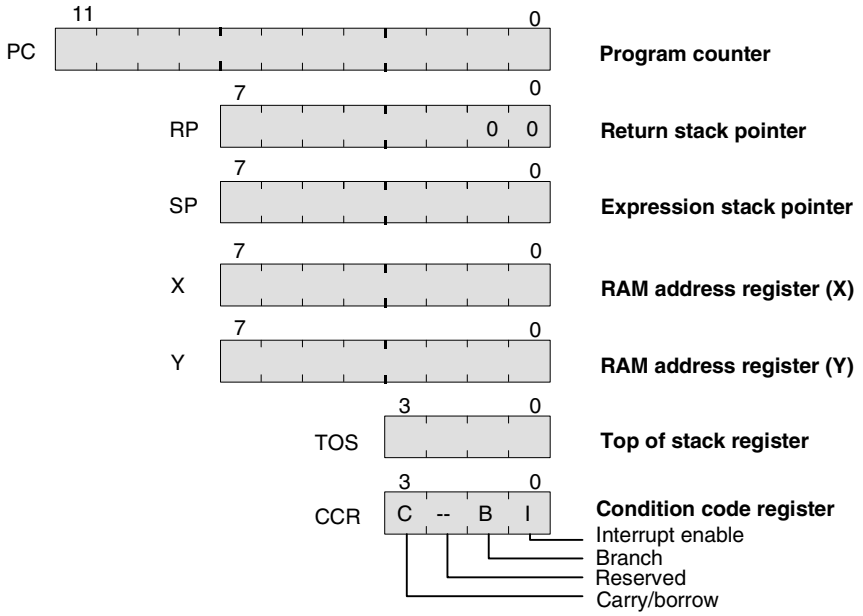
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MARC4
Core Size	4-Bit
Speed	4MHz
Connectivity	SSI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	EEPROM
EEPROM Size	64 x 16
RAM Size	256 x 4
Voltage - Supply (Vcc/Vdd)	1.8V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-SSO
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atam893t-tkq

Figure 4-4. Programming Model



4.2.3.2 RAM Address Registers

The RAM is addressed with the four 8-bit wide RAM address registers: SP, RP, X and Y. These registers allow access to any of the 256 RAM nibbles.

4.2.3.3 Expression Stack Pointer (SP)

The stack pointer contains the address of the next-to-top 4-bit item (TOS-1) of the expression stack. The pointer is automatically pre-incremented if a nibble is moved onto the stack or post-decremented if a nibble is removed from the stack. Every post-decrement operation moves the item (TOS-1) to the TOS register before the SP is decremented. After a reset the stack pointer has to be initialized with “>SP S0” to allocate the start address of the expression stack area.

4.2.3.4 Return Stack Pointer (RP)

The return stack pointer points to the top element of the 12-bit wide return stack. The pointer automatically pre-increments if an element is moved onto the stack, or it post-decrements if an element is removed from the stack. The return stack pointer increments and decrements in steps of 4. This means that every time a 12-bit element is stacked, a 4-bit RAM location is left unwritten. This location is used by the qFORTH compiler to allocate 4-bit variables. After a reset the return stack pointer has to be initialized via “>RP FCh”.

4.2.3.5 RAM Address Registers (X and Y)

The X and Y registers are used to address any 4-bit item in the RAM. A fetch operation moves the addressed nibble onto the TOS. A store operation moves the TOS to the addressed RAM location. By using either the pre-increment or post-decrement addressing mode, arrays in the RAM can be compared, filled or moved.

4.2.5 I/O Bus

The I/O ports and the registers of the peripheral modules are I/O mapped. All communication between the core and the on-chip peripherals takes place via the I/O bus and the associated I/O control. With the MARC4 IN and OUT instructions the I/O bus allows a direct read or write access to one of the 16 primary I/O addresses. More about the I/O access to the on-chip peripherals is described in the section “Peripheral Modules”. The I/O bus is internal and is not accessible by the customer on the final microcontroller device, but it is used as the interface for the MARC4 emulation (see section “Emulation”).

4.2.6 Instruction Set

The MARC4 instruction set is optimized for the high level programming language qFORTH. Many MARC4 instructions are qFORTH words. This enables the compiler to generate a fast and compact program code. The CPU has an instruction pipeline allowing the controller to prefetch an instruction from program memory at the same time as the present instruction is being executed. The MARC4 is a zero address machine, the instructions containing only the operation to be performed and no source or destination address fields. The operations are implicitly performed on the data placed on the stack. There are one and two byte instructions which are executed within 1 to 4 machine cycles. A MARC4 machine cycle is made up of two system clock cycles (SYSCL). Most of the instructions are only one byte long and are executed in a single machine cycle. For more information refer to the “MARC4 Programmer's Guide”.

4.2.7 Interrupt Structure

The MARC4 can handle interrupts with eight different priority levels. They can be generated from the internal and external interrupt sources or by a software interrupt from the CPU itself. Each interrupt level has a hard-wired priority and an associated vector for the service routine in the program memory (see Table 4-2 on page 11). The programmer can postpone the processing of interrupts by resetting the interrupt enable flag (I) in the CCR. An interrupt occurrence will still be registered, but the interrupt routine only started after the I flag is set. All interrupts can be masked, and the priority individually software configured by programming the appropriate control register of the interrupting module (see section “Peripheral Modules”).

4.2.7.1 Interrupt Processing

For processing the eight interrupt levels, the MARC4 includes an interrupt controller with two 8-bit wide “interrupt pending” and “interrupt active” registers. The interrupt controller samples all interrupt requests during every non-I/O instruction cycle and latches these in the interrupt pending register. If no higher priority interrupt is present in the interrupt active register, it signals the CPU to interrupt the current program execution. If the interrupt enable bit is set, the processor enters an interrupt acknowledge cycle. During this cycle a short call (SCALL) instruction to the service routine is executed and the current PC is saved on the return stack.

An interrupt service routine is completed with the RTI instruction. This instruction resets the corresponding bits in the interrupt pending/active register and fetches the return address from the return stack to the program counter. When the interrupt enable flag is reset (triggering of interrupt routines are disabled), the execution of new interrupt service routines is inhibited but not the logging of the interrupt requests in the interrupt pending register. The execution of the interrupt is delayed until the interrupt enable flag is set again. Note that interrupts are only lost if an interrupt request occurs while the corresponding bit in the pending register is still set (i.e., the interrupt service routine is not yet finished).

Table 4-2. Hardware Interrupts

Interrupt	Interrupt Mask		Interrupt Source
	Register	Bit	
INT1	P5CR	P52M1, P52M2 P53M1, P53M2	Any edge at BP52 Any edge at BP53
INT2	T1M	T1IM	Timer 1
INT3	SISC	SIM	SSI buffer full/empty or BP40/BP43 interrupt
INT4	T2CM	T2IM	Timer 2 compare match/overflow
INT5	T3CM1 T3CM2 T3C	T3IM1 T3IM2 T3EIM	Timer 3 compare register 1 match Timer 3 compare register 2 match Timer 3 edge event occurs (T3I)
INT6	P5CR	P50M1, P50M2 P51M1, P51M2	Any edge at BP50 Any edge at BP51
INT7	VCM	VIM	External/internal voltage monitoring

4.2.7.3 Software Interrupts

The programmer can generate interrupts by using the Software Interrupt Instruction (SWI) which is supported in qFORTH by predefined macros named SWI0...SWI7. The software triggered interrupt operates exactly like any hardware triggered interrupt. The SWI instruction takes the top two elements from the expression stack and writes the corresponding bits via the I/O bus to the interrupt pending register. Therefore, by using the SWI instruction, interrupts can be re-prioritized or lower priority processes scheduled for later execution.

4.2.7.4 Hardware Interrupts

In the ATAM893-D, there are eleven hardware interrupt sources with seven different levels. Each source can be masked individually by mask bits in the corresponding control registers. An overview of the possible hardware configurations is shown in Table 4-2.

4.3 Master Reset

The master reset forces the CPU into a well-defined condition. It is unmaskable and is activated independent of the current program state. It can be triggered by either initial supply power-up, a short collapse of the power supply, brown-out detection circuitry, watchdog time-out, or an external input clock supervisor stage (see Figure 4-7 on page 12).

A master reset activation will reset the interrupt enable flag, the interrupt pending register and the interrupt active register. During the power-on reset phase the I/O bus control signals are set to reset mode thereby initializing all on-chip peripherals. All bi-directional ports are set to input mode.

Attention: During any reset phase, the BP20/NTE input is driven towards V_{DD} by a strong pull-up transistor. This pin must not be pulled down to V_{SS} during reset by any external circuitry representing a resistor of less than 150 kΩ

Releasing the reset results in a short call instruction (opcode C1h) to the EEPROM address 008h. This activates the initialization routine $RESET which in turn has to initialize all necessary RAM variables, stack pointers and peripheral configuration registers (see Table 5-1 on page 23).

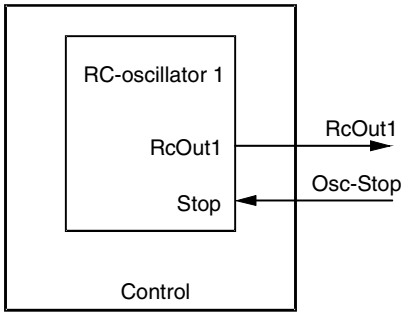
4.5.2 Oscillator Circuits and External Clock Input Stage

The ATAM893-D series consists of four different internal oscillators: two RC-oscillators, one 4-MHz crystal oscillator, one 32-kHz crystal oscillator and one external clock input stage.

4.5.2.1 RC-oscillator 1 Fully Integrated

For timing insensitive applications, it is possible to use the fully integrated RC-oscillator 1. It operates without any external components and saves additional costs. The RC-oscillator 1 center frequency tolerance is better than ±50% over the full temperature and voltage range. The basic center frequency of the RC-oscillator 1 is $f_O \approx$ 4.0 MHz. The RC oscillator 1 is selected by default after power-on reset.

Figure 4-13. RC-oscillator 1



4.5.2.2 External Input Clock

The OSC1 or OSC2 can be driven by an external clock source provided it meets the specified duty cycle, rise and fall times and input levels. Additionally, the external clock stage contains a supervisory circuit for the input clock. The supervisor function is controlled via the OS1, OS0 bit in the SC register and the CCS bit in the CM register. If the external input clock is missing for more than 1 ms and CCS = 0 is set in the CM register, the supervisory circuit generates a hardware reset.

Figure 4-14. External Input Clock

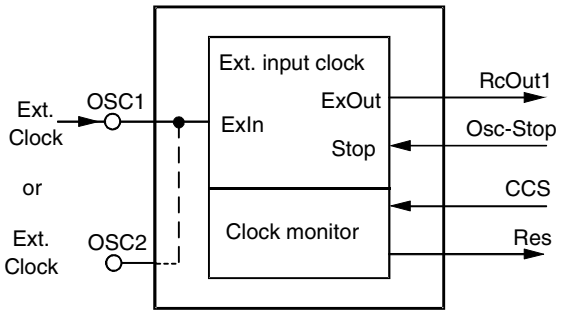


Table 4-7. Oscillator Select

Mode	OS1	OS0	Input for SUBCL	Selected Oscillators
1	1	1	C_{in}/16	RC-oscillator 1 and external input clock
2	0	1	C_{in}/16	RC-oscillator 1 and RC-oscillator 2
3	1	0	C_{in}/16	RC-oscillator 1 and 4-MHz crystal oscillator
4	0	0	32 kHz	RC-oscillator 1 and 32-kHz crystal oscillator

Note: If the bit CCS = 0 in the CM-register the RC-oscillator 1 always stops

4.6 Power-down Modes

The sleep mode is a shut-down condition which is used to reduce the average system power consumption in applications where the microcontroller is not fully utilized. In this mode, the system clock is stopped. The sleep mode is entered via the SLEEP instruction. This instruction sets the interrupt enable bit (I) in the condition code register to enable all interrupts and stops the core. During the sleep mode the peripheral modules remain active and are able to generate interrupts. The microcontroller exits the sleep mode by carrying out any interrupt or a reset.

The sleep mode can only be kept when none of the interrupt pending or active register bits are set. The application of the $AUTOSLEEP routine ensures the correct function of the sleep mode. For standard applications use the $AUTOSLEEP routine to enter the power-down mode. Using the SLEEP instruction instead of the $AUTOSLEEP following an I/O instruction requires the insertion of 3 non I/O instruction cycles (for example NOP NOP NOP) between the IN or OUT command and the SLEEP command.

The total power consumption is directly proportional to the active time of the microcontroller. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{total}(V_{DD},f_{syscl}) = I_{Sleep} + \left(I_{DD} \times \frac{t_{active}}{t_{total}}\right) I_{DD} \text{ depends on } V_{DD} \text{ and } f_{syscl}$$

The ATAM893-D has various power-down modes. During the sleep mode the clock for the MARC4 core is stopped. With the NSTOP bit in the clock management register (CM) it is programmable if the clock for the on-chip peripherals is active or stopped during the sleep mode. If the clock for the core and the peripherals is stopped the selected oscillator is switched off. An exception is the 32-kHz oscillator, if it is selected it runs continuously independent of the NSTOP bit. If the oscillator is stopped or the 32-kHz oscillator is selected, power consumption is extremely low.

Table 4-8. Power-down Modes

Mode	CPU Core	Osc-Stop[1]	Brown-out Function	RC-Oscillator 1 RC-Oscillator 2 4-MHz Oscillator	32-kHz Oscillator	External Input Clock
Active	RUN	NO	Active	RUN	RUN	YES
Power-down	SLEEP	NO	Active	RUN	RUN	YES
SLEEP	SLEEP	YES	STOP	STOP	RUN	STOP

Note: Osc-Stop = SLEEP and NSTOP and WDL

5.2 Bi-directional Ports

With the exception of Port 1 and Port 6, all other ports (2, 4 and 5) are 4 bits wide. Port 1 and Port 6 have a data width of 2 bits (bit 0 and bit 3). All ports may be used for data input or output. All ports are equipped with Schmitt trigger inputs and a variety of mask options for open drain, open source, full complementary outputs, pull-up and pull-down transistors. All Port Data Registers (PxDAT) are I/O mapped to the primary address register of the respective port address and the Port Control Register (PxCR), to the corresponding auxiliary register.

There are five different directional ports available:

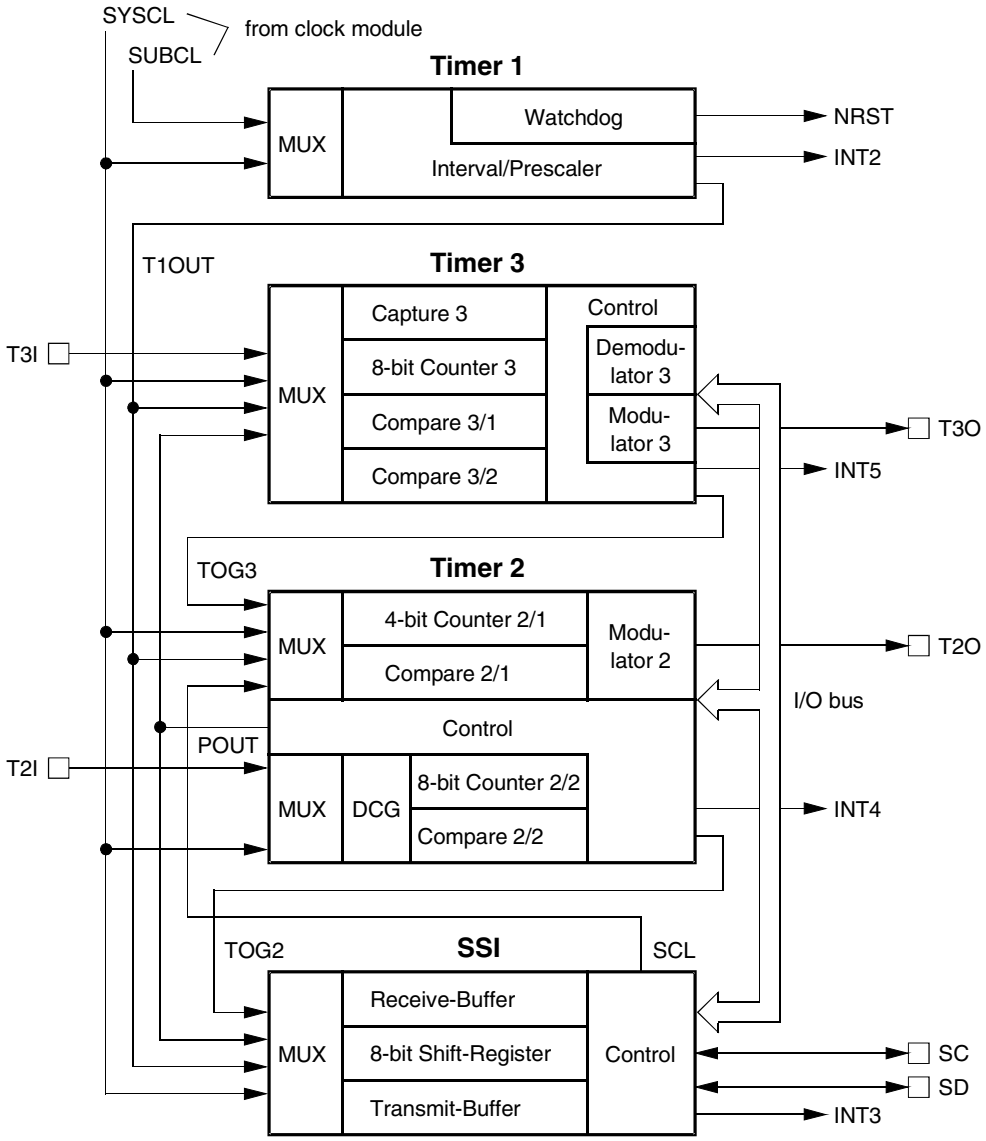
Port 1	2-bit wide bi-directional ports with automatic full bus width direction switching
Port 2	4-bit wide bit-wise-programmable I/O port
Port 5	4-bit wide bit-wise-programmable bi-directional port with optional strong pull-ups and programmable interrupt logic
Port 4	4-bit wide bit-wise-programmable bi-directional port also provides the I/O interface to Timer 2, SSI, voltage monitor input and external interrupt input
Port 6	2-bit wide bit-wise-programmable bi-directional port also provides the I/O interface to Timer 3 and external interrupt input

5.2.1 Bi-directional Port 1

In Port 1 the data direction register is not independently software programmable, the direction of the complete port being switched automatically when an I/O instruction occurs (see Figure 5-2 on page 25). The port is switched to output mode via an OUT instruction and to input via an IN instruction. The data written to a port will be stored into the output data latches and appears immediately at the port pin following the OUT instruction. After RESET all output latches are set to '1' and the port is switched to input mode. An IN instruction reads the condition of the associated pins.

Note: Care must be taken when switching the bi-directional port from output to input. The capacitive pin loading at this port in conjunction with the high resistance pull-ups may cause the CPU to read the contents of the output data register rather than the external input state. To avoid this, one of the following programming techniques should be used:
Use two IN-instructions and DROP the first data nibble. The first IN switches the port from output to input and the DROP removes the first invalid nibble. The second IN reads the valid pin state.
Use an OUT-instruction followed by an IN-instruction. Via the OUT-instruction, the capacitive load is charged or discharged depending on the optional pull-up/pull-down configuration. Write a '1' for pins with pull-up resistors and a '0' for pins with pull-down resistors.

Figure 5-7. UTCM Block Diagram



5.3.1 Timer 1

The Timer 1 is an interval timer which can be used to generate periodic interrupts and as prescaler for Timer 2, Timer 3, the serial interface and the watchdog function.

The Timer 1 consists of a programmable 14-stage divider that is driven by either SUBCL or SYSCL. The timer output signal can be used as prescaler clock or as SUBCL and as source for the Timer 1 interrupt. Because of other system requirements the Timer 1 output T1OUT is synchronized with SYSCL. Therefore, in the power-down mode SLEEP (CPU core →sleep and OSC-Stop →yes) the output T1OUT is stopped (T1OUT = 0). Nevertheless, the Timer 1 can be active in SLEEP and generate Timer 1 interrupts. The interrupt is maskable via the T1IM bit and the SUBCL can be bypassed via the T1BP bit of the T1C2 register. The time interval for the timer output can be programmed via the Timer 1 control register T1C1.

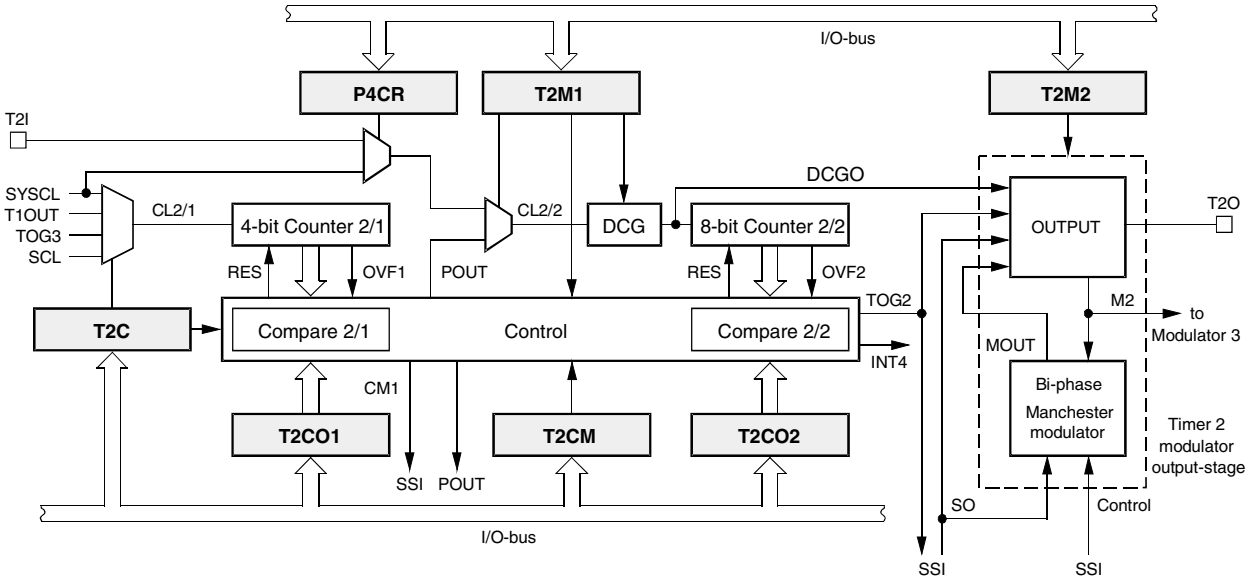
The Timer 2 has a 4-bit compare register (T2CO1) and an 8-bit compare register (T2CO2). Both these compare registers are cascadable as a 12-bit compare register, or 8-bit compare register and 4-bit compare register.

For 12-bit compare data value: $m = x + 1$ $0 \leq x \leq 4095$

For 8-bit compare data value: $n = y + 1$ $0 \leq y \leq 255$

For 4-bit compare data value: $l = z + 1$ $0 \leq z \leq 15$

Figure 5-10. Timer 2

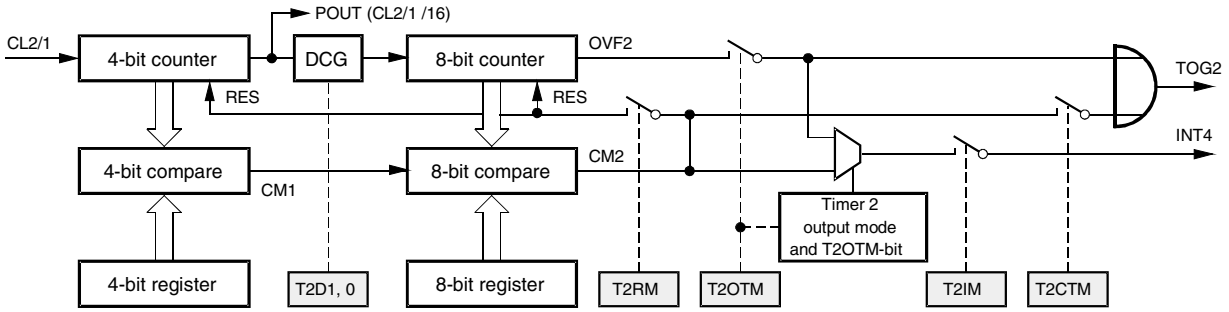


5.3.2.1 Timer 2 Modes

Mode 1: 12-bit Compare Counter

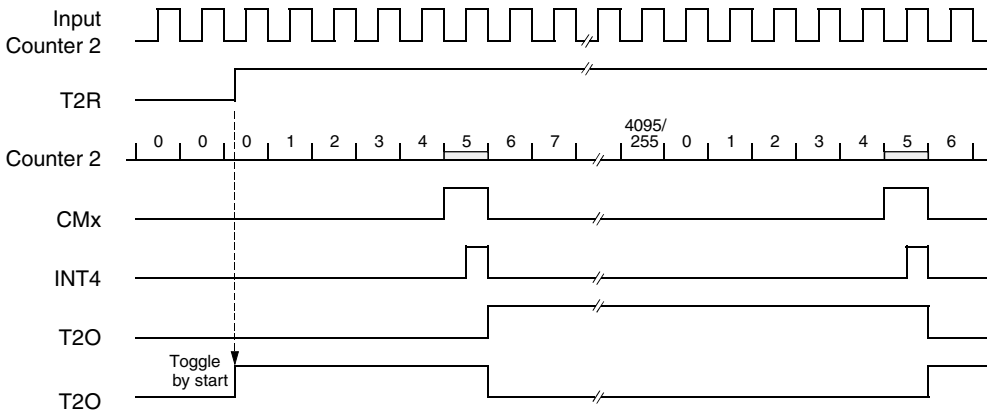
The 4-bit stage and the 8-bit stage work together as a 12-bit compare counter. A compare match signal of the 4-bit and the 8-bit stage generates the signal for the counter reset, toggle flip-flop or interrupt. The compare action is programmable via the compare mode register (T2CM). The 4-bit counter overflow (OVF1) supplies the clock output (POUT) with clocks. The duty cycle generator (DCG) has to be bypassed in this mode.

Figure 5-11. 12-bit Compare Counter



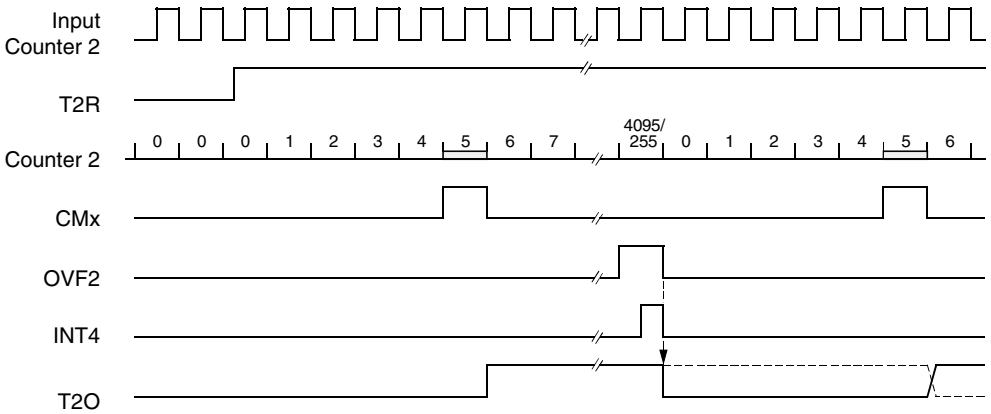
Toggle Mode B: A Timer 2 compare match toggles the output flip-flop (M2) →T2O

Figure 5-16. Pulse Generator – the Timer Output Toggles with the Timer Start if the T2TS-bit Is Set



Toggle Mode C: A Timer 2 compare match toggles the output flip-flop (M2) →T2O

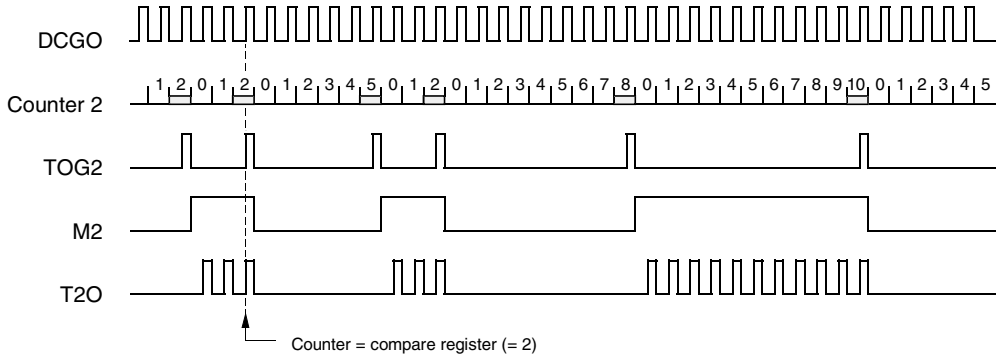
Figure 5-17. Pulse Generator – the Timer Toggles with Timer Overflow and Compare Match



Timer 2 Output Mode 2

Duty Cycle Burst Generator 1: The DCG output signal (DCGO) is given to the output, and gated by the output flip-flop (M2)

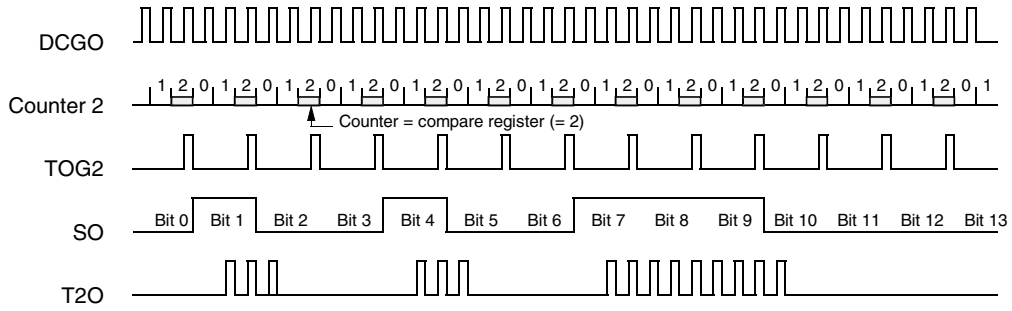
Figure 5-18. Carrier Frequency Burst Modulation with Timer 2 Toggle Flip-flop Output



Timer 2 Output Mode 3

Duty Cycle Burst Generator 2: The DCG output signal (DCGO) is given to the output, and gated by the SSI internal data output (SO)

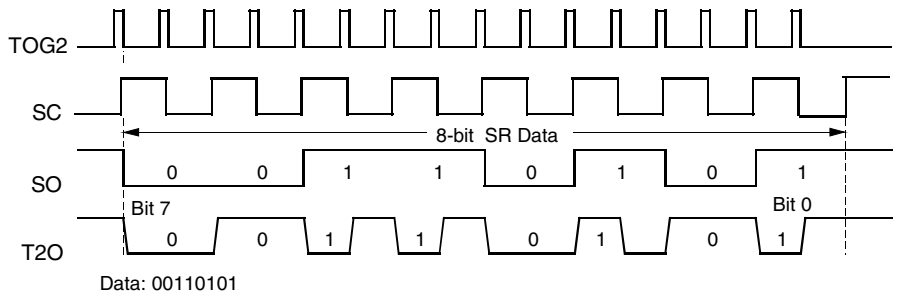
Figure 5-19. Carrier Frequency Burst Modulation with the SSI Data Output



Timer 2 Output Mode 4

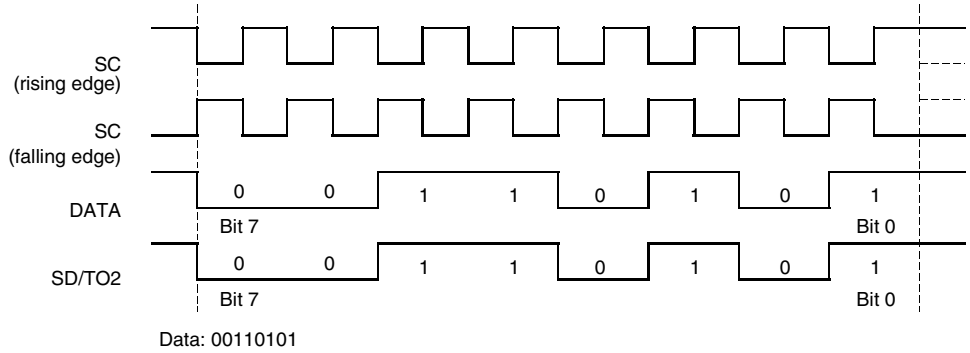
Bi-phase Modulator: Timer 2 Modulates the SSI Internal Data Output (SO) to Bi-phase Code.

Figure 5-20. Bi-phase Modulation



5.3.4.4 8-bit Synchronous Mode

Figure 5-39. 8-bit Synchronous Mode



In the 8-bit synchronous mode, the SSI can operate as either a 2- or 3-wire interface (see section “SSI Peripheral Configuration”). The serial data (SD) is received or transmitted in NRZ format, synchronized to either the rising or falling edge of the shift clock (SC). The choice of clock edge is defined by the Serial Mode Control bits (SM0,SM1). It should be noted that the transmission edge refers to the SC clock edge with which the SD changes. To avoid clock skew problems, the incoming serial input data is shifted in with the opposite edge.

When used together with one of the timer modulator or demodulator stages, the SSI must be set in the 8-bit synchronous mode 1.

In RX mode, as soon as the SSI is activated (SIR = 0), 8 shift clocks are generated and the incoming serial data is shifted into the shift register. This first telegram is automatically transferred into the receive buffer and the SRDY set to 0 indicating that the receive buffer contains valid data. At the same time an interrupt (if enabled) is generated. The SSI then continues shifting in the following 8-bit telegram. If, during this time the first telegram has been read by the controller, the second telegram will also be transferred in the same way into the receive buffer and the SSI will continue clocking in the next telegram. Should, however, the first telegram not have been read (SRDY = 1), then the SSI will stop, temporarily holding the second telegram in the shift register until a certain point of time when the controller is able to service the receive buffer. In this way no data is lost or overwritten.

Deactivating the SSI (SIR = 1) in mid-telegram will immediately stop the shift clock and latch the present contents of the shift register into the receive buffer. This can be used for clocking in a data telegram of less than 8 bits in length. Care should be taken to read out the final complete 8-bit data telegram of a multiple word message before deactivating the SSI (SIR = 1) and terminating the reception. After termination, the shift register contents will overwrite the receive buffer.

5.3.4.5 9-bit Shift Mode

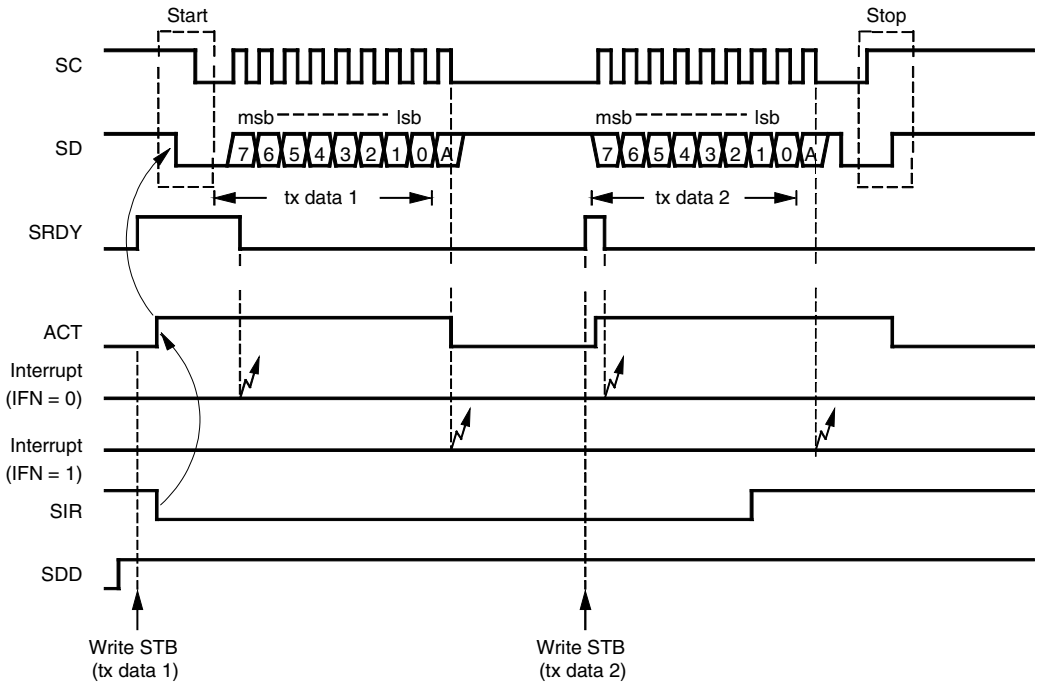
In the 9-bit shift mode, the SSI is able to handle the MCL protocol (described below). It always operates as an MCL master device, i.e., SC is always generated and output by the SSI. Both the MCL start and stop conditions are automatically generated whenever the SSI is activated or deactivated by the SIR bit. In accordance with the MCL protocol, the output data is always changed in the clock low phase and shifted in on the high phase.

Before activating the SSI (SIR = 0) and commencing an MCL dialog, the appropriate data direction for the first word must be set using the SDD control bit. The state of this bit controls the direction of the data port (BP43 or MCL_SD). Once started, the 8 data bits are, depending on the selected direction, either clocked into or out of the shift register. During the 9th clock period, the port direction is automatically switched over so that the corresponding acknowledge bit can be shifted out or read in. In transmit mode, the acknowledge bit received from the slave device is captured in the SSI Status Register (TACK) where it can be read by the controller. In receive mode, the state of the acknowledge bit to be returned to the slave device is predetermined by the SSI Status Register (RACK).

Changing the directional mode (TX/RX) should not be performed during the transfer of an MCL telegram. One should wait until the end of the telegram which can be detected using the SSI interrupt (IFN = 1) or by interrogating the ACT status.

Once started, a 9-bit telegram will always run to completion and will not be prematurely terminated by the SIR bit. So, if the SIR bit is set to ‘1’ in telegram, the SSI will complete the current transfer and terminate the dialog with an MCL stop condition.

Figure 5-42. Example of MCL Transmit Dialog



5.3.4.9 Modulation and Demodulation

If the shift register is used together with Timer 2 or Timer 3 for modulation or demodulation purposes, the 8-bit synchronous mode must be used. In this case, the unused Port 4 pins can be used as conventional bi-directional ports.

The modulation and demodulation stages, if enabled, operate as soon as the SSI is activated (SIR = 0) and cease when deactivated (SIR = 1).

Due to the byte-orientated data control, the SSI (when running normally) generates serial bit streams which are submultiples of 8 bits. An SSI output masking (OMSK) function permits, however, the generation of bit streams of any length. The OMSK signal is derived indirectly from the 4-bit prescaler of the Timer 2 and masks out a programmable number of unrequited trailing data bits during the shifting out of the final data word in the bit stream. The number of non-masked data bits is defined by the value pre-programmed in the prescaler compare register. To use output masking, the modulator stop mode bit (MSM) must be set to'0' before programming the final data word into the SSI transmit buffer. This in turn, enables shift clocks to the prescaler when this final word is shifted out. On reaching the compare value, the prescaler triggers the OMSK signal and all following data bits are blanked.

5.3.4.10 Internal 2-wire Multi-chip Link

Two additional on-chip pads (MCL_SC and MCL_SD) for the SC and the SD line can be used as chip-to-chip link for multi-chip applications. These pads can be activated by setting the MCL bit in the SISC register. They are also used as interface to the internal data EEPROM

Figure 5-46. Multi-chip Link

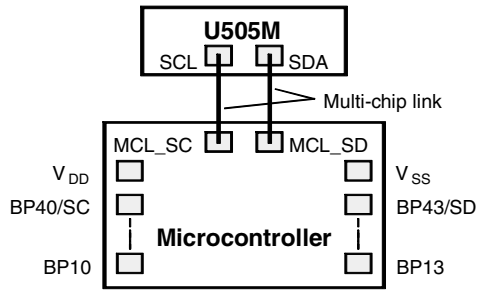
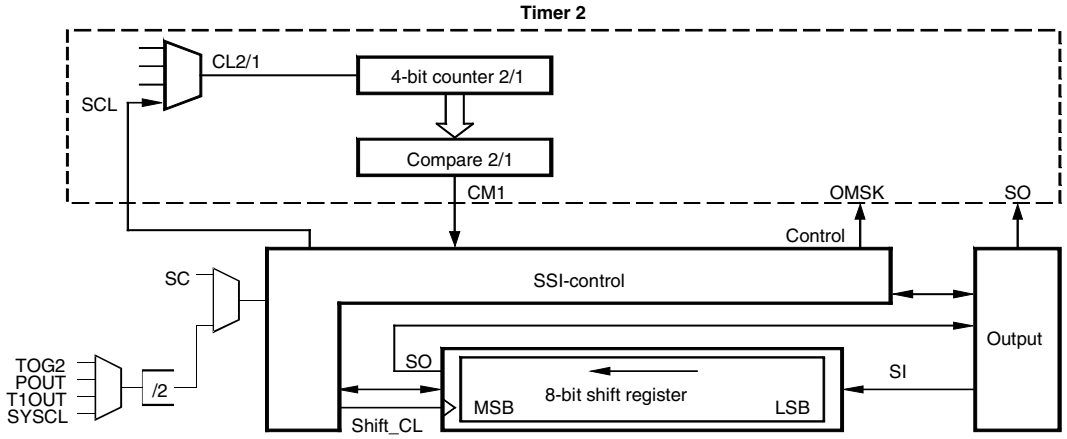


Figure 5-47. SSI Output Masking Function



5.3.4.13 Serial Interface Control Register 2 (SIC2)

Auxiliary register address: 'A'hex

	Bit 3	Bit 2	Bit 1	Bit 0	
SIC2	**MSM**	**SM1**	**SM0**	**SDD**	**Reset value: 1111b**

MSM	**M**odular **S**top **M**ode MSM = 1, modulator stop mode disabled (output masking off) MSM = 0, modulator stop mode enabled (output masking on) - used in modulation modes for generating bit streams which are not sub multiples of 8 bit.
SM1	**S**erial **M**ode control bit **1**
SM0	**S**erial **M**ode control bit **0**

Table 5-17. Serial Mode Control Bits

Mode	SM1	SM0	SSI Mode
1	1	1	8-bit NRZ-data changes with the rising edge of SC
2	1	0	8-bit NRZ-data changes with the falling edge of SC
3	0	1	9-bit two-wire MCL mode
4	0	0	8-bit two-wire pseudo MCL mode (no acknowledge)

SDD	**S**erial **D**ata **D**irection SDD = 1, transmit mode – SD line used as output (transmit data). SRDY is set by a transmit buffer write access SDD = 0, receive mode – SD line used as input (receive data). SRDY is set by a receive buffer read access

Note: SDD controls port directional control and defines the reset function for the SRDY-flag

Combination Mode 9: Bi-phase Demodulation

SSI mode 1: 8-bit shift register internal data input (SI) and the internal shift clock (SCI) from the Timer 3

Timer 3 mode 11: Bi-phase demodulation with Timer 3

In the Bi-phase demodulation mode the timer works like in the Manchester demodulation mode. The difference is that the bits are decoded with the toggle flip-flop. This flip-flop samples the edge in the middle of the bit-frame and the compare register 1 match event shifts the toggle flip-flop output into shift register. Before activating the demodulation the timer and the demodulation stage must be synchronized with the bit-stream. The Bi-phase code timing consists of parts with the half bit-length and the complete bit-length. The synchronization routine must start the demodulator after an interval with the complete bit-length.

The counter can be driven by any internal clock source and the output T3O can be used by Timer 2 in this mode.

Figure 5-58. Bi-phase Demodulation

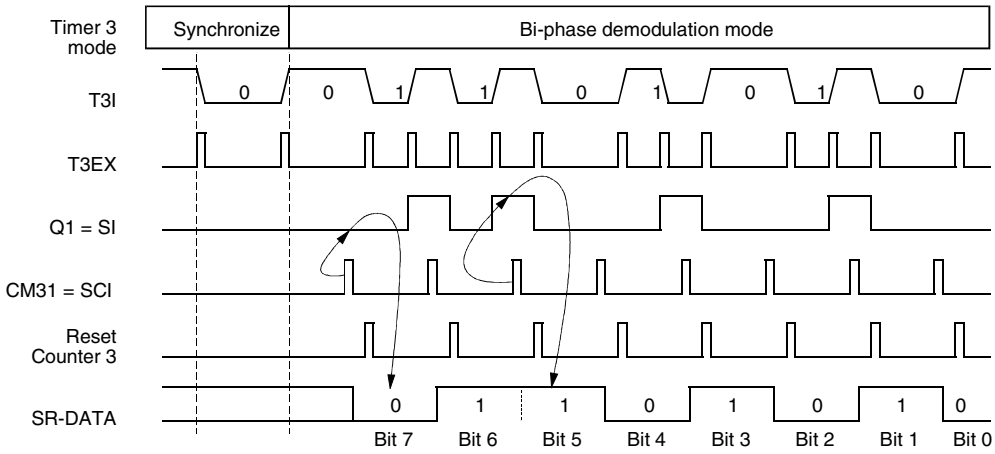


Figure 5-60. Frequency Measurement

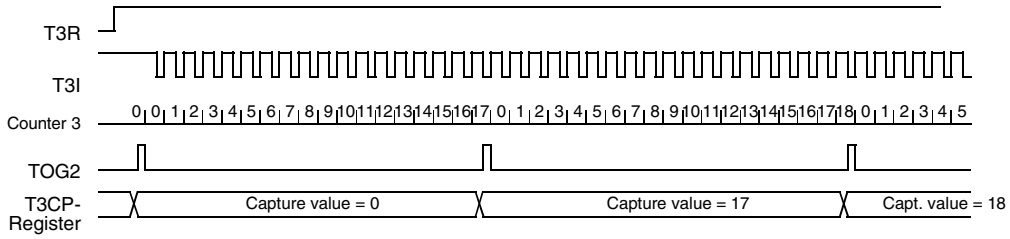
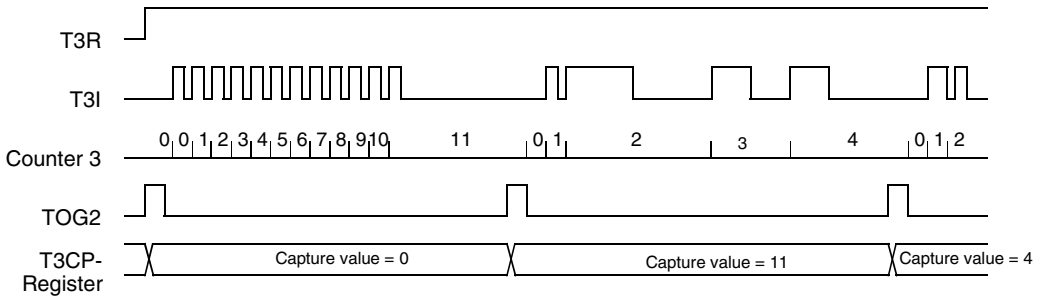


Figure 5-61. Event Counter with Time Gate

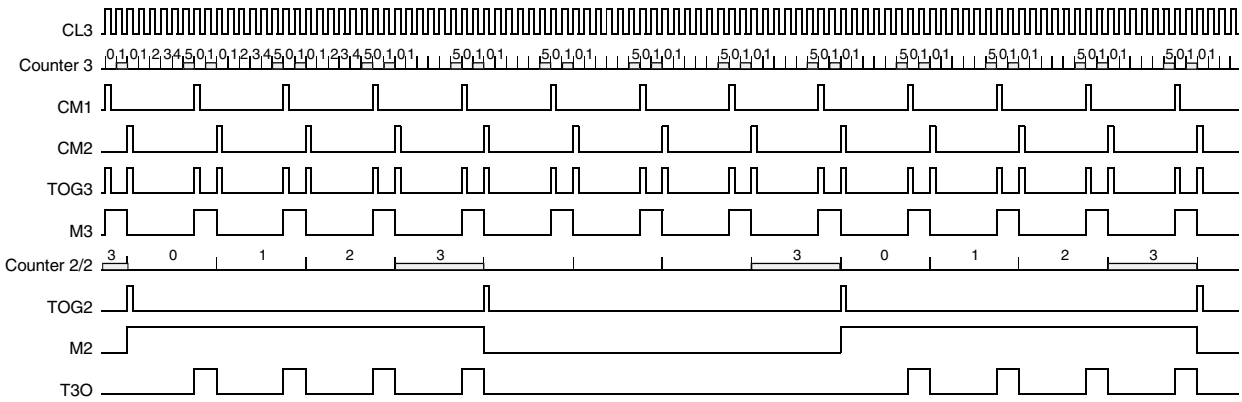


Combination Mode 11: Burst Modulation 1

Timer 2 mode 1/2:	12-bit compare counter/8-bit compare counter and 4-bit prescaler
Timer 2 output mode 1/6:	Timer 2 compare match toggles the output flip-flop (M2) to the Timer 3
Timer 3 mode 6:	Carrier frequency burst modulation controlled by Timer 2 output (M2)

The Timer 3 counter is driven by an internal or external clock source. Its compare- and compare mode registers must be programmed to generate the carrier frequency with the output toggle flip-flop. The output toggle flip-flop (M2) of Timer 2 is used to enable and disable the Timer 3 output. The Timer 2 can be driven by the toggle output signal of Timer 3 (TOG3) or any other clock source.

Figure 5-62. Burst Modulation 1

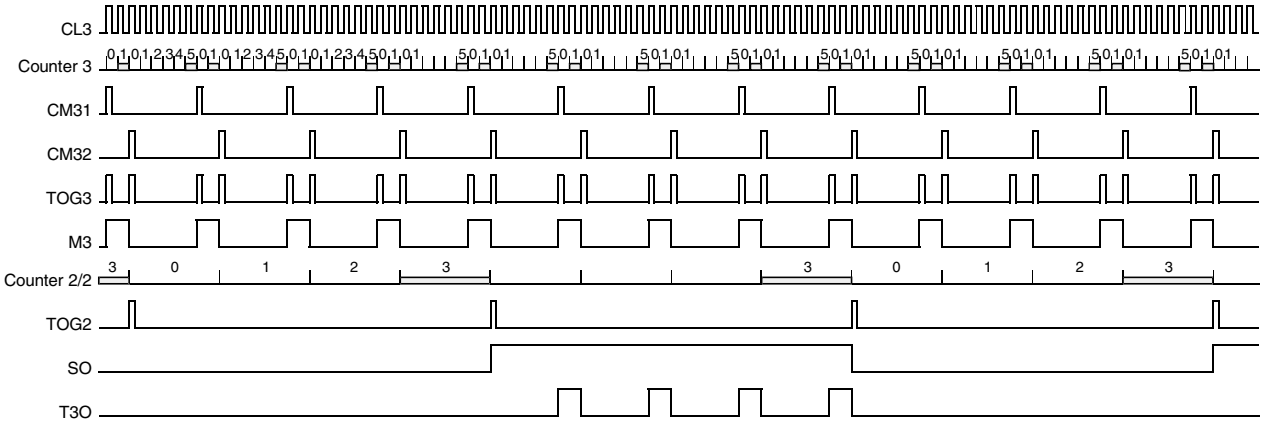


Combination Mode 12: Burst Modulation 2

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 3
Timer 2 output mode 2: Timer 2 output mode 1/6:	8-bit compare counter and 4-bit prescaler Timer 2 compare match toggles (TOG2) to the SSI
Timer 3 mode 7:	Carrier frequency burst modulation controlled by the internal output (SO) of SSI

The Timer 3 counter is driven by an internal or external clock source. Its compare- and compare mode registers must be programmed to generate the carrier frequency with the output toggle flip-flop (M3). The internal data output (SO) of the SSI is used to enable and disable the Timer 3 output. The SSI can be supplied with the toggle signal of Timer 2.

Figure 5-64. Burst Modulation 2



Combination Mode 13: FSK Modulation

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 3
Timer 2 output mode 3: Timer 2 output mode 1/6:	8-bit compare counter and 4-bit prescaler Timer 2 4-bit compare match signal (POUT) to the SSI
Timer 3 mode 8:	FSK modulation with shift register data output (SO)

The two compare registers are used to generate two different time intervals. The SSI data output selects which compare register is used for the output frequency generation. A '0' level at the SSI data output enables the compare register 1 and a '1' level enables the compare register 2. The compare- and compare mode registers must be programmed to generate the two frequencies via the output toggle flip-flop. The SSI can be supplied with the toggle signal of Timer 2 or any other clock source. The Timer 3 counter is driven by an internal or external clock source.

10. AC Characteristics

Supply voltage V_{DD} = 1.8 to 6.5 V, V_{SS} = 0 V, T_{amb} = 25°C unless otherwise specified.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Operation Cycle Time						
System clock cycle	V_{DD} = 1.8 to 6.5 V T_{amb} = -40 to 125° C	t_{SYSCL}	500		2000	ns
	V_{DD} = 2.4 to 6.5 V T_{amb} = -40 to 125° C	t_{SYSCL}	250		2000	ns
Timer 2 input Timing Pin T2I						
Timer 2 input clock		f_{T2I}			5	MHz
Timer 2 input LOW time	Rise/fall time < 10 ns	t_{T2IL}	100			ns
Timer 2 input HIGH time	Rise/fall time < 10 ns	t_{T2IH}	100			ns
Timer 3 Input Timing Pin T3I						
Timer 3 input clock		f_{T3I}			SYSCL/2	MHz
Timer 3 input LOW time	Rise/fall time < 10 ns	t_{T3IL}	2 t_{SYSCL}			ns
Timer 3 input HIGH time	Rise/fall time < 10 ns	t_{T3IH}	2 t_{SYSCL}			ns
Interrupt Request Input Timing						
Interrupt request LOW time	Rise/fall time < 10 ns	t_{IRL}	100			ns
Interrupt request HIGH time	Rise/fall time < 10 ns	t_{IRH}	100			ns
External System Clock						
EXSCL at OSC1, ECM = EN	Rise/fall time < 10 ns	f_{EXSCL}	0.5		4	MHz
EXSCL at OSC1, ECM = DI	Rise/fall time < 10 ns	f_{EXSCL}	0.02		4	MHz
Input HIGH time	Rise/fall time < 10 ns	t_{IH}	0.1			µs
Reset Timing						
Power-on reset time	$V_{DD} > V_{POR}$	t_{POR}		1.5	5	ms
RC Oscillator 1						
Frequency		f_{RcOut1}		3.8		MHz
Stability	V_{DD} = 2.0 to 6.5 V T_{amb} = -40 to 125° C	Δf/f			±50	%
RC Oscillator 2 - External Resistor						
Frequency	R_{ext} = 180 kΩ	f_{RcOut2}		4		MHz
Stability	V_{DD} = 2.0 to 6.5 V T_{amb} = -40 to 125° C	Δf/f			+15 -20	%
Stabilization time		t_S			10	µs
4-MHz Crystal Oscillator (Operating Range V_{DD} = 2.2 V to 6.5 V)						
Frequency		f_X		4		MHz
Start-up time		t_{SQ}		5		ms
Stability		Δf/f	-10		10	ppm
Integrated input/output capacitances (configurable)	C_{IN}/C_{OUT} programmable	C_{IN} C_{OUT}	0, 2, 5, 7, 10 or 12 0, 2, 5, 7, 10 or 12			pF pF

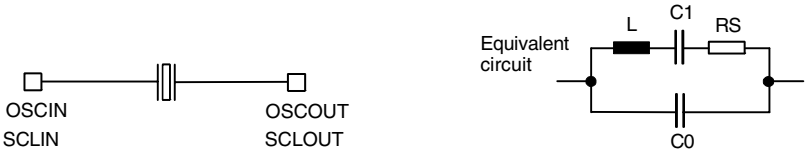
10. AC Characteristics (Continued)

Supply voltage V_{DD} = 1.8 to 6.5 V, V_{SS} = 0 V, T_{amb} = 25°C unless otherwise specified.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
32-kHz Crystal Oscillator (Operating Range V_{DD} = 2.0 V to 6.5 V)						
Frequency		f_X		32.768		kHz
Start-up time		t_{SQ}		0.5		s
Stability		$\Delta f/f$	-10		10	ppm
Integrated input/output capacitances (configurable)	C_{IN}/C_{OUT} programmable	C_{IN} C_{OUT}	0, 2, 5, 7, 10 or 12 0, 2, 5, 7, 10 or 12			pF pF
External 32-kHz Crystal Parameters						
Crystal frequency		f_X		32.768		kHz
Serial resistance		RS		30	50	kΩ
Static capacitance		C0		1.5		pF
Dynamic capacitance		C1		3		fF
External 4-MHz Crystal Parameters						
Crystal frequency		f_X		4.0		MHz
Serial resistance		RS		40	150	Ω
Static capacitance		C0		1.4	3	pF
Dynamic capacitance		C1		3		fF
EEPROM						
Operating current during erase/write cycle		I_{WR}		600	1300	µA
Endurance, erase-/write cycles		E_D	500000	1000000		Cycles
	T_{amb} = 125°C	E_D	10000	20000		Cycles
Data erase/write cycle time	For 16-bit access	t_{DEW}		9	13	ms
Data retention time		t_{DR}	100			Years
	T_{amb} = 85°C	t_{DR}	1			Years
Power-up to read operation		t_{PUR}			0.2	ms
Power-up to write operation		t_{PUW}			0.2	ms
Program EEPROM	Erase-/write cycles, T_{amb} = 0 to 40°C	n_{EW}	100	1000		Cycles
Serial Interface						
SCL clock frequency		f_{SC_MCL}		100	500	kHz

11. Crystal Characteristics

Figure 11-1. Crystal Equivalent Circuit



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
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ASIC/ASSP/Smart Cards
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Maxwell Building
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Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
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74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

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Fax: 1(719) 540-1759

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Fax: (33) 4-76-58-34-80

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