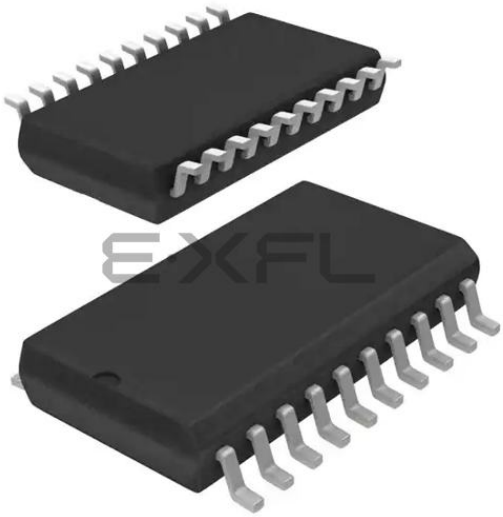

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MARC4
Core Size	4-Bit
Speed	4MHz
Connectivity	SSI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	EEPROM
EEPROM Size	64 x 16
RAM Size	256 x 4
Voltage - Supply (Vcc/Vdd)	1.8V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-SSO
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atam893t-tks

4.2.5 I/O Bus

The I/O ports and the registers of the peripheral modules are I/O mapped. All communication between the core and the on-chip peripherals takes place via the I/O bus and the associated I/O control. With the MARC4 IN and OUT instructions the I/O bus allows a direct read or write access to one of the 16 primary I/O addresses. More about the I/O access to the on-chip peripherals is described in the section “Peripheral Modules”. The I/O bus is internal and is not accessible by the customer on the final microcontroller device, but it is used as the interface for the MARC4 emulation (see section “Emulation”).

4.2.6 Instruction Set

The MARC4 instruction set is optimized for the high level programming language qFORTH. Many MARC4 instructions are qFORTH words. This enables the compiler to generate a fast and compact program code. The CPU has an instruction pipeline allowing the controller to prefetch an instruction from program memory at the same time as the present instruction is being executed. The MARC4 is a zero address machine, the instructions containing only the operation to be performed and no source or destination address fields. The operations are implicitly performed on the data placed on the stack. There are one and two byte instructions which are executed within 1 to 4 machine cycles. A MARC4 machine cycle is made up of two system clock cycles (SYSCL). Most of the instructions are only one byte long and are executed in a single machine cycle. For more information refer to the “MARC4 Programmer's Guide”.

4.2.7 Interrupt Structure

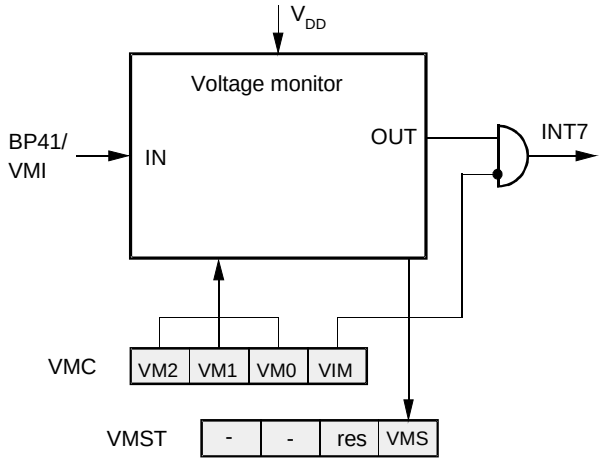
The MARC4 can handle interrupts with eight different priority levels. They can be generated from the internal and external interrupt sources or by a software interrupt from the CPU itself. Each interrupt level has a hard-wired priority and an associated vector for the service routine in the program memory (see Table 4-2 on page 11). The programmer can postpone the processing of interrupts by resetting the interrupt enable flag (I) in the CCR. An interrupt occurrence will still be registered, but the interrupt routine only started after the I flag is set. All interrupts can be masked, and the priority individually software configured by programming the appropriate control register of the interrupting module (see section “Peripheral Modules”).

4.2.7.1 Interrupt Processing

For processing the eight interrupt levels, the MARC4 includes an interrupt controller with two 8-bit wide “interrupt pending” and “interrupt active” registers. The interrupt controller samples all interrupt requests during every non-I/O instruction cycle and latches these in the interrupt pending register. If no higher priority interrupt is present in the interrupt active register, it signals the CPU to interrupt the current program execution. If the interrupt enable bit is set, the processor enters an interrupt acknowledge cycle. During this cycle a short call (SCALL) instruction to the service routine is executed and the current PC is saved on the return stack.

An interrupt service routine is completed with the RTI instruction. This instruction resets the corresponding bits in the interrupt pending/active register and fetches the return address from the return stack to the program counter. When the interrupt enable flag is reset (triggering of interrupt routines are disabled), the execution of new interrupt service routines is inhibited but not the logging of the interrupt requests in the interrupt pending register. The execution of the interrupt is delayed until the interrupt enable flag is set again. Note that interrupts are only lost if an interrupt request occurs while the corresponding bit in the pending register is still set (i.e., the interrupt service routine is not yet finished).

Figure 4-9. Voltage Monitor



4.4.1 Voltage Monitor Control/Status Register

Primary register address: 'F'hex

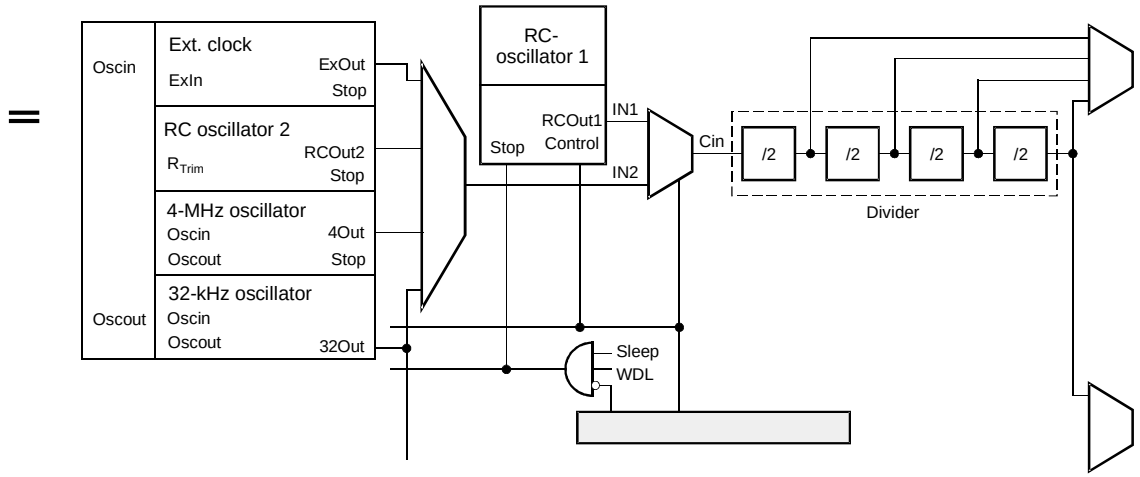
	Bit 3	Bit 2	Bit 1	Bit 0	
VMC: Write	VM2	VM1	VM0	VIM	Reset value: 1111b
VMST: Read	–	–	reserved	VMS	Reset value: xx11b

VM2: Voltage monitor Mode bit 2
VM1: Voltage monitor Mode bit 1
VM0: Voltage monitor Mode bit 0

Table 4-3. Voltage Monitor Modes

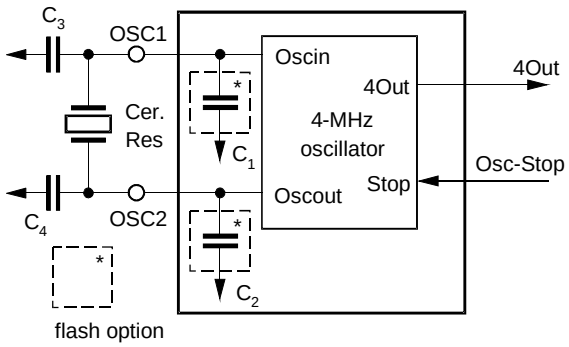
The clock module is programmable via software with the clock management register (CM) and the system configuration register (SC). The required oscillator configuration can be selected with the OS1 bit and the OS0 bit in the SC register. A programmable 4-bit divider stage allows the adjustment of the system clock speed. A special feature of the clock management is that an external oscillator may be used and switched on and off via a port pin for the power-down mode. Before the external clock is switched off, the internal RC-oscillator 1 must be selected with the CCS bit and then the SLEEP mode may be activated. In this state an interrupt can wake up the controller with the RC-oscillator, and the external oscillator can be activated and selected by software. A synchronization stage avoids clock periods that are too short if the clock source or the clock speed is changed. If an external input clock is selected, a supervisor circuit monitors the external input and generates a hardware reset if the external clock source fails or drops below 500 kHz for more than 1 ms.

Figure 4-12. Clock Module



The clock module generates two output clocks. One is the system clock (SYSCL) and the other the periphery (SUBCL). The SYSCL can supply the core and the peripherals and the SUBCL can supply only the peripherals with clocks. The modes for clock sources are programmable with the OS1 bit and OS0 bit in the SC register and the CCS bit in the CM register.

Figure 4-17. Ceramic Resonator

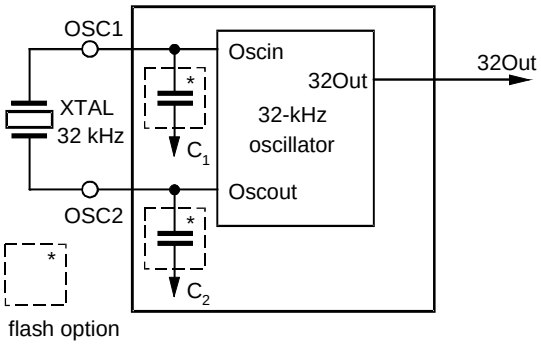


Note: Both, the 4-MHz and the 32-kHz crystal oscillator, use an integrated 14 stage divider circuit to stabilize oscillation before the oscillator output is used as system clock. This results in an additional delay of about 4 ms for the 4-MHz crystal and about 500 ms for the 32-kHz crystal.

4.5.2.5 32-kHz Oscillator

Some applications require long-term time keeping or low resolution timing. In this case, an on-chip, low power 32-kHz crystal oscillator can be used to generate both the SUBCL and the SYSCL. In this mode, power consumption is greatly reduced. The 32-kHz crystal oscillator can not be stopped while the power-down mode is in operation.

Figure 4-18. 32-kHz Crystal Oscillator



Note: Both, the 4-MHz and the 32-kHz crystal oscillator, use an integrated 14 stage divider circuit to stabilize oscillation before the oscillator output is used as system clock. This results in an additional delay of about 4 ms for the 4-MHz crystal and about 500 ms for the 32-kHz crystal.

4.5.3 Clock Management

The clock management register controls the system clock divider and synchronization stage. Writing to this register triggers the synchronization cycle.

4.5.3.1 Clock Management Register (CM)

Auxiliary register address: '3'hex

	Bit 3	Bit 2	Bit 1	Bit 0	
CM:	**NSTOP**	**CCS**	**CSS1**	**CSS0**	**Reset value: 1111b**

NSTOP — **N**ot **STOP** peripheral clock
NSTOP = 0, stops the peripheral clock while the core is in SLEEP mode
NSTOP = 1, enables the peripheral clock while the core is in SLEEP mode

CCS — **C**ore **C**lock **S**elect
CCS = 1, the internal RC-oscillator 1 generates SYSCL
CCS = 0, the 4-MHz crystal oscillator, the 32-kHz crystal oscillator, an external clock source or the RC-oscillator 2 with the external resistor at OSC1 generates SYSCL dependent on the setting of OS0 and OS1 in the system configuration register

CSS1 — **C**ore **S**peed **S**elect **1**

CSS0 — **C**ore **S**peed **S**elect **0**

Table 4-6. Core Speed Select

CSS1	CSS0	Divider	Note
0	0	16	
1	1	8	Reset value
1	0	4	
0	1	2	

4.5.3.2 System Configuration Register (SC)

Primary register address: '3'hex

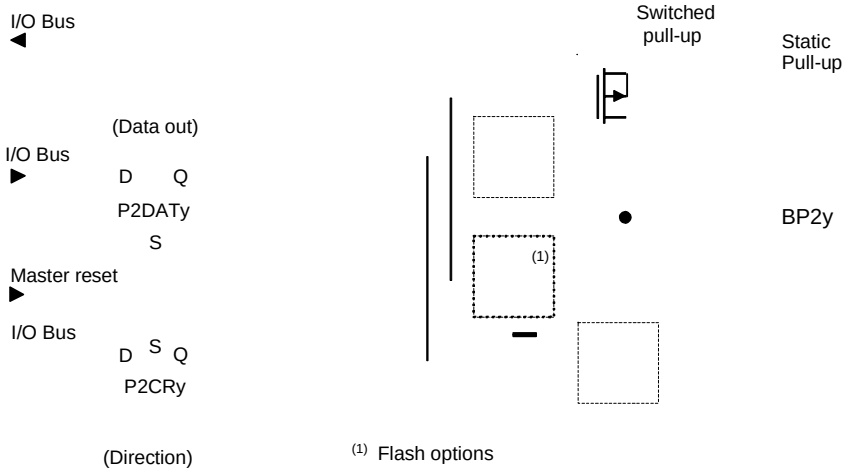
	Bit 3	Bit 2	Bit 1	Bit 0	
SC: write	**BOT**	**–**	**OS1**	**OS0**	**Reset value: 1x11b**

BOT — **B**rown-**O**ut **T**hreshold
BOT = 1, low brown-out voltage threshold (1.65 V)
BOT = 0, high brown-out voltage threshold (1.95 V)

OS1 — **O**scillator **S**elect **1**

OS0 — **O**scillator **S**elect **0**

Figure 5-3. Bi-directional Port 2



5.2.2.1 Port 2 Data Register (P2DAT)

Bit 3 = MSB, Bit 0 = LSB

5.2.2.2 Port 2 Control Register (P2CR)

Value 1111b means all pins in input mode

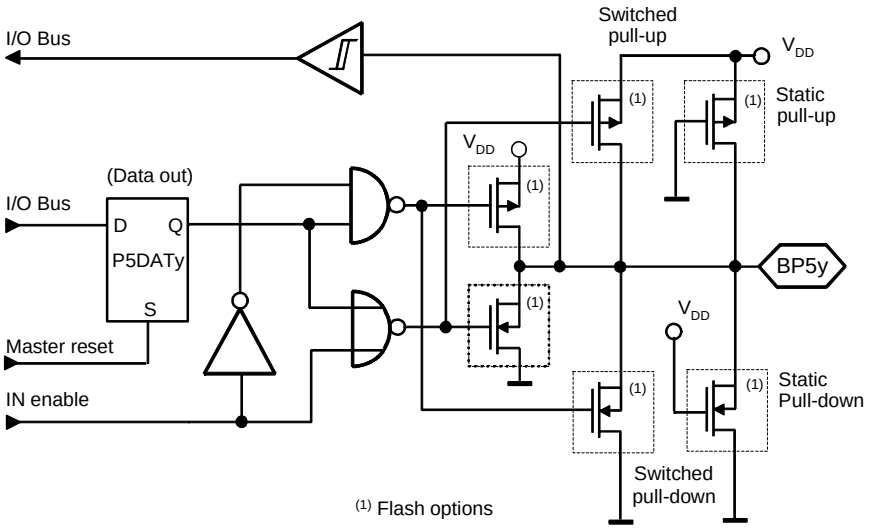
5.2.3 Bi-directional Port 5

As all other bi-directional ports, this port includes a bit-wise programmable Control Register (P5CR), which allows the individual programming of each port bit as input or output. It also opens up the possibility of reading the pin condition when in output mode. This is a useful feature for self testing and for serial bus applications.

The port pins can also be used as external interrupt inputs (see Figure 5-4 and Figure 5-5 on page 28). The interrupts (INT1 and INT6) can be masked or independently configured to trigger on either edge. The interrupt configuration and port direction is controlled by the Port 5 Control Register (P5CR). An additional low resistance pull-up/-down transistor mask option provides an internal bus pull-up for serial bus applications.

The Port 5 Data Register (P5DAT) is I/O mapped to the primary address register of address '5'h and the Port 5 Control Register (P5CR) to the corresponding auxiliary register. The P5CR is a byte-wide register and is configured by writing first the low nibble and then the high nibble (see Section 5.1 on page 22).

Figure 5-4. Bi-directional Port 5



This timer starts running automatically after any power-on reset! If the watchdog function is not activated, the timer can be restarted by writing into the T1C1 register with T1RM = 1.

Timer 1 can also be used as a watchdog timer to prevent a system from stalling. The watchdog timer is a 3-bit counter that is supplied by a separate output of Timer 1. It generates a system reset when the 3-bit counter overflows. To avoid this, the 3-bit counter must be reset before it overflows. The application software has to accomplish this by reading the CWD register.

After power-on reset the watchdog must be activated by software in the $RESET initialization routine. There are two watchdog modes, in one mode the watchdog can be switched on and off by software, in the other mode the watchdog is active and locked. This mode can only be stopped by carrying out a system reset.

The watchdog timer operation mode and the time interval for the watchdog reset can be programmed via the watchdog control register (WDC).

Figure 5-8. Timer 1 Module

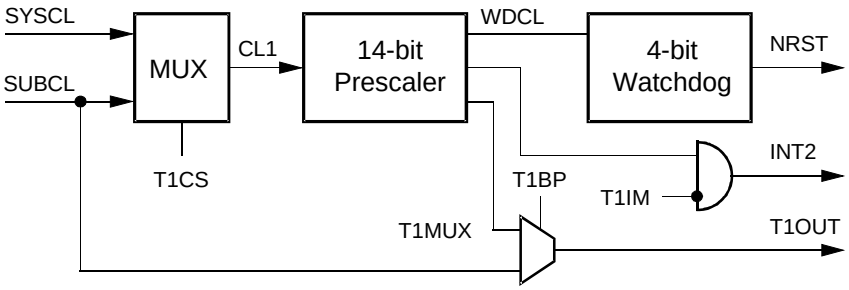
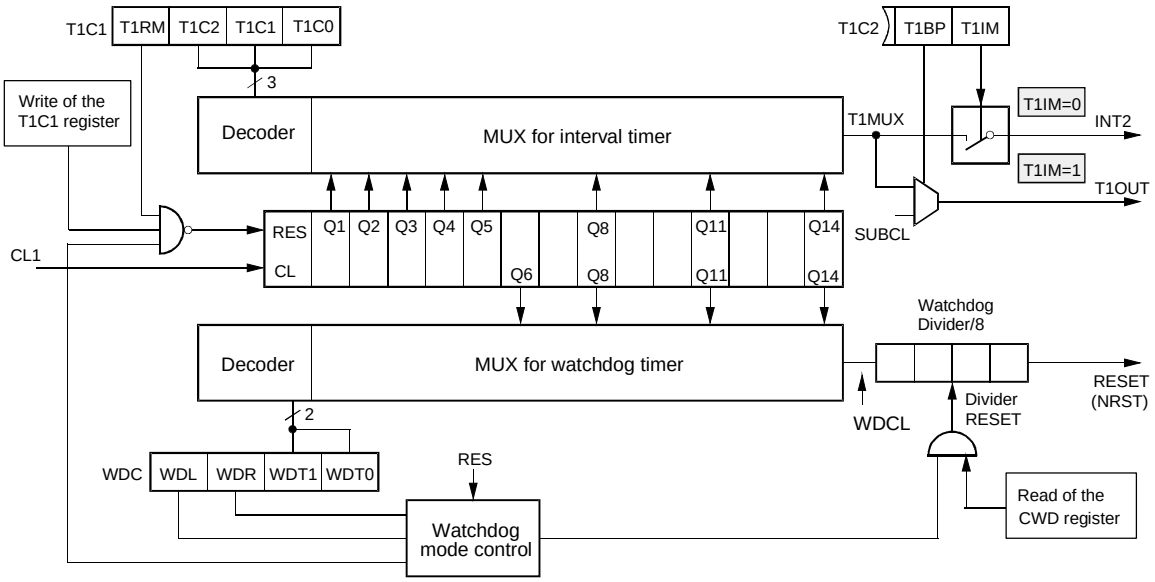


Figure 5-9. Timer 1 and Watchdog



5.3.1.2 Timer 1 Control Register 2 (T1C2)

Address: ’7’hex - Subaddress: ’9’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T1C2	**–**	**T1BP**	**T1CS**	**T1IM**	**Reset value: x111b**

Bit 3 = MSB, Bit 0 = LSB

T1BP	**T**imer **1** SUBCL **B**y**P**assed T1BP = 1, TIOUT = T1MUX T1BP = 0, T1OUT = SUBCL
T1CS	**T**imer **1** input **C**lock **S**elect T1CS = 1, CL1 = SUBCL (see Figure 5-8 on page 33) T1CS = 0, CL1 = SYSCL (see Figure 5-8 on page 33)
T1IM	**T**imer **1** **I**nterrupt **M**ask T1IM = 1, disables Timer 1 interrupt T1IM = 0, enables Timer 1 interrupt

5.3.1.3 Watchdog Control Register (WDC)

Address: ’7’hex - Subaddress: ’A’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
WDC	**WDL**	**WDR**	**WDT1**	**WDT0**	**Reset value: 1111b**

Bit 3 = MSB, Bit 0 = LSB

WDL	**W**atch**D**og **L**ock mode WDL = 1, the watchdog can be enabled and disabled by using the WDR-bit WDL = 0, the watchdog is enabled and locked. In this mode the WDR-bit has no effect. After the WDL-bit is cleared, the watchdog is active until a system reset or power-on reset occurs.
WDR	**W**atch**D**og **R**un and stop mode WDR = 1, the watchdog is stopped/disabled WDR = 0, the watchdog is active/enabled
WDT1	**W**atch**D**og **T**ime **1**
WDT0	**W**atch**D**og **T**ime **0**

Both these bits control the time interval for the watchdog reset.

5.3.2.5 *Timer 2 Control Register (T2C)*

Address: '7'hex — Subaddress: '0'hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T2C	**T2CS1**	**T2CS0**	**T2TS**	**T2R**	**Reset value: 0000b**

T2CS1 **T**imer **2** **C**lock **S**elect bit **1**

T2CS0 **T**imer **2** **C**lock **S**elect bit **0**

T2TS **T**imer **2** **T**oggle with **S**tart
T2TS = 0, the output flip-flop of Timer 2 is not toggled with the timer start
T2TS = 1, the output flip-flop of Timer 2 is toggled when the timer is started with T2R

T2R **T**imer **2** **R**un
T2R = 0, Timer 2 stop and reset
T2R = 1, Timer 2 run

Table 5-8. Timer 2 Clock Select Bits

T2CS1	T2CS0	Input Clock (CL 2/1) of Counter Stage 2/1
0	0	System clock (SYSCL)
0	1	Output signal of Timer 1 (T1OUT)
1	0	Internal shift clock of SSI (SCL)
1	1	Output signal of Timer 3 (TOG3)

5.3.2.6 *Timer 2 Mode Register 1 (T2M1)*

Address: '7'hex — Subaddress: '1'hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T2M1	**T2D1**	**T2D0**	**T2MS1**	**T2MS0**	**Reset value: 1111b**

T2D1 **T**imer **2** **D**uty cycle bit **1**

T2D0 **T**imer **2** **D**uty cycle bit **0**

T2MS1 **T**imer **2** **M**ode **S**elect bit **1**

T2MS0 **T**imer **2** **M**ode **S**elect bit **0**

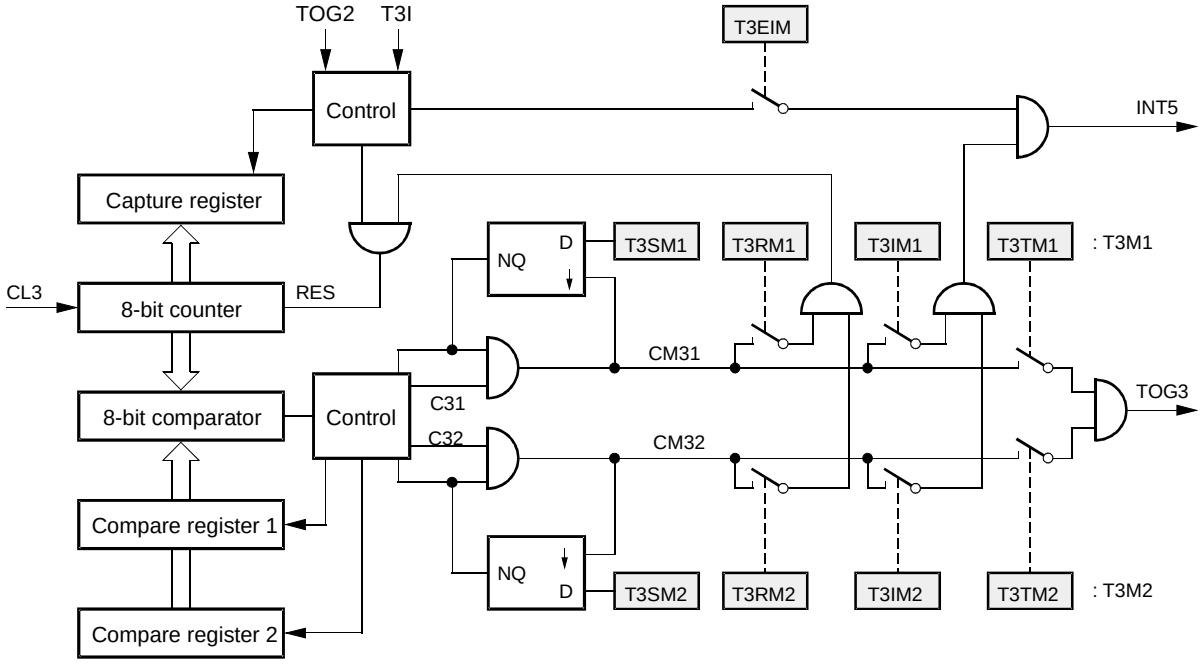
Table 5-9. Timer 2 Duty Cycle Bits

T2D1	T2D0	Function of Duty Cycle Generator (DCG)	Additional Divider Effect
1	1	Bypassed (DCGO0)	/1
1	0	Duty cycle 1/1 (DCGO1)	/2
0	1	Duty cycle 1/2 (DCGO2)	/3
0	0	Duty cycle 1/3 (DCG03)	/4

A special feature of this timer is the trigger- and single-action mode. In trigger mode, the counter starts counting triggered by the external signal at its input. In single-action mode, the counter counts only one time up to the programmed compare match event. These modes are very useful for modulation, demodulation, signal generation, signal measurement and phase control. For phase control, the timer input is protected against negative voltages and has zero-cross detection capability.

Timer 3 has a modulator output stage and input functions for demodulation. As modulator it works together with Timer 2 or the serial interface. When the shift register is used for modulation the data shifted out of the register is encoded bit-wise. In all demodulation modes, the decoded data bits are shifted automatically into the shift register.

Figure 5-25. Counter 3 Stage



5.3.3.2 Timer/Counter Modes

Timer 3 has 6 timer modes and 6 modulator/demodulator modes. The mode is set via the Timer 3 Mode Register T3M.

In all these modes, the compare register and the compare-mode register belonging to it define the counter value for a compare match and the action of a compare match. A match of the current counter value with the content of one compare register triggers a counter reset, a Timer 3 interrupt or the toggling of the output flip-flop. The compare mode registers T3M1 and T3M2 contain the mask bits for enabling or disabling these actions.

The counter can also be enabled to execute single actions with one or both compare registers. If this mode is set the corresponding compare match event is generated only once after the counter starts.

Table 5-13. Timer 3 Mode Select Bits (Continued)

Mode	T3M3	T3M2	T3M1	T3M0	Timer 3 Modes
8	1	0	0	0	FSK modulation with shift register (SO)
9	0	1	1	1	Pulse-width modulation with shift register (SO) and Timer 2 (TOG2), internal trigger restart (SCO) →counter reset
10	0	1	1	0	Manchester demodulation/pulse-width demodulation(1) (T2O →T3O)
11	0	1	0	1	Bi-phase demodulation(1) (T2O →T3O)
12	0	1	0	0	Timer/counter with external capture mode (T3I)
13	0	0	1	1	Not allowed
14	0	0	1	0	Not allowed
15	0	0	0	1	Not allowed
16	0	0	0	0	Not allowed

Note: 1. In this mode, the SSI can be used only as demodulator (8-bit NRZ rising edge). All other SSI modes are not allowed.

5.3.3.8 Timer 3 Control Register 1 (T3C) Write

Primary register address: 'C'hex — Write

	Bit 3	Bit 2	Bit 1	Bit 0	
Write	**T3EIM**	**T3TOP**	**T3TS**	**T3R**	**Reset value: 0000b**

T3EIM — **T**imer **3** **E**dge **I**nterrupt **M**ask
T3EIM = 0, disables the interrupt when an edge event for Timer 3 occurs (T3I)
T3EIM = 1, enables the interrupt when an edge event for Timer 3 occurs (T3I)

T3TOP — **T**imer **3** **T**oggle **O**utput **P**reset T3TOP = 0, sets toggle output (M3) to '0'
..... T3TOP = 1, sets toggle output (M3) to '1'
..... Note: If T3R = 1, no output preset is possible

T3TS — **T**imer **3** **T**oggle with **S**tart . T3TS = 0, Timer 3 output is not toggled during the start
..... T3TS = 1, Timer 3 output is toggled if started with T3R

T3R — **T**imer **3** **R**un ..... T3R = 0, Timer 3 stop and reset
..... T3R = 1, Timer 3 run

5.3.3.9 *Timer 3 Status Register 1 (T3ST) Read*

Primary register address: 'C'hex — Read

	Bit 3	Bit 2	Bit 1	Bit 0	
Read	**- - -**	**T3ED**	**T3C2**	**T3C1**	**Reset value: x000b**

T3ED **T**imer **3** **E**dge **D**etect
This bit will be set by the edge-detect logic of Timer 3 input (T3I)

T3C2 **T**imer **3** **C**ompare **2**
This bit will be set when a match occurs between Counter 3 and T3CO2

T3C1 **T**imer **3** **C**ompare **1**
This bit will be set when a match occurs between Counter 3 and T3CO1

Note: The status bits T3C1, T3C2 and T3ED will be reset after a READ access to T3ST.

5.3.3.10 *Timer 3 Clock Select Register (T3CS)*

Address: 'B'hex — Subaddress: '1'hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T3CS	**T3E1**	**T3E0**	**T3CS1**	**T3CS0**	**Reset value: 1111b**

T3E1 **T**imer **3** **E**dge select bit **1**

T3E0 **T**imer **3** **E**dge select bit **0**

Table 5-14. External Input Edge Select Bits

T3E1	T3E0	Timer 3 Input Edge Select (T3I)
1	1	- - -
1	0	Positive edge at T3I pin
0	1	Negative edge at T3I pin
0	0	Each edge at T3I pin

T3CS1 **T**imer **3** **C**lock **S**ource select bit **1**

T3CS0 **T**imer **3** **C**lock **S**ource select bit **0**

Table 5-15. Select Clock Source Bits

T3CS1	TCS0	Counter 3 Input Signal (CL3)
1	1	System clock (SYSCL)
1	0	Output signal of Timer 2 (POUT)
0	1	Output signal of Timer 1 (T1OUT)
0	0	External input signal from T3I edge detect

5.3.4.13 Serial Interface Control Register 2 (SIC2)

Auxiliary register address: 'A'hex

	Bit 3	Bit 2	Bit 1	Bit 0	
SIC2	**MSM**	**SM1**	**SM0**	**SDD**	**Reset value: 1111b**

MSM	**M**odular **S**top **M**ode MSM = 1, modulator stop mode disabled (output masking off) MSM = 0, modulator stop mode enabled (output masking on) - used in modulation modes for generating bit streams which are not sub multiples of 8 bit.
SM1	**S**erial **M**ode control bit **1**
SM0	**S**erial **M**ode control bit **0**

Table 5-17. Serial Mode Control Bits

Mode	SM1	SM0	SSI Mode
1	1	1	8-bit NRZ-data changes with the rising edge of SC
2	1	0	8-bit NRZ-data changes with the falling edge of SC
3	0	1	9-bit two-wire MCL mode
4	0	0	8-bit two-wire pseudo MCL mode (no acknowledge)

SDD	**S**erial **D**ata **D**irection SDD = 1, transmit mode – SD line used as output (transmit data). SRDY is set by a transmit buffer write access SDD = 0, receive mode – SD line used as input (receive data). SRDY is set by a receive buffer read access

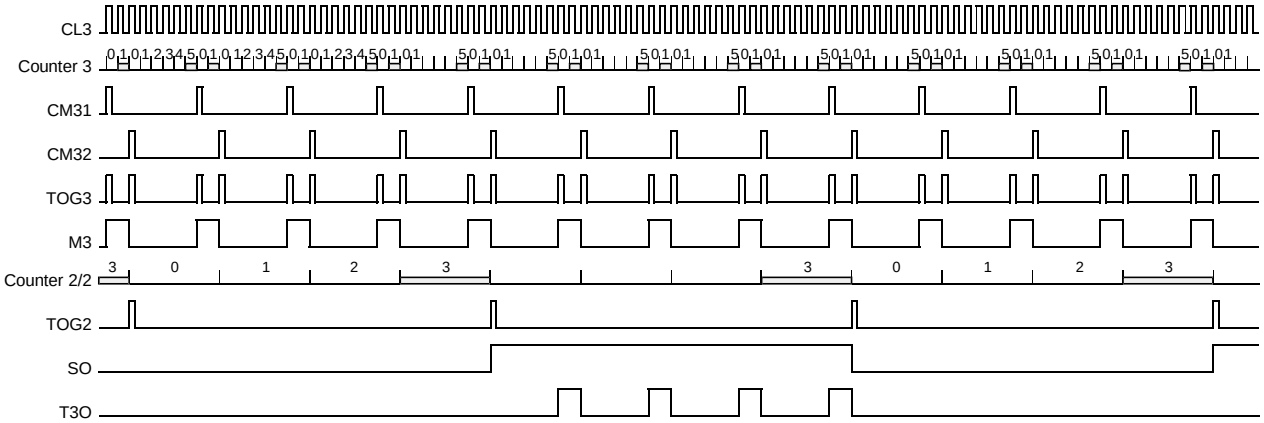
Note: SDD controls port directional control and defines the reset function for the SRDY-flag

Combination Mode 12: Burst Modulation 2

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 3
Timer 2 output mode 2: Timer 2 output mode 1/6:	8-bit compare counter and 4-bit prescaler Timer 2 compare match toggles (TOG2) to the SSI
Timer 3 mode 7:	Carrier frequency burst modulation controlled by the internal output (SO) of SSI

The Timer 3 counter is driven by an internal or external clock source. Its compare- and compare mode registers must be programmed to generate the carrier frequency with the output toggle flip-flop (M3). The internal data output (SO) of the SSI is used to enable and disable the Timer 3 output. The SSI can be supplied with the toggle signal of Timer 2.

Figure 5-64. Burst Modulation 2



Combination Mode 13: FSK Modulation

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 3
Timer 2 output mode 3: Timer 2 output mode 1/6:	8-bit compare counter and 4-bit prescaler Timer 2 4-bit compare match signal (POUT) to the SSI
Timer 3 mode 8:	FSK modulation with shift register data output (SO)

The two compare registers are used to generate two different time intervals. The SSI data output selects which compare register is used for the output frequency generation. A '0' level at the SSI data output enables the compare register 1 and a '1' level enables the compare register 2. The compare- and compare mode registers must be programmed to generate the two frequencies via the output toggle flip-flop. The SSI can be supplied with the toggle signal of Timer 2 or any other clock source. The Timer 3 counter is driven by an internal or external clock source.

6.2.2.2 Write One Data Byte

Start	Control byte	A	Data byte 1	A	Stop

6.2.2.3 Write Two Data Bytes

Start	Control byte	A	Data byte 1	A	Data byte 2	A	Stop

6.2.2.4 Write Control Byte Only

Start	Control byte	A	Stop

6.2.2.5 Write Control Bytes

Write low byte first

MSB							LSB
A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					0	1	0

Byte order

LB(R)	HB(R)

Write high byte first

MSB							LSB
A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					1	0	0

Byte order

HB(R)	LB(R)

A →acknowledge; HB: high byte; LB: low byte; R: row address

6.2.3 Read Operations

The EEPROM allows byte-, word- and current address read operations. The read operations are initiated in the same way as write operations. Every read access is initiated by sending the START condition followed by the control byte which contains the address and the read mode. When the device has received a read command, it returns an acknowledge, loads the addressed word into the read/write buffer and sends the selected data byte to the master. The master has to acknowledge the received byte if it wants to proceed with the read operation. If two bytes are read out from the buffer the device increments respectively decrements the word address automatically and loads the buffer with the next word. The read mode bits determines if the low or high byte is read first from the buffer and if the word address is incremented or decremented for the next read access. If the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The master can terminate the read operation after every byte by not responding with an acknowledge (N) by issuing a stop condition.

9. DC Operating Characteristics (Continued)

V_{SS} = 0 V, T_{amb} = -40 to 125°C unless otherwise specified.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power-on Reset Threshold Voltage						
POR threshold voltage	BOT = 1	V_{POR}	1.54	1.7	1.88	V
POR threshold voltage	BOT = 0	V_{POR}	1.83	2.0	2.20	V
POR hysteresis		V_{POR}		50		mV
Voltage Monitor Threshold Voltage						
VM high threshold voltage	V_{DD} > VM, VMS = 1	V_{MThh}		3.0	3.35	V
VM high threshold voltage	V_{DD} < VM, VMS = 0	V_{MThh}	2.74	3.0		V
VM middle threshold voltage	V_{DD} > VM, VMS = 1	V_{MThm}		2.6	2.9	V
VM middle threshold voltage	V_{DD} < VM, VMS = 0	V_{MThm}	2.38	2.6		V
VM low threshold voltage	V_{DD} > VM, VMS = 1	V_{MThl}		2.2	2.44	V
VM low threshold voltage	V_{DD} < VM, VMS = 0	V_{MThl}	2.0	2.2		V
External Input Voltage						
VMI	V_{DD} = 3 V, VMS = 1	V_{VMI}		1.3	1.44	V
VMI	V_{DD} = 3 V, VMS = 0	V_{VMI}	1.16	1.3		V
All Bi-directional Ports						
Input voltage LOW	V_{DD} = 1.8 to 6.5 V	V_{IL}	V_{SS}		$0.2 \times V_{DD}$	V
Input voltage HIGH	V_{DD} = 1.8 to 6.5 V	V_{IH}	$0.8 \times V_{DD}$		V_{DD}	V
Input LOW current (switched pull-up)	V_{DD} = 2.0 V, V_{DD} = 3.0 V, $V_{IL} = V_{SS}$ V_{DD} = 6.5 V	I_{IL}	-3 -10 -80	-8 -20 -150	-14 -40 -240	µA µA µA
Input HIGH current (switched pull-down)	V_{DD} = 2.0 V, V_{DD} = 3.0 V, $V_{IH} = V_{DD}$ V_{DD} = 6.5 V	I_{IH}	2.5 10 60	8 20 100	14 40 160	µA µA µA
Input LOW current (static pull-up)	V_{DD} = 2.0 V V_{DD} = 3.0 V, $V_{IL} = V_{SS}$ V_{DD} = 6.5 V	I_{IL}	-30 -80 -300	-50 -160 -700	-90 -320 -1200	µA µA µA
Input LOW current (static pull-down)	V_{DD} = 2.0 V V_{DD} = 3.0 V, $V_{IH} = V_{DD}$ V_{DD} = 6.5 V	I_{IH}	20 80 300	50 160 600	100 320 1200	µA µA µA
Input leakage current	$V_{IL} = V_{SS}$	I_{IL}			100	nA
Input leakage current	$V_{IH} = V_{DD}$	I_{IH}			100	nA
Output LOW current	$V_{OL} = 0.2 \times V_{DD}$ V_{DD} = 2.0 V V_{DD} = 3.0 V, V_{DD} = 6.5 V	I_{OL}	0.9 3 8	1.8 5 15	3.6 8 22	mA mA mA
Output HIGH current	$V_{OH} = 0.8 \times V_{DD}$ V_{DD} = 2.0 V V_{DD} = 3.0 V, V_{DD} = 6.5 V	I_{OH}	-0.8 -3 -7	-1.7 -5 -15	-3.4 -8 -24	mA mA mA

Note: The pin BP20/NTE has a static pull-up resistor during the reset-phase of the microcontroller

13. Ordering Information

Extended Type Number[1]	Program Memory	Data-EEPROM	Package	Delivery
ATAM893x-TKSYz	4 kB Flash	2x512 Bit	SSO20	Tubes
ATAM893x-TKQYz	4 kB Flash	2x512 Bit	SSO20	Taped and reeled
ATAM893x-TKHYz	4 kB Flash	2x512 Bit	SSO20	Taped and reeled + Dry pack

Note: 1. x = Hardware revision
z = Operating temperature range
= D (-40°C to +125°C)
Y = Lead-free

14. Package Information

Package SSO20
Dimensions in mm