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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51re2-rltum

Table 3. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer								
DPL	82h	Data Pointer Low byte								
DPH	83h	Data Pointer High byte								

Table 4. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1_0	SMOD0_0	-	POF	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	-	-	M0	XRS2	XRS1	XRS0	EXTRAM	AO
AUXR1	A2h	Auxiliary Register 1	EES	SP9	U2	-	GF2	0	-	DPS
CKRL	97h	Clock Reload Register	-	-	-	-	-	-	-	-
BMSEL	92h	Bank Memory Select	MBO2	MBO1	MBO0		-	FBS2	FBS1	FBS0
CKCON0	8Fh	Clock Control Register 0	TWIX2	WDX2	PCAX2	SIX2_0	T2X2	T1X2	T0X2	X2
CKCON1	AFh	Clock Control Register 1	-	-	-	-	-	-	SIX2_1	SPIX2

Table 5. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	-	-	-	-	ES_1	ESPI	ETWI	EKBD
IPH0	B7h	Interrupt Priority Control High 0	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
IPL0	B8h	Interrupt Priority Control Low 0	-	PPCL	PT2L	PSL	PT1L	PX1L	PT0L	PX0L
IPH1	B3h	Interrupt Priority Control High 1	-	-	-	-	PSH_1	SPIH	IE2CH	KBDH
IPL1	B2h	Interrupt Priority Control Low 1	-	-	-	-	PSL_1	SPIL	IE2CL	KBDL

Table 6. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								

Enhanced Features

In comparison to the original 80C52, the AT89C51RE2 implements some new features, which are:

- X2 option
- Dual Data Pointer
- Extended RAM
- Extended stack
- Programmable Counter Array (PCA)
- Hardware Watchdog
- SPI interface
- 4-level interrupt priority system
- power-off flag
- ONCE mode
- ALE disabling
- Enhanced features on the UART and the timer 2

X2 Feature

The AT89C51RE2 core needs only 6 clock periods per machine cycle. This feature called ‘X2’ provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically the operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

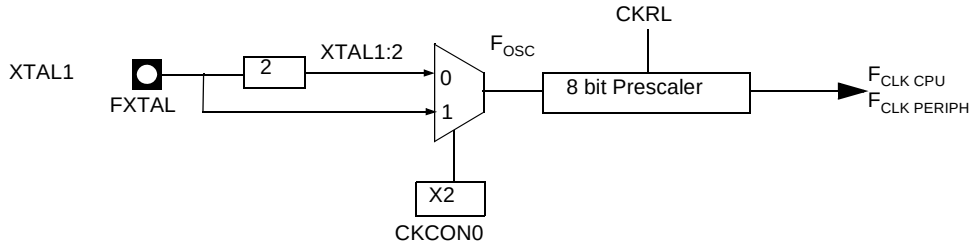
Description

The clock for the whole circuit and peripherals is first divided by two before being used by the CPU core and the peripherals.

This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%.

Figure 2 shows the clock generation block diagram. X2 bit is validated on the rising edge of the XTAL1÷2 to avoid glitches when switching from X2 to STD mode. Figure 3 shows the switching mode waveforms.

Figure 2. Clock Generation Diagram



```
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

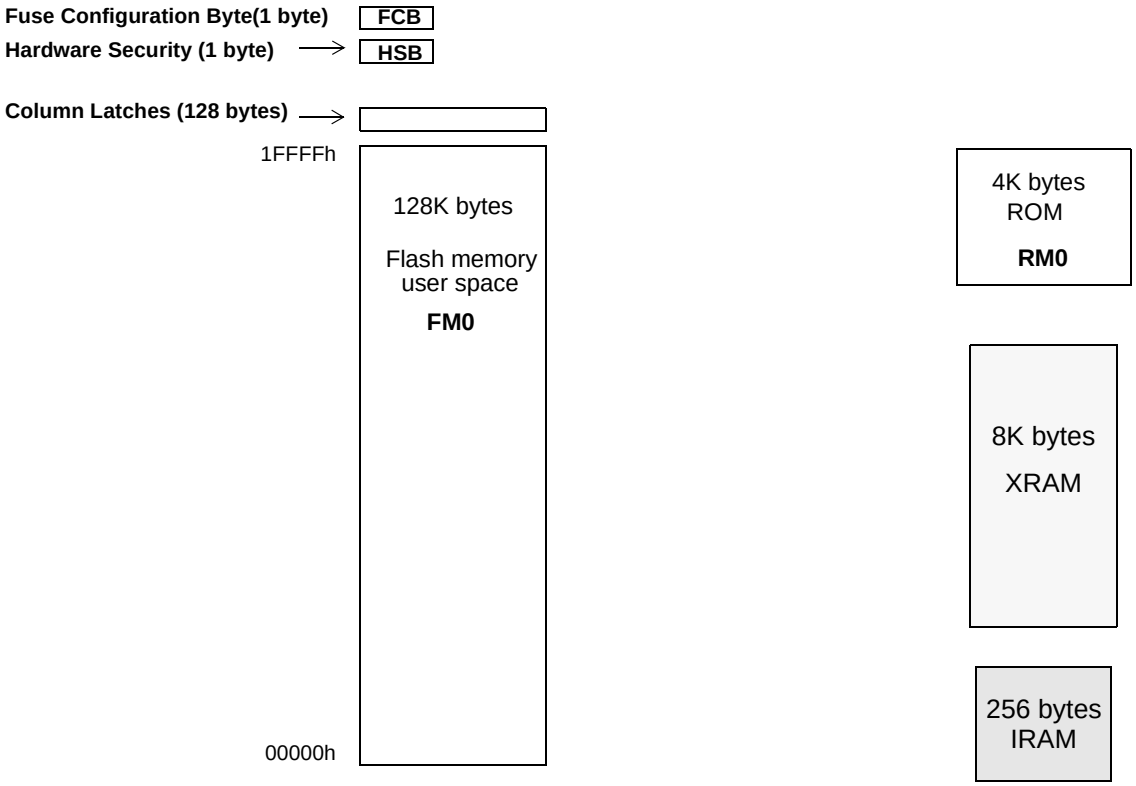
Memory Architecture

AT89C51RE2 features several on-chip memories:

- Flash memory:
  containing 128 Kbytes of program memory (user space) organized into 128 bytes pages.
- Boot ROM:
  4K bytes for boot loader.
- 8K bytes internal XRAM

Physical memory organisation

Figure 5. Physical memory organisation



FCON Register

Table 23. FCON Register

FCON Register (S:D1h)
Flash Control Register

7	6	5	4	3	2	1	0
FPL3	**FPL2**	**FPL1**	**FPL0**	**FPS**	**FMOD2**	**FMOD1**	**FMOD0**

Bit Number	Bit Mnemonic	Description
7-4	FPL3:0	**Programming Launch Command Bits** Write 5Xh followed by AXh to launch the programming according to FMOD2:0. (see Table 26.)
3	FPS	**Flash Map Program Space** When this bit is set: The MOVX @DPTR, A instruction writes in the columns latches space When this bit is cleared: The MOVX @DPTR, A instruction writes in the regular XDATA memory space
2-0	FMOD2:0	**Flash Mode** These bits allow to select the target memory area and operation on FM0 See Table 25.

Reset Value= 0000 0000b

Table 29. Write MOVX @DPTR,A

FPS of FCCON	EA	XRAM ERAM	CL FM0
0	X	winner	
1	1		winner
	0	winner	

Table 30. MOVC A, @A+DPTR executed from External code EA=0

FMOD2:0	FBS (Fetch)	MBO (Target)	MOVC A,@A+DPTR
X	X	X	Read External Code

Table 31. MOVC A, @A+DPTR executed from External code EA=1, PC>=0x8000, FBS=Bank3

FMOD2:0	MBO (Target)	DPTR	MOVC A,@A+DPTR
X	X	< 0x8000	Depends on FLB2:0 Can Returns Random value, for secured part.
	X	>= 0x8000	External code read

Bootloader Description

Entry points

After reset only one bootloader entry point is possible. This entry point stands at address 0x0000 of the boot ROM memory. This entry point executes the boot process of the bootloader.

The bootloader entry point can be selected through two processes:

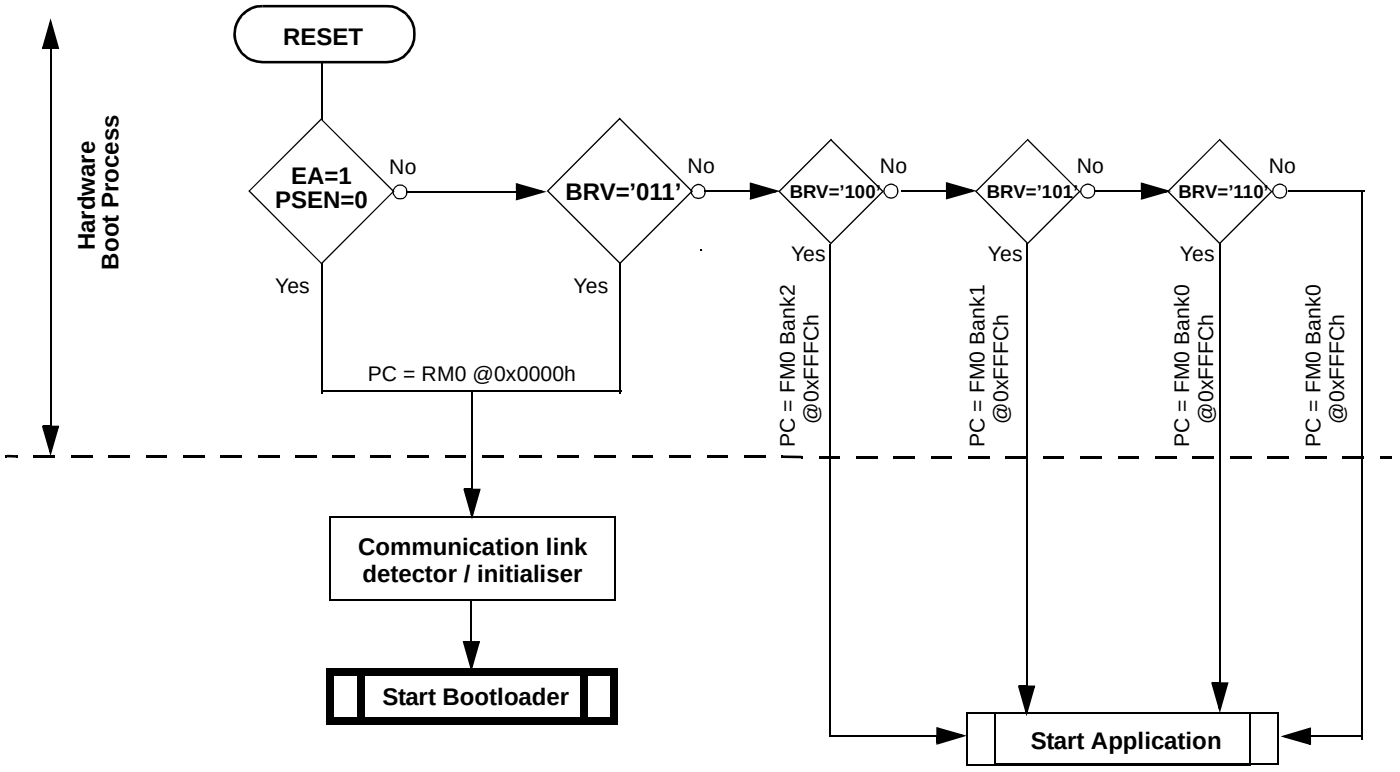
At reset, if the hardware conditions are applied, the bootloader entry point is accessed and executed.

At reset, if the hardware conditions are not set and the BRV2-0 is programmed ‘011’, the bootloader entry point is accessed and the bootprocess is started.

Boot Process Description

The boot process consists in three main operations:

- The hardware boot process request detection
- The communication link detection (Uart or OCD)
- The start-up of the bootloader



Hardware boot process request detection

The hardware boot process request is detected when the hardware conditions (under reset, EA=1 and PSEN=0) are received by the processor or when no hardware condition is applied and the BRV2:0 is configured ‘011’.

Communication link detection

Two interfaces are available for ISP:

- UART0
- OCD UART

Erasing commands The erasing command is supported by the following areas:

Table 39. Memory space & Erase

Memory/Information Family	Comments/Restriction
FLASH	need security level check

Nothing is done on the other areas.

FLASH The erasing command on the Flash memory:

- erases the four physical flash memory banks (from address 0000h to 1FFFFh).
- the HSB (Hardware Security Byte) is set at NO_PROTECTION:
  - FLB2.0 = ‘111’

Registers

Table 46. TCON Register

TCON (S:88h)
Timer/Counter Control Register

7	6	5	4	3	2	1	0
TF1	**TR1**	**TF0**	**TR0**	**IE1**	**IT1**	**IE0**	**IT0**

Bit Number	Bit Mnemonic	Description
7	TF1	**Timer 1 Overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on Timer/Counter overflow, when Timer 1 register overflows.
6	TR1	**Timer 1 Run Control Bit** Clear to turn off Timer/Counter 1. Set to turn on Timer/Counter 1.
5	TF0	**Timer 0 Overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on Timer/Counter overflow, when Timer 0 register overflows.
4	TR0	**Timer 0 Run Control Bit** Clear to turn off Timer/Counter 0. Set to turn on Timer/Counter 0.
3	IE1	**Interrupt 1 Edge Flag** Cleared by hardware when interrupt is processed if edge-triggered (see IT1). Set by hardware when external interrupt is detected on INT1# pin.
2	IT1	**Interrupt 1 Type Control Bit** Clear to select low level active (level triggered) for external interrupt 1 (INT1#). Set to select falling edge active (edge triggered) for external interrupt 1.
1	IE0	**Interrupt 0 Edge Flag** Cleared by hardware when interrupt is processed if edge-triggered (see IT0). Set by hardware when external interrupt is detected on INT0# pin.
0	IT0	**Interrupt 0 Type Control Bit** Clear to select low level active (level triggered) for external interrupt 0 (INT0#). Set to select falling edge active (edge triggered) for external interrupt 0.

Reset Value = 0000 0000b

Baud Rate Selection for UART 1 for Mode 1 and 3

The Baud Rate Generator for transmit and receive clocks can be selected separately via the T2CON and BDRCON_1 registers.

Figure 41. Baud Rate Selection for UART 1

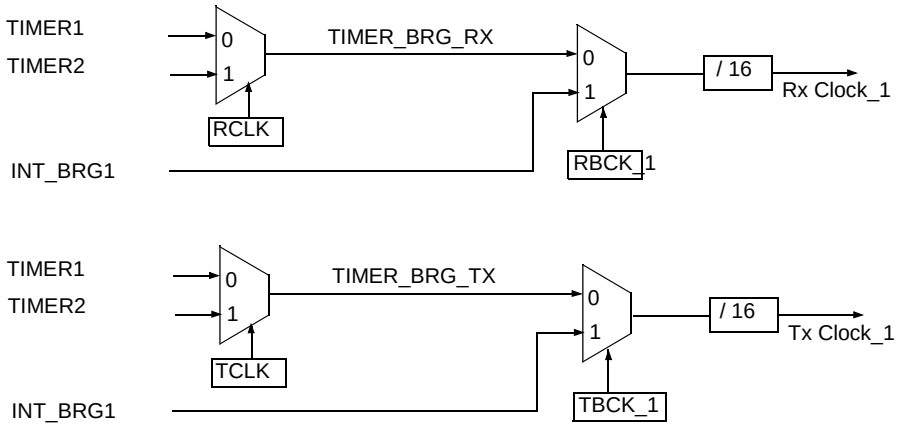


Table 67. Baud Rate Selection Table UART 1

TCLK (T2CON)	RCLK (T2CON)	TBCK_1 (BDRCON_1)	RBCK_1 (BDRCON_1)	Clock Source UART Tx_1	Clock Source UART Rx_1
0	0	0	0	Timer 1	Timer 1
1	0	0	0	Timer 2	Timer 1
0	1	0	0	Timer 1	Timer 2
1	1	0	0	Timer 2	Timer 2
X	0	1	0	INT_BRG_1	Timer 1
X	1	1	0	INT_BRG_1	Timer 2
0	X	0	1	Timer 1	INT_BRG_1
1	X	0	1	Timer 2	INT_BRG_1
X	X	1	1	INT_BRG_1	INT_BRG_1

Table 77. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1_0	**SMOD0_0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1_0	**Serial port Mode bit 1 for UART** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0_0	Serial port Mode bit 0 for UART Cleared to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Cleared to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Cleared by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

Table 104. Status in Slave Receiver Mode (Continued)

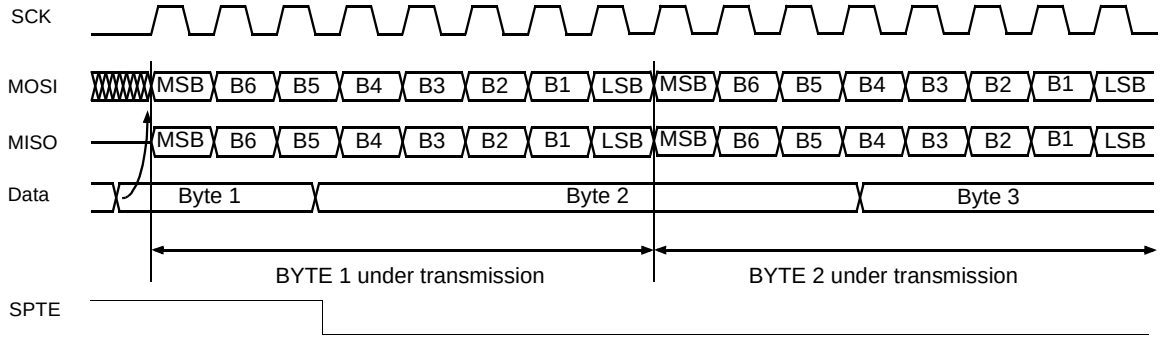
Status Code (SSCS)	Status of the 2-wire bus and 2-wire hardware	Application Software Response					Next Action Taken By 2-wire Software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
98h	Previously addressed with general call; data has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		Read data byte or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		Read data byte or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free
A0h	A STOP condition or repeated START condition has been received while still addressed as slave	No SSDAT action or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No SSDAT action or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		No SSDAT action or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free

When a transmission is in progress a new data can be queued and sent as soon as transmission has been completed. So it is possible to transmit bytes without latency, useful in some applications.

The SPTE bit in SPSCR is set as long as the transmission buffer is free. It means that the user application can write SPDAT with the data to be transmitted until the SPTE becomes cleared.

Figure 62 shows a queuing transmission in master mode. Once the Byte 1 is ready, it is immediately sent on the bus. Meanwhile an other byte is prepared (and the SPTE is cleared), it will be sent at the end of the current transmission. The next data must be ready before the end of the current transmission.

Figure 62. Queuing Transmission In Master Mode



In slave mode it is almost the same except it is the external master that start the transmission.

Also, in slave mode, if no new data is ready, the last value received will be the next data byte transmitted.

Power Monitor

The POR/PFD function monitors the internal power-supply of the CPU core memories and the peripherals, and if needed, suspends their activity when the internal power supply falls below a safety threshold. This is achieved by applying an internal reset to them.

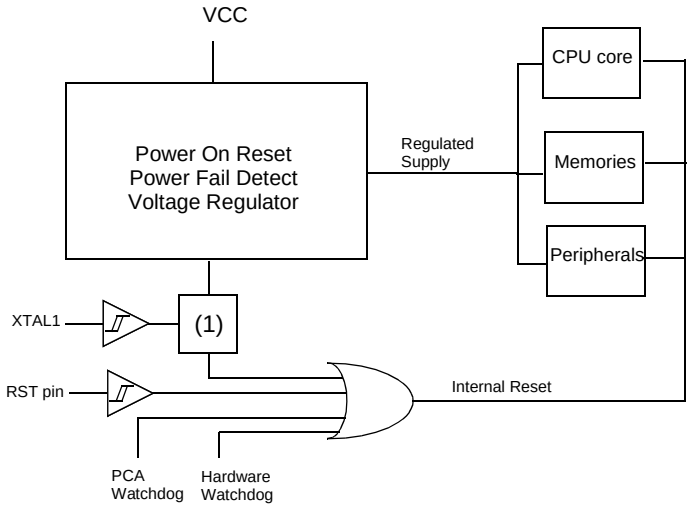
By generating the Reset the Power Monitor insures a correct start up when AT89C51RE2 is powered up.

Description

In order to startup and maintain the microcontroller in correct operating mode, V_{CC} has to be stabilized in the V_{CC} operating range and the oscillator has to be stabilized with a nominal amplitude compatible with logic level VIH/VIL.

These parameters are controlled during the three phases: power-up, normal operation and power going down. See Figure 66.

Figure 66. Power Monitor Block Diagram

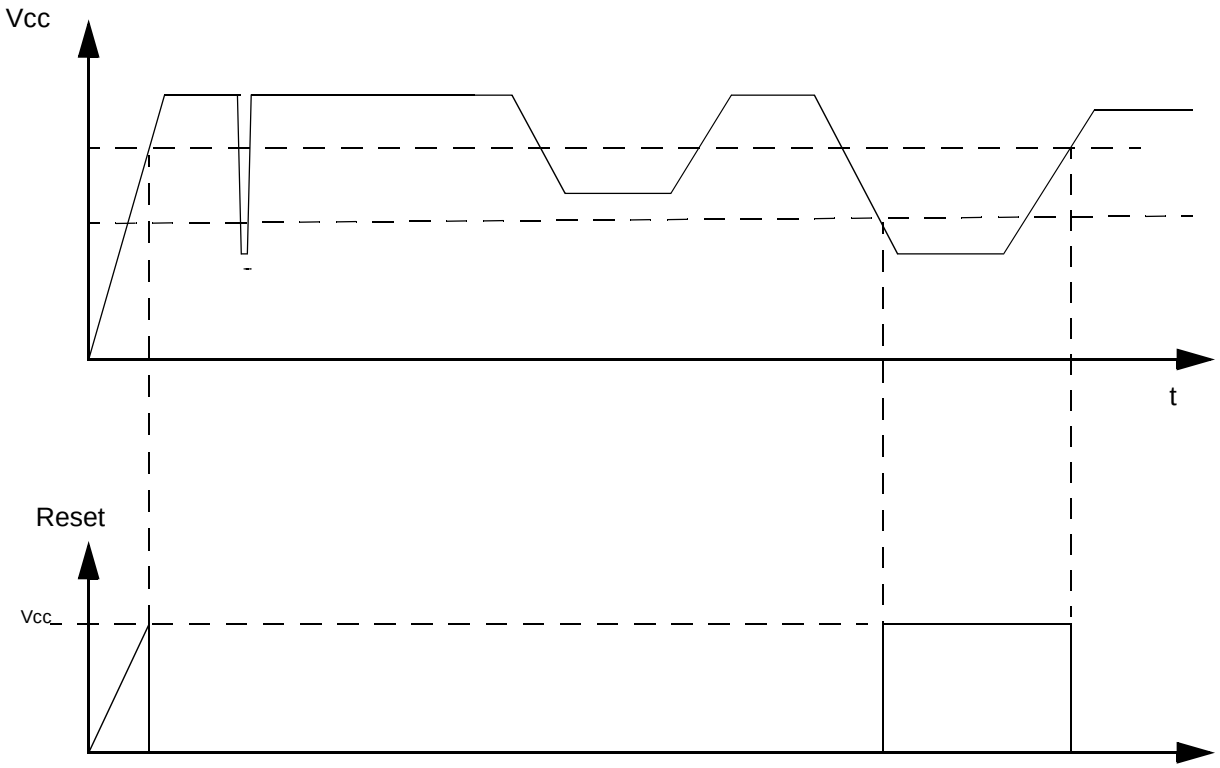


Note: 1. Once XTAL1 High and low levels reach above and below VIH/VIL. a 1024 clock period delay will extend the reset coming from the Power Fail Detect. If the power falls below the Power Fail Detect threshold level, the Reset will be applied immediately.

The Voltage regulator generates a regulated internal supply for the CPU core the memories and the peripherals. Spikes on the external Vcc are smoothed by the voltage regulator.

The Power fail detect monitor the supply generated by the voltage regulator and generate a reset if this supply falls below a safety threshold as illustrated in the Figure 67 below.

Figure 67. Power Fail Detect



When the power is applied, the Power Monitor immediately asserts a reset. Once the internal supply after the voltage regulator reach a safety level, the power monitor then looks at the XTAL clock input. The internal reset will remain asserted until the Xtal1 levels are above and below VIH and VIL. Further more. An internal counter will count 1024 clock periods before the reset is de-asserted.

If the internal power supply falls below a safety level, a reset is immediately asserted.

Power-off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (Table 118). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

Table 118. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Cleared to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Cleared to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Cleared by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Reset Output

As detailed in Section “Hardware Watchdog Timer”, page 124, the WDT generates a 96-clock period pulse on the RST pin. In order to properly propagate this pulse to the rest of the application in case of external capacitor or power-supply supervisor circuit, a 1 kΩ resistor must be added as shown Figure 70.

Figure 70. Recommended Reset Output Schematic

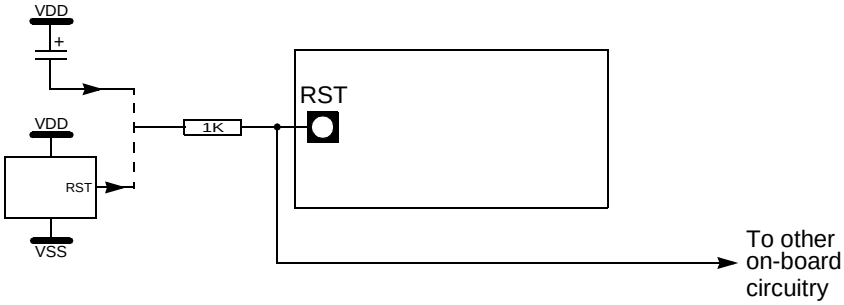


Table 121. AC Parameters for a Variable Clock

Symbol	Type	Standard Clock	X2 Clock	X parameter for -M(1) range	X parameter for -L(2) range	Units
T_{LHLL}	Min	2 T - x	T - x	15	15	ns
T_{AVLL}	Min	T - x	0.5 T - x	20	20	ns
T_{LLAX}	Min	T - x	0.5 T - x	20	20	ns
T_{LLIV}	Max	4 T - x	2 T - x	35	35	ns
T_{LLPL}	Min	T - x	0.5 T - x	15	15	ns
T_{PLPH}	Min	3 T - x	1.5 T - x	25	25	ns
T_{PLIV}	Max	3 T - x	1.5 T - x	45	45	ns
T_{PXIX}	Min	x	x	0	0	ns
T_{PXIZ}	Max	T - x	0.5 T - x	15	15	ns
T_{AVIV}	Max	5 T - x	2.5 T - x	45	45	ns
T_{PLAZ}	Max	x	x	10	10	ns

Notes: 1. ‘ -L ‘ refers to 2V - 5.5V version.
2. ‘ -M ’ refers to 4.5V to 5.5V version.

Document Revision History

Changes from 7663B to 7663C

1. Modified ordering information.
2. Various grammatical corections throughout document.

Changes from 7663C to 7663D

1. TWI interface added.

Changes from 7663D to 7663E

1. Removed 64 and 68 pins package product version.
2. Minor correction on Table 69 on page 102.