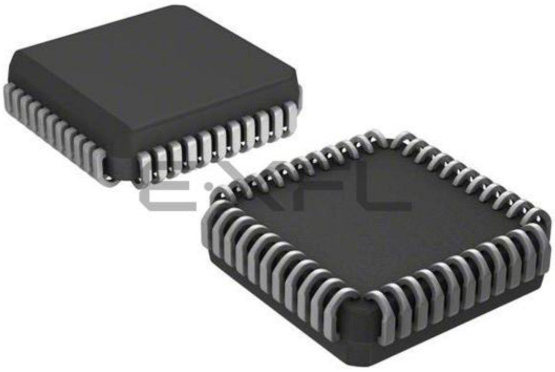

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51re2-slsum

SFR Mapping

The Special Function Registers (SFRs) of the AT89C51RE2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3, P4, P5, P6
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR_0, SADEN_0, SBUF_0, SCON_0, SADDR_1, SADEN_1, SBUF_1, SCON_1,
- PCA (Programmable Counter Array) registers: CCON, CCAPMx, CL, CH, CCAPxH, CCAPxL (x: 0 to 4)
- Power and clock control registers: PCON, CKAL, CKCON0_1
- Hardware Watchdog Timer registers: WDTRST, WDTPRG
- Interrupt system registers: IE0, IPL0, IPH0, IE1, IPL1, IPH1
- Keyboard Interface registers: KBE, KBF, KBLS
- 2-wire Interface registers: SSCON, SSCS, SSDAT, SSADR
- SPI registers: SPCON, SPSTR, SPDAT
- BRG (Baud Rate Generator) registers: BRL_0, BRL_1, BDRCON_0, BDRCON_1
- Memory register: FCON, FSTA
- Clock Prescaler register: CKRL
- Others: AUXR, AUXR1, CKCON0, CKCON1, BMSEL

Table 78. BDRCON_0 Register

BDRCON_0 - Baud Rate Control Register (9Bh)

7	6	5	4	3	2	1	0
-	-	-	BRR_0	TBCK_0	RBCK_0	SPD_0	SRC_0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	BRR_0	Baud Rate Run Control bit Cleared to stop the internal Baud Rate Generator. Set to start the internal Baud Rate Generator.
3	TBCK_0	Transmission Baud rate Generator Selection bit for UART Cleared to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
2	RBCK_0	Reception Baud Rate Generator Selection bit for UART Cleared to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
1	SPD_0	Baud Rate Speed Control bit for UART Cleared to select the SLOW Baud Rate Generator. Set to select the FAST Baud Rate Generator.
0	SRC_0	Baud Rate Source select bit in Mode 0 for UART Cleared to select $F_{OSC}/12$ as the Baud Rate Generator ($F_{CLK\ PERIPH}/6$ in X2 mode). Set to select the internal Baud Rate Generator for UARTs in mode 0.

Reset Value = XXX0 0000b
Not bit addressable

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, the serial interrupt flag is set again and a number of status code in SSCS are possible. There are 40h, 48h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA=logic 1). The appropriate action to be taken for each of these status code is detailed in Table . This scheme is repeated until a STOP condition is transmitted.

SSIE, CR2, CR1 and CR0 are not affected by the serial transfer and are referred to Table 7 to Table 11. After a repeated START condition (state 10h) the TWI module may switch to the master transmitter mode by loading SSDAT with SLA+W.

Slave Receiver Mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (Figure 54). To initiate the slave receiver mode, SSADR and SSCON must be loaded as follows:

Figure 53. Format and State in the Master Receiver Mode

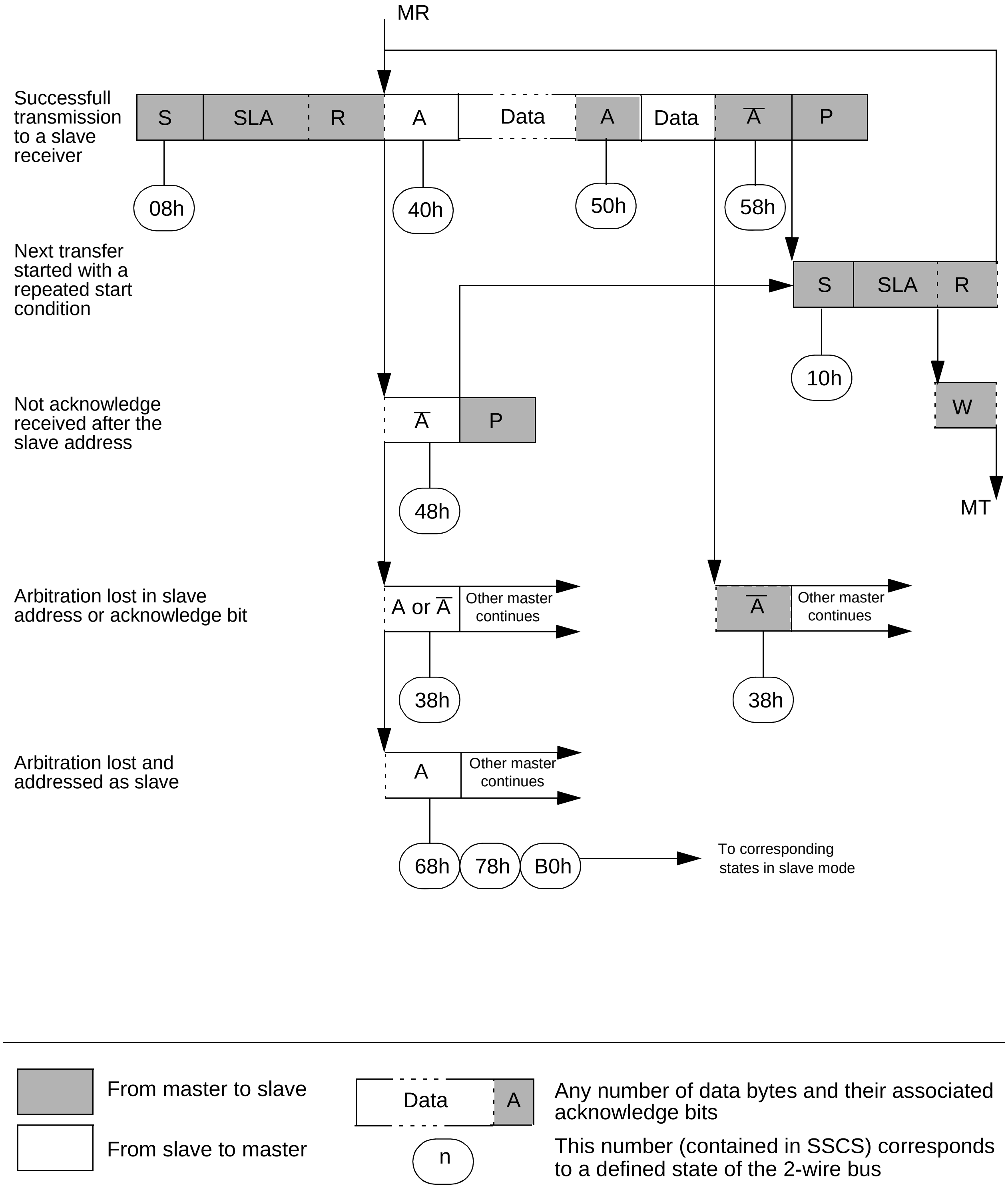
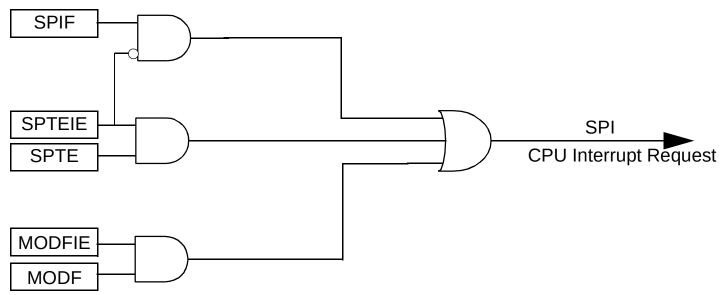


Figure 65. SPI Interrupt Requests Generation



Registers

Three registers in the SPI module provide control, status and data storage functions. These registers are describe in the following paragraphs.

Serial Peripheral Control Register (SPCON)

- The Serial Peripheral Control Register does the following:
- Selects one of the Master clock rates
- Configure the SPI Module as Master or Slave
- Selects serial clock polarity and phase
- Enables the SPI Module
- Frees the SS pin for a general-purpose

Table 115 describes this register and explains the use of each bit

Table 115. SPCON Register

SPCON - Serial Peripheral Control Register (0D4H)

7	6	5	4	3	2	1	0
SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0

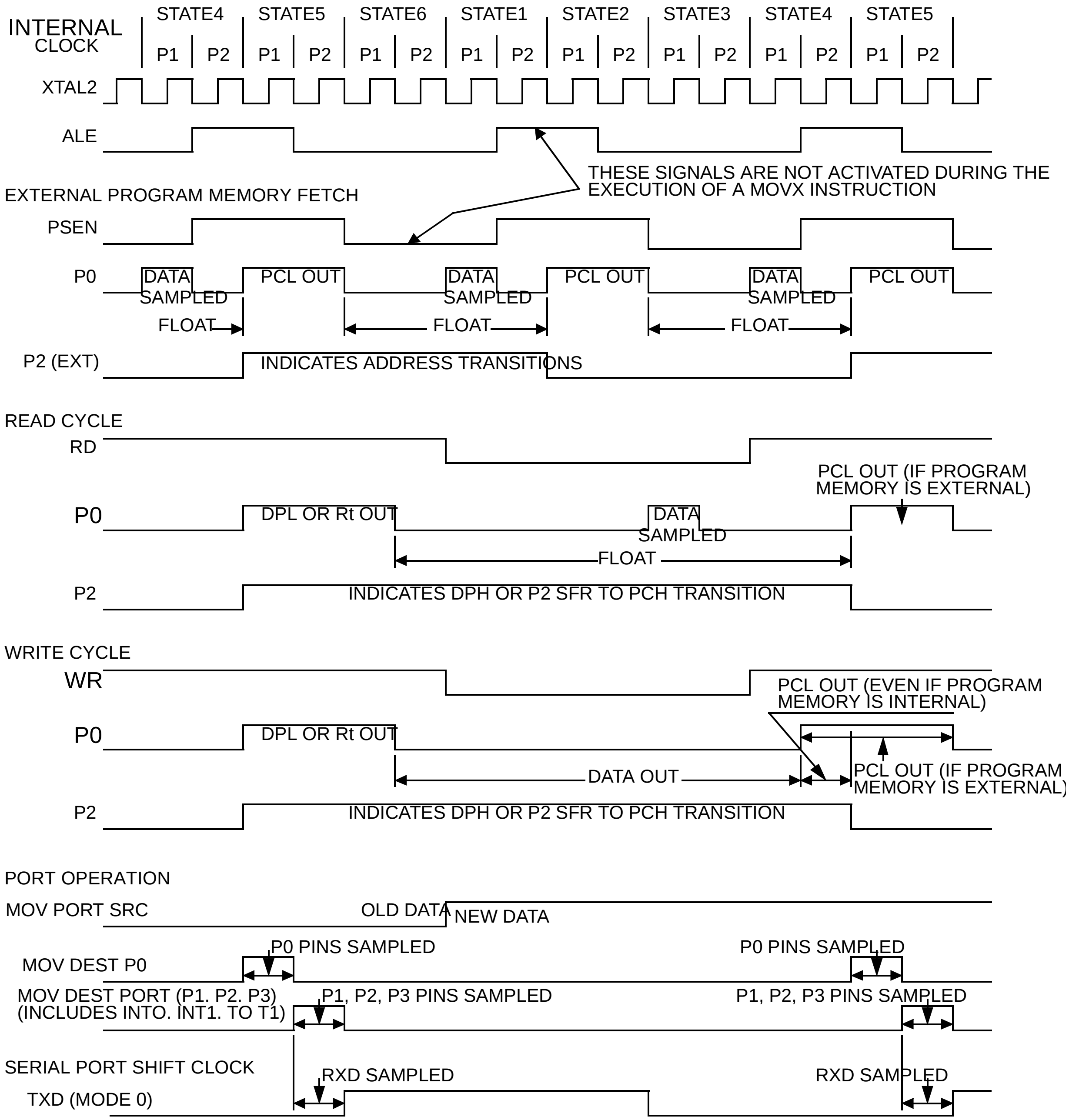
Bit Number	Bit Mnemonic	Description
7	SPR2	Serial Peripheral Rate 2 Bit with SPR1 and SPR0 define the clock rate (See bits SPR1 and SPR0 for detail).
6	SPEN	Serial Peripheral Enable Cleared to disable the SPI interface (internal reset of the SPI). Set to enable the SPI interface.
5	SSDIS	$\overline{SS}$ Disable Cleared to enable $\overline{SS}$ in both Master and Slave modes. Set to disable $\overline{SS}$ in both Master and Slave modes. In Slave mode, this bit has no effect if CPHA =’0’. When SSDIS is set, no MODF interrupt request is generated**.**
4	MSTR	Serial Peripheral Master Cleared to configure the SPI as a Slave. Set to configure the SPI as a Master.

For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 must be changed to XTAL2/2.

Figure 75. Internal Clock Signals



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Ordering Information

Table 130. Possible Order Entries

Part Number	Supply Voltage	Temperature Range	Package
AT89C51RE2-SLSUM	2.7V-5.5V	Industrial & Green	PLCC44
AT89C51RE2-RLTUM			VQFP44
AT89C51RE2-SLSEM	2.7V-5.5V	Engineering Samples	PLCC44
AT89C51RE2-RLTEM			VQFP44