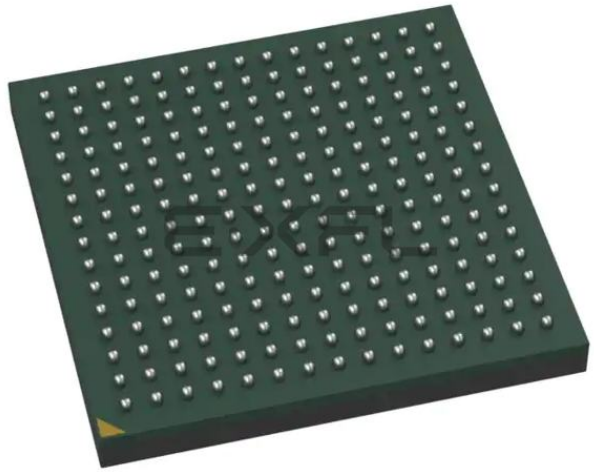

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM920T |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 100MHz |
| Co-Processors/DSP | - |
| RAM Controllers | SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | LCD |
| Ethernet | - |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 1.8V, 3.0V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | - |
| Package / Case | 225-LFBGA |
| Supplier Device Package | 225-MAPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mxscvp10 |

**Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | Primary | | | Alternate | | GPIO | | AIN | BIN | AOUT | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Signal | Dir | Pull-Up | Signal | Dir | Mux | Pull-Up | | | | |
| NVDD2 | B10 | LSCLK | O | | | | PD6 | 69K | | | | PD6 |
| NVDD3 | D10 | SPI1_MOSI | I/O | | | | PC17 | 69K | | | | PC17 |
| NVDD3 | E10 | SPI1_MISO | I/O | | | | PC16 | 69K | | | | PC16 |
| NVDD3 | B9 | SPI1_$\overline{SS}$ | I/O | | | | PC15 | 69K | | | | PC15 |
| NVDD3 | A10 | SPI1_SCLK | I/O | | | | PC14 | 69K | | | | PC14 |
| NVDD3 | A9 | SPI1_$\overline{SPI_RDY}$ | I/O | | | | PC13 | 69K | | | $\overline{DMA\_REQ}$ | PC13 |
| NVDD3 | E8 | UART1_RXD | I | | | | PC12 | 69K | | | | PC12 |
| NVDD3 | B8 | UART1_TXD | O | | | | PC11 | 69K | | | | PC11 |
| NVDD3 | C9 | $\overline{UART1\_RTS}$ | I | | | | PC10 | 69K | | | | PC10 |
| NVDD3 | E9 | $\overline{UART1\_CTS}$ | O | | | | PC9 | 69K | | | | PC9 |
| NVDD3 | A8 | SSI_TXCLK | I/O | | | | PC8 | 69K | | | | PC8 |
| NVDD3 | C8 | SSI_TXFS | I/O | | | | PC7 | 69K | | | | PC7 |
| NVDD3 | F9 | SSI_TXDAT | O | | | | PC6 | 69K | | | | PC6 |
| NVDD3 | B7 | SSI_RXDAT | I | | | | PC5 | 69K | | | | PC5 |
| NVDD3 | F8 | SSI_RXCLK | I | | | | PC4 | 69K | | | | PC4 |
| NVDD3 | A7 | SSI_RXFS | I | | | | PC3 | 69K | | | | PC3 |
| NVDD4 | C7 | UART2_RXD | I | | | | PB31 | 69K | | | | PB31 |
| NVDD4 | D8 | UART2_TXD | O | | | | PB30 | 69K | | | | PB30 |
| NVDD4 | E7 | $\overline{UART2\_RTS}$ | I | | | | PB29 | 69K | | | | PB29 |
| NVDD4 | F7 | $\overline{UART2\_CTS}$ | O | | | | PB28 | 69K | | | | PB28 |
| NVDD4 | B6 | USBD_VMO | O | | | | PB27 | 69K | | | | PB27 |
| NVDD4 | C6 | USBD_VPO | O | | | | PB26 | 69K | | | | PB26 |
| NVDD4 | A6 | USBD_VM | I | | | | PB25 | 69K | | | | PB25 |
| NVDD4 | D6 | USBD_VP | I | | | | PB24 | 69K | | | | PB24 |
| NVDD4 | A5 | USBD_SUSPND | O | | | | PB23 | 69K | | | | PB23 |

**Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | Primary | | | Alternate | | GPIO | | AIN | BIN | AOUT | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Signal | Dir | Pull-Up | Signal | Dir | Mux | Pull-Up | | | | |
| NVDD2 | H10 | NVDD2 | Static | | | | | | | | | |
| | G9 | NVSS | Static | | | | | | | | | |
| QVDD3 | F11 | QVDD3 | Static | | | | | | | | | |
| | G10 | QVSS | Static | | | | | | | | | |
| NVDD2 | C15 | NVDD2 | Static | | | | | | | | | |
| | H9 | NVSS | Static | | | | | | | | | |
| QVDD4 | D7 | QVDD4 | Static | | | | | | | | | |
| | L13 | QVSS | Static | | | | | | | | | |
| NVDD3 | D9 | NVDD3 | Static | | | | | | | | | |
| | J9 | NVSS | Static | | | | | | | | | |
| | K9 | NVSS | Static | | | | | | | | | |
| NVDD4 | G7 | NVDD4 | Static | | | | | | | | | |
| NVDD1 | F6 | NVDD1 | Static | | | | | | | | | |
| NVDD1 | L6 | NVDD1 | Static | | | | | | | | | |
| NVDD1 | M6 | NVDD1 | Static | | | | | | | | | |
| NVDD1 | K8 | NVDD1 | Static | | | | | | | | | |
| | L10 | NVSS | Static | | | | | | | | | |
| | L11 | NVSS | Static | | | | | | | | | |
| | M11 | NVSS | Static | | | | | | | | | |

1 Pull down this input with 1KΩ resistor to GND.

2 External circuit required to drive this input.

3 Tie this input high (to AVDD) or pull down with 1KΩ resistor to GND.

4 Pull up this output with a resistor to NVDD2.

## 4.2 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table, $T_{ref}$ is a reference clock period after the pre-divider and $T_{dck}$ is the output double clock period.

**Table 10. DPLL Specifications**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| DPLL input clock freq range | Vcc = 1.8V | 5 | – | 100 | MHz |
| Pre-divider output clock freq range | Vcc = 1.8V | 5 | – | 30 | MHz |
| DPLL output clock freq range | Vcc = 1.8V | 80 | – | 220 | MHz |
| Pre-divider factor (PD) | – | 1 | – | 16 | – |
| Total multiplication factor (MF) | Includes both integer and fractional parts | 5 | – | 15 | – |
| MF integer part | – | 5 | – | 15 | – |
| MF numerator | Should be less than the denominator | 0 | – | 1022 | – |
| MF denominator | – | 1 | – | 1023 | – |
| Pre-multiplier lock-in time | – | – | – | 312.5 | µsec |
| Freq lock-in time after full reset | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 250 | 280 (56 µs) | 300 | $T_{ref}$ |
| Freq lock-in time after partial reset | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 220 | 250 (50 µs) | 270 | $T_{ref}$ |
| Phase lock-in time after full reset | FPL mode and integer MF (does not include pre-multi lock-in time) | 300 | 350 (70 µs) | 400 | $T_{ref}$ |
| Phase lock-in time after partial reset | FPL mode and integer MF (does not include pre-multi lock-in time) | 270 | 320 (64 µs) | 370 | $T_{ref}$ |
| Freq jitter (p-p) | – | – | 0.005 (0.01%) | 0.01 | $2 \bullet T_{dck}$ |
| Phase jitter (p-p) | Integer MF, FPL mode, Vcc=1.8V | – | 1.0 (10%) | 1.5 | ns |
| Power supply voltage | – | 1.7 | – | 2.5 | V |
| Power dissipation | FOL mode, integer MF, $f_{dck}$ = 100 MHz, Vcc = 1.8V | – | – | 4 | mW |

## 4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4.

**NOTE**

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

### 4.4.2.2 WAIT Read Cycle DMA Enabled

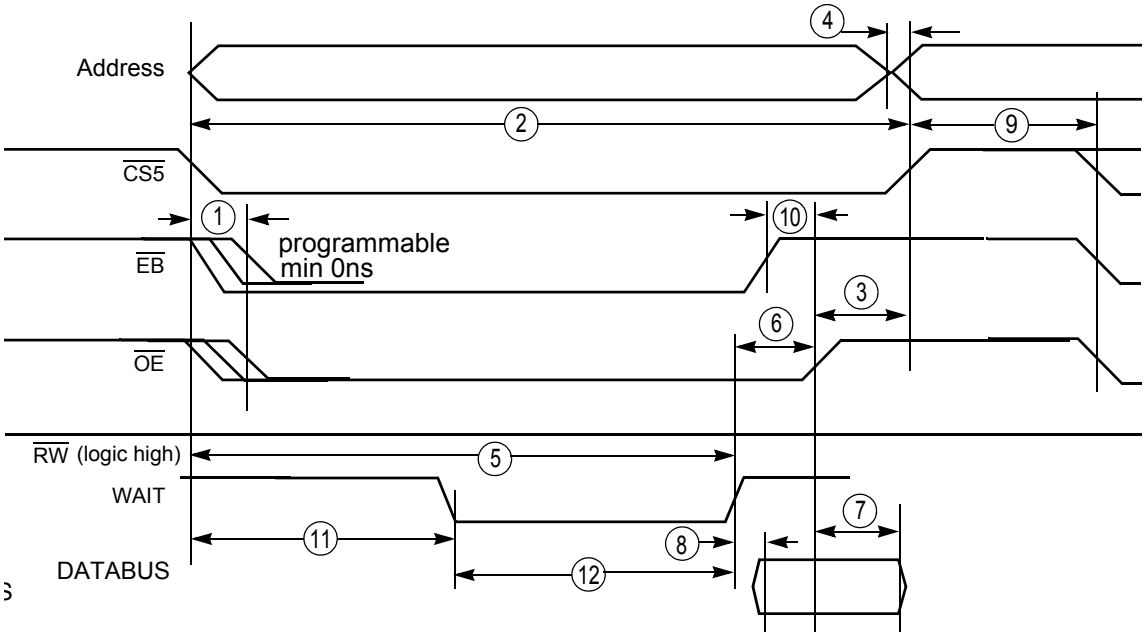
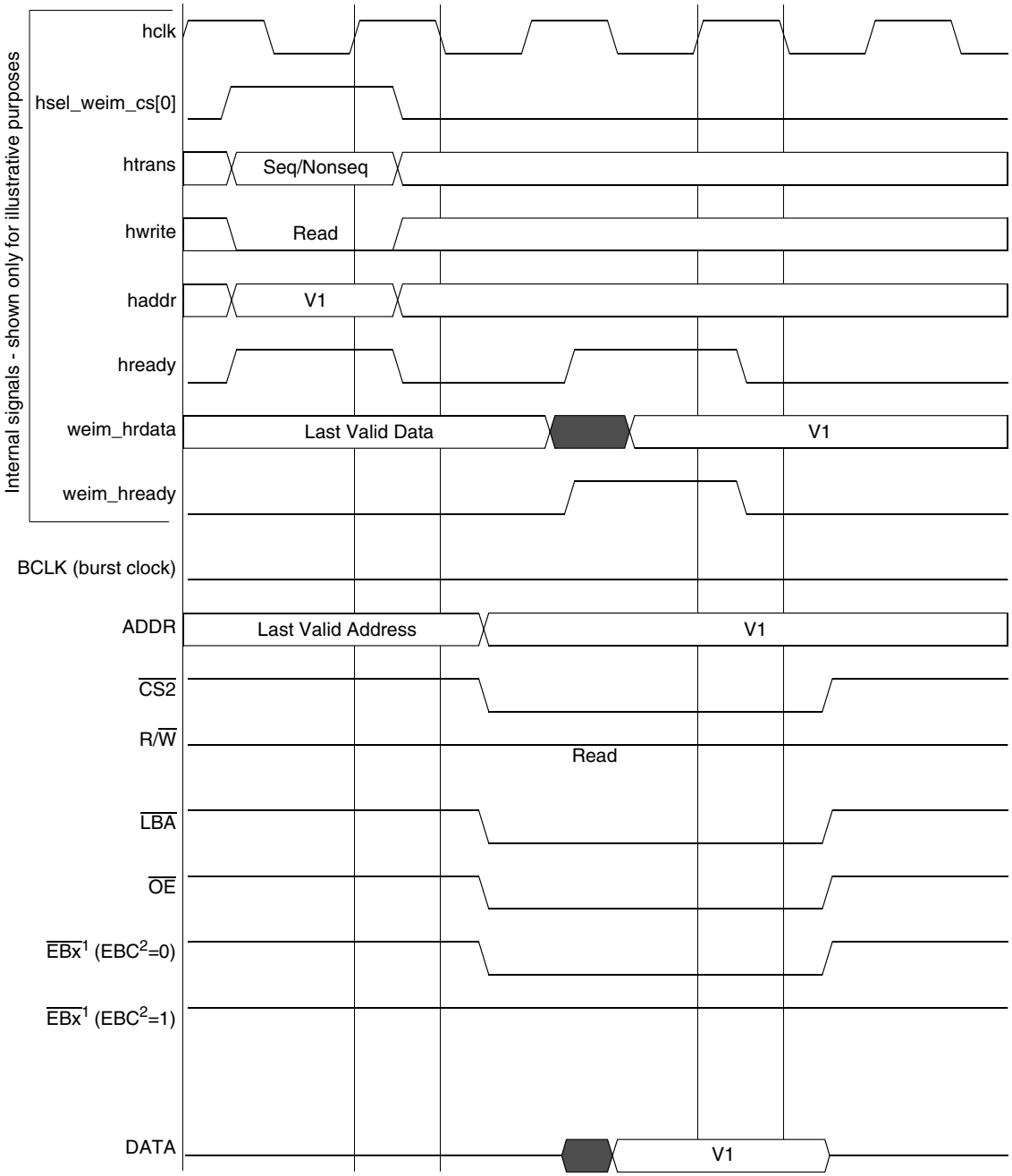



**Figure 7. DTACK WAIT Read Cycle DMA Enabled**

**Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz**

| Number | Characteristic | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $\overline{OE}$ and $\overline{EB}$ assertion time | See note 2 | – | ns |
| 2 | $\overline{CS}$ pulse width | 3T | – | ns |
| 3 | $\overline{OE}$ negated before $\overline{CS5}$ is negated | 1.5T-0.68 | 1.5T-0.06 | ns |
| 4 | Address inactived before $\overline{CS}$ negated | – | 0.05 | ns |
| 5 | Wait asserted after $\overline{CS5}$ asserted | – | 1020T | ns |
| 6 | Wait asserted to $\overline{OE}$ negated | 2T+1.57 | 3T+7.33 | ns |
| 7 | Data hold timing after $\overline{OE}$ negated | T-1.49 | – | ns |
| 8 | Data ready after wait is asserted | – | T | ns |
| 9 | $\overline{CS}$ deactive to next $\overline{CS}$ active | T | – | ns |
| 10 | OE negate after EB negate | 0.06 | 0.18 | ns |
| 11 | Wait becomes low after CS5 asserted | 0 | 1019T | ns |




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 10. WSC = 1, A.HALF/E.HALF**

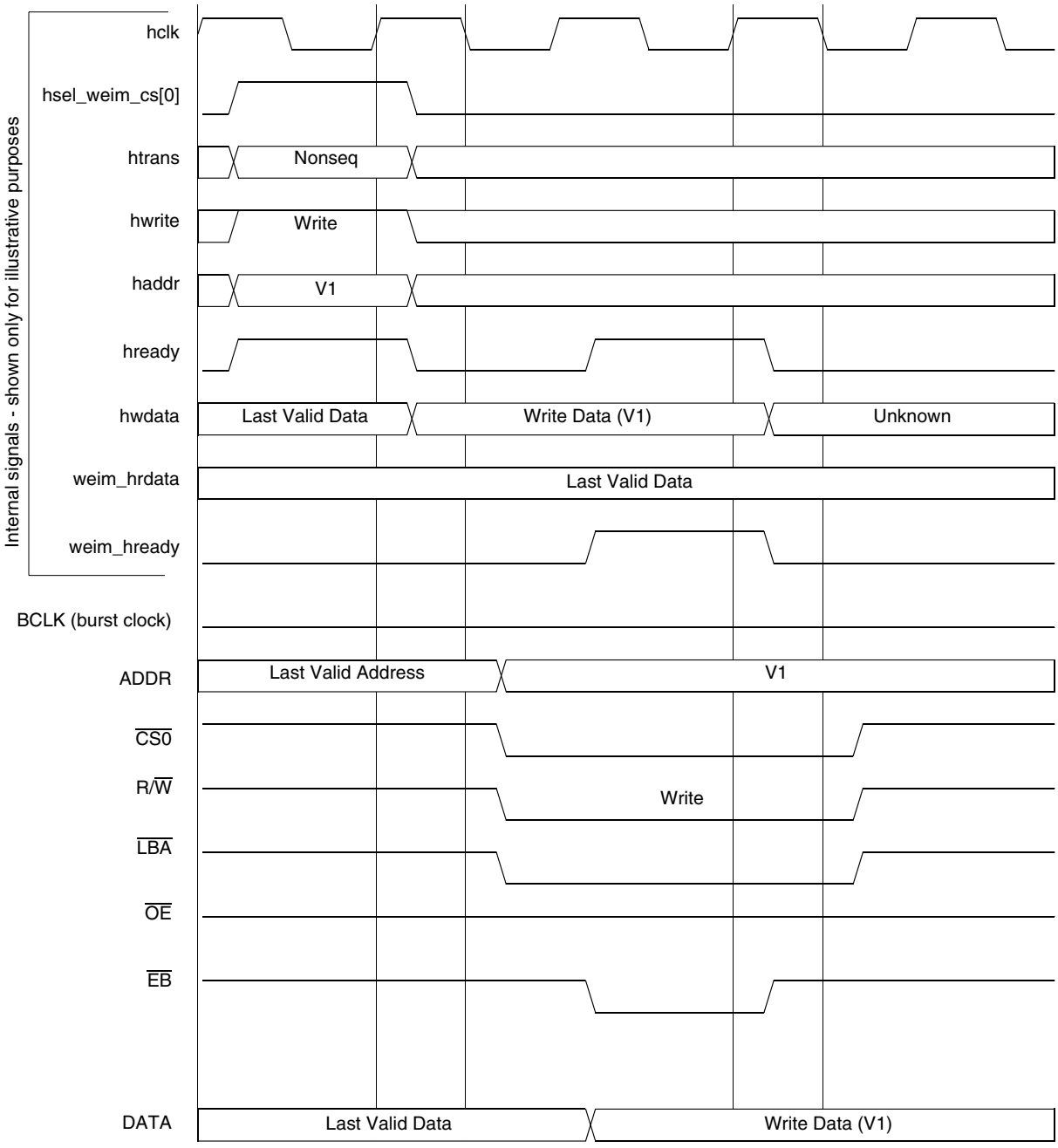
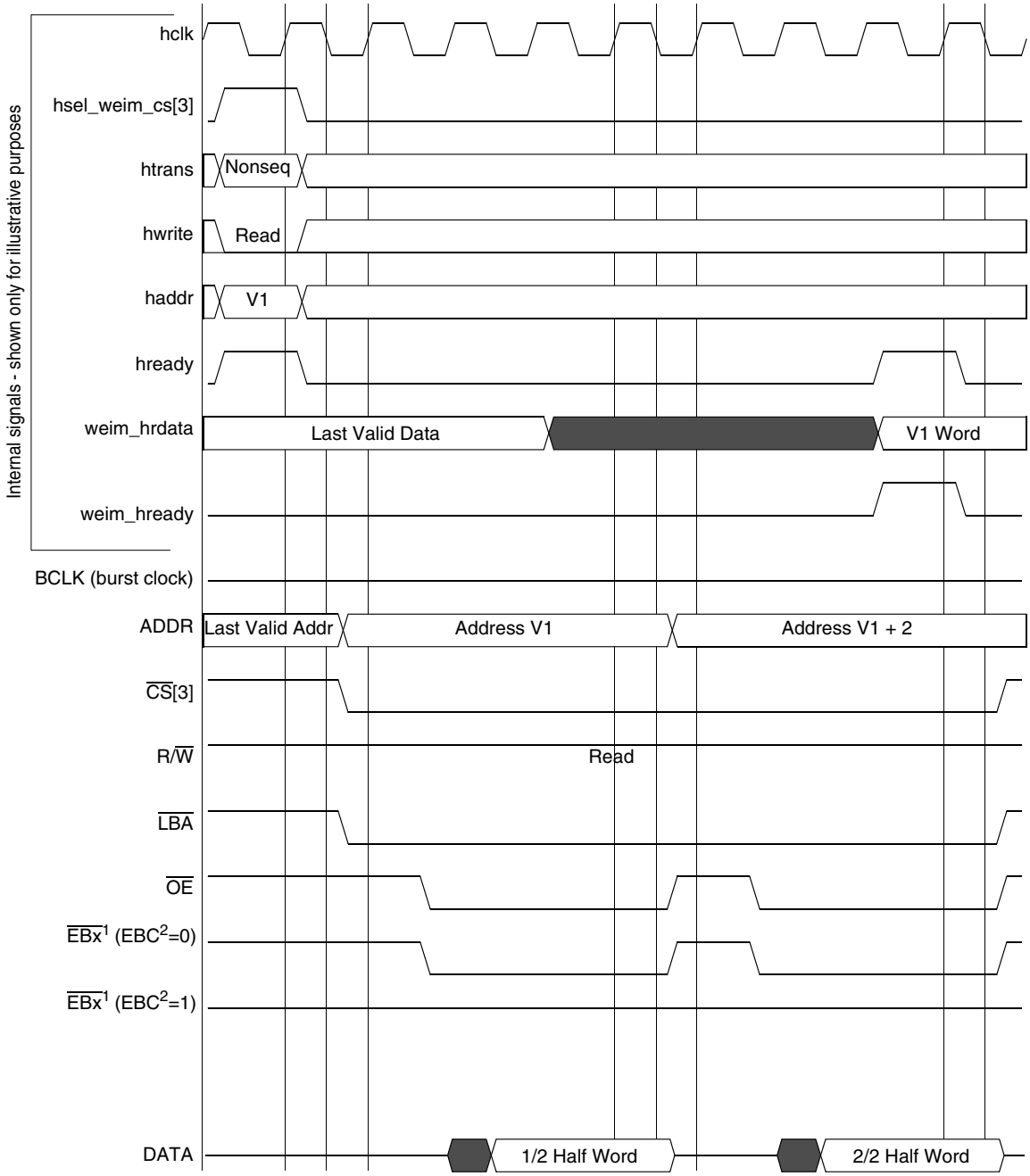



**Figure 11. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF**

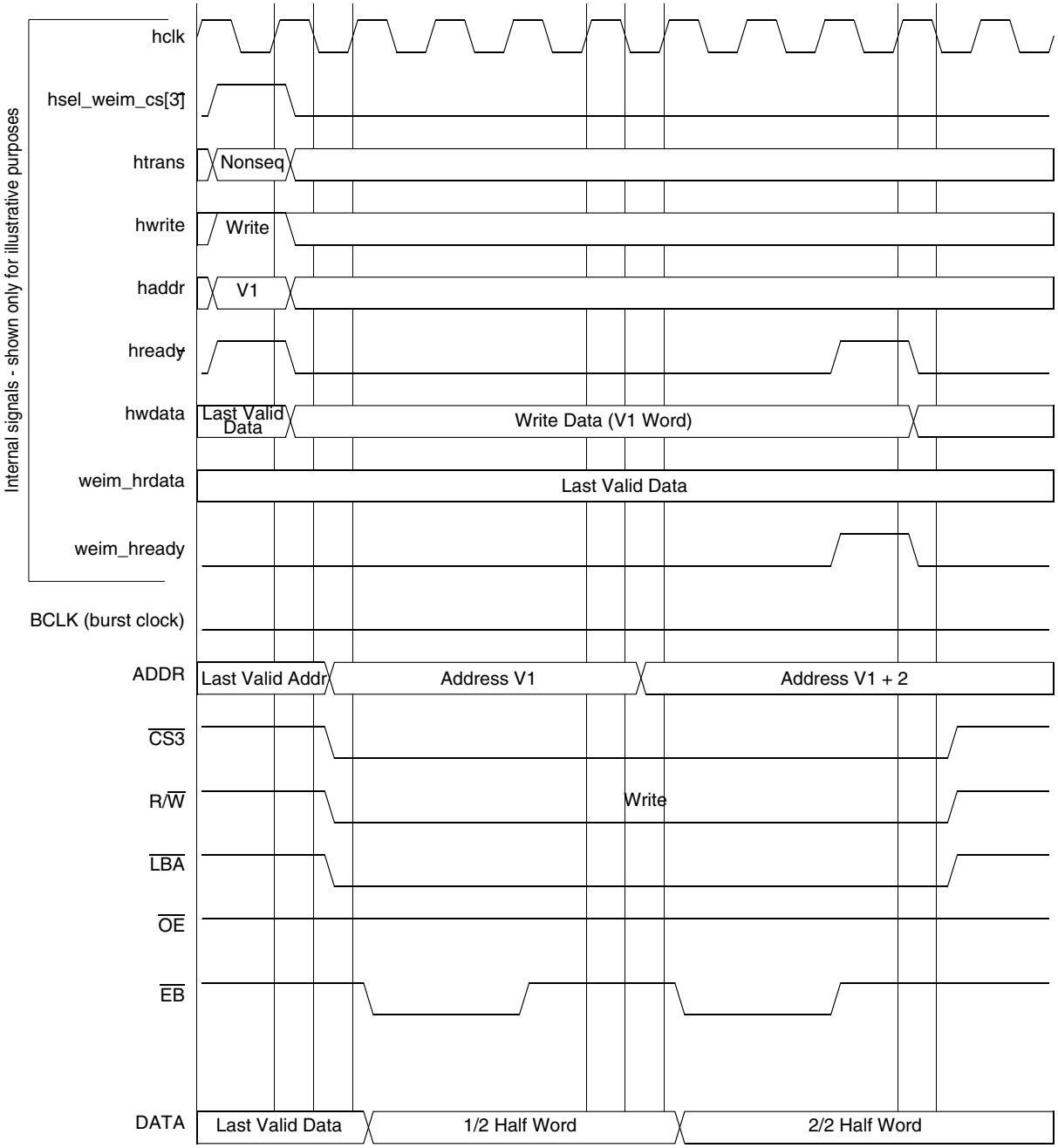
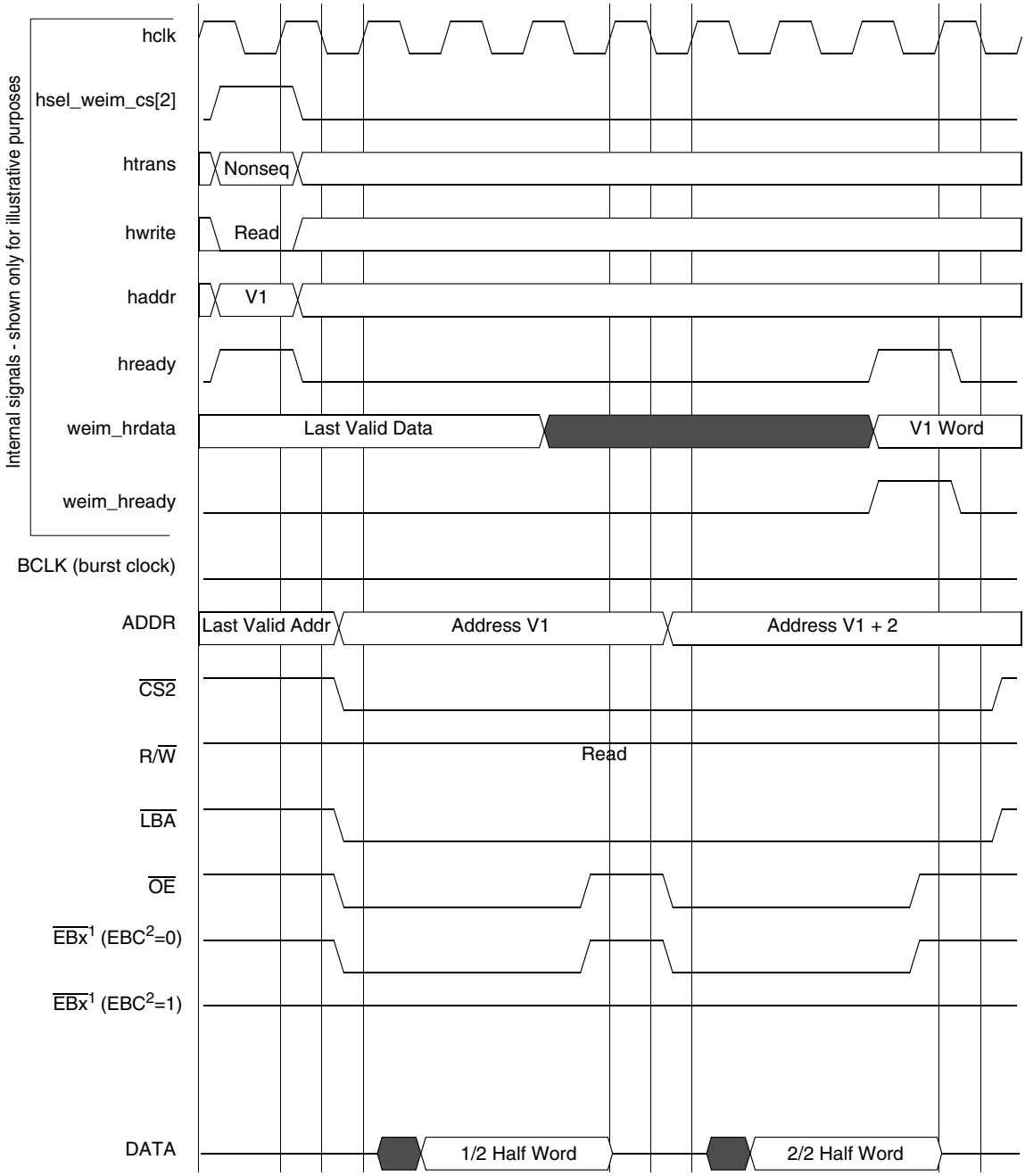
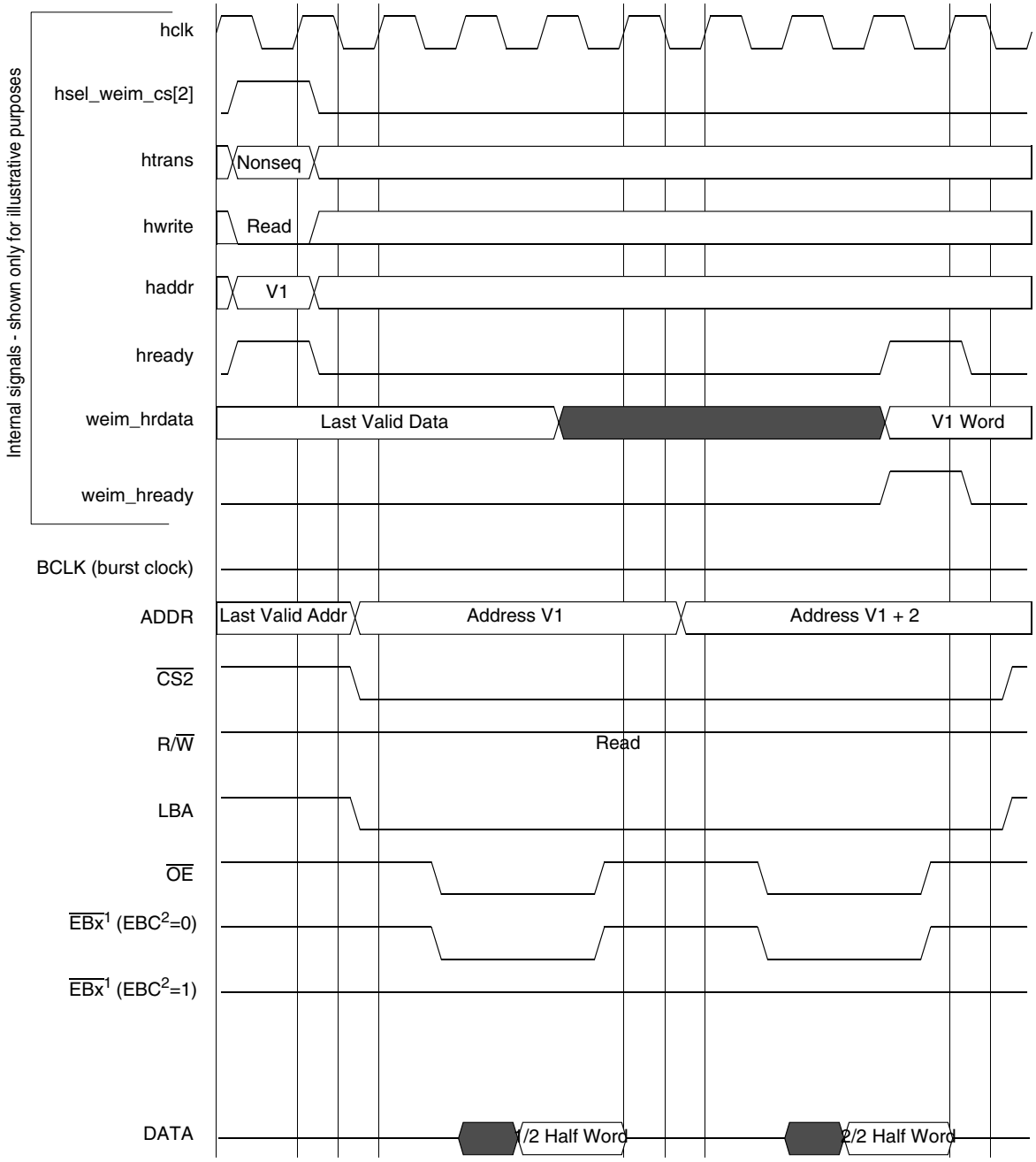



**Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF**

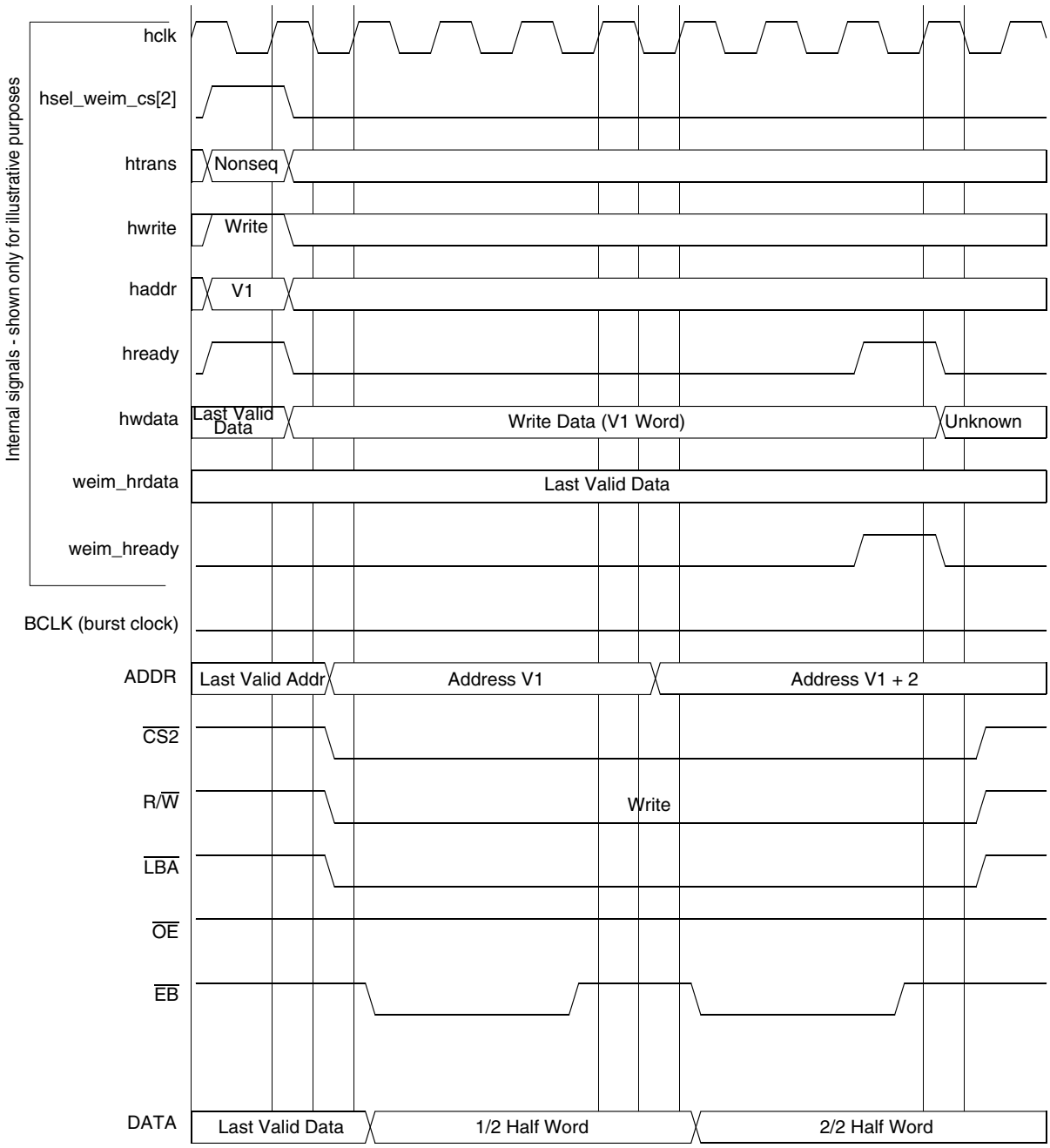
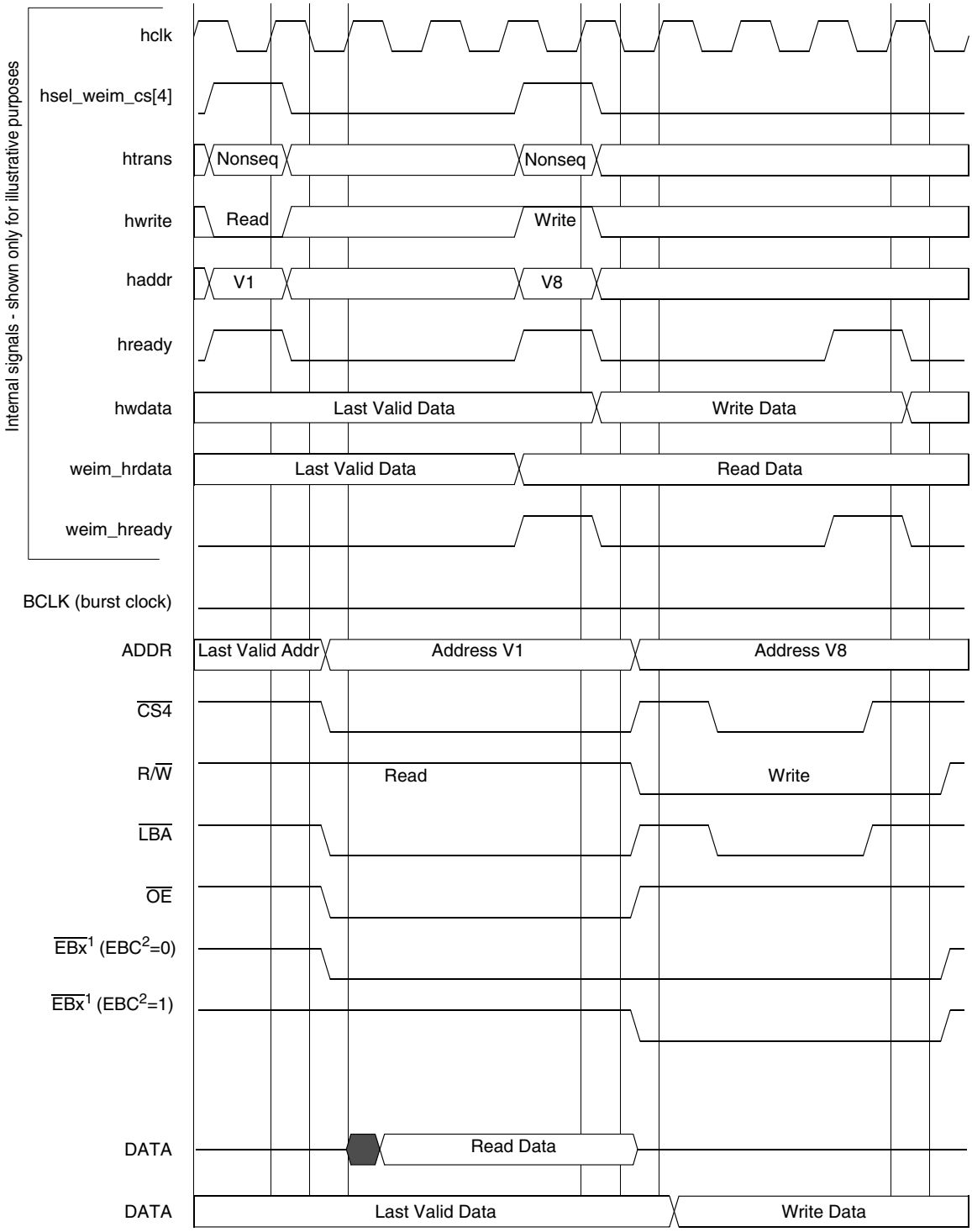
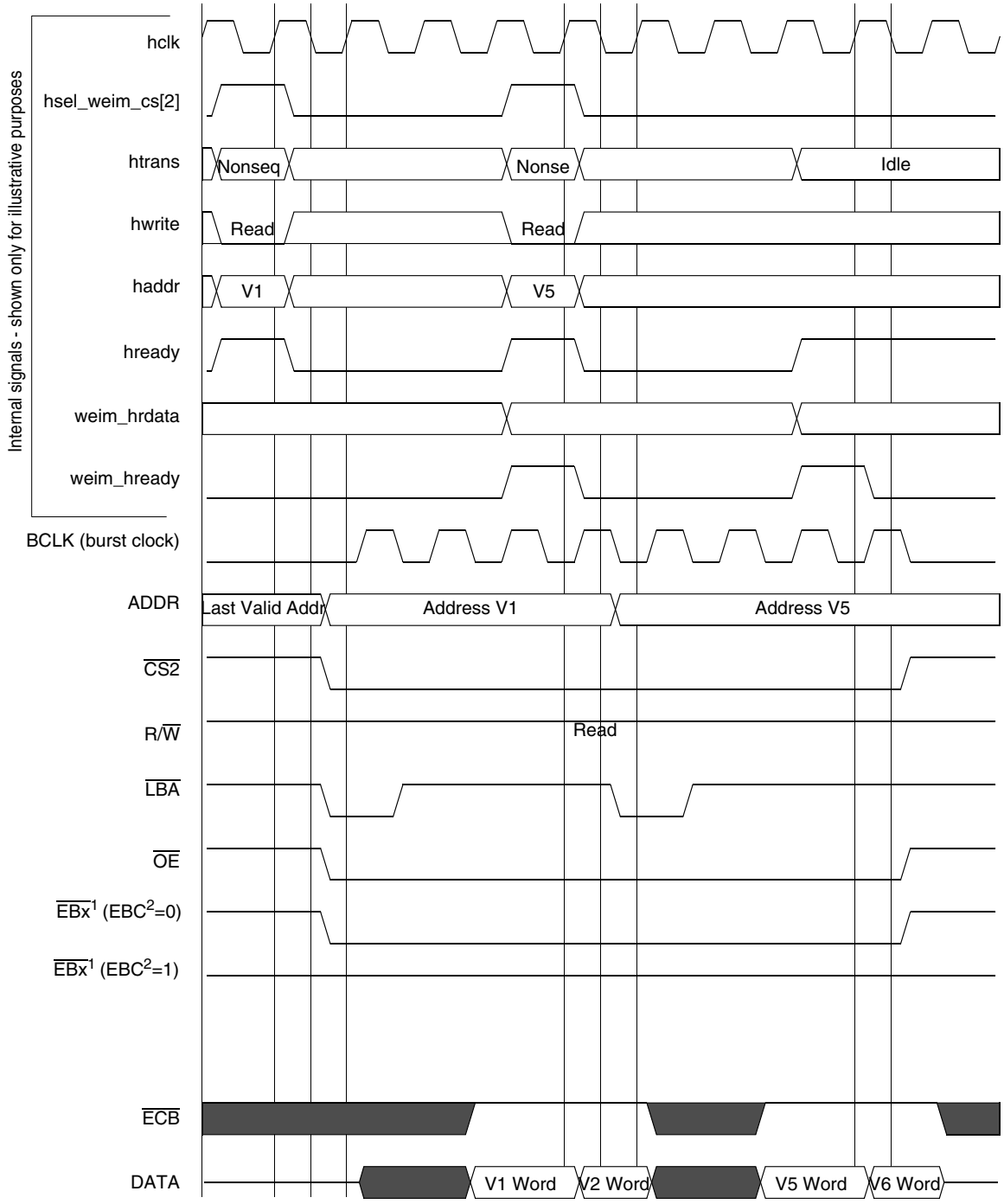



**Figure 21. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF**



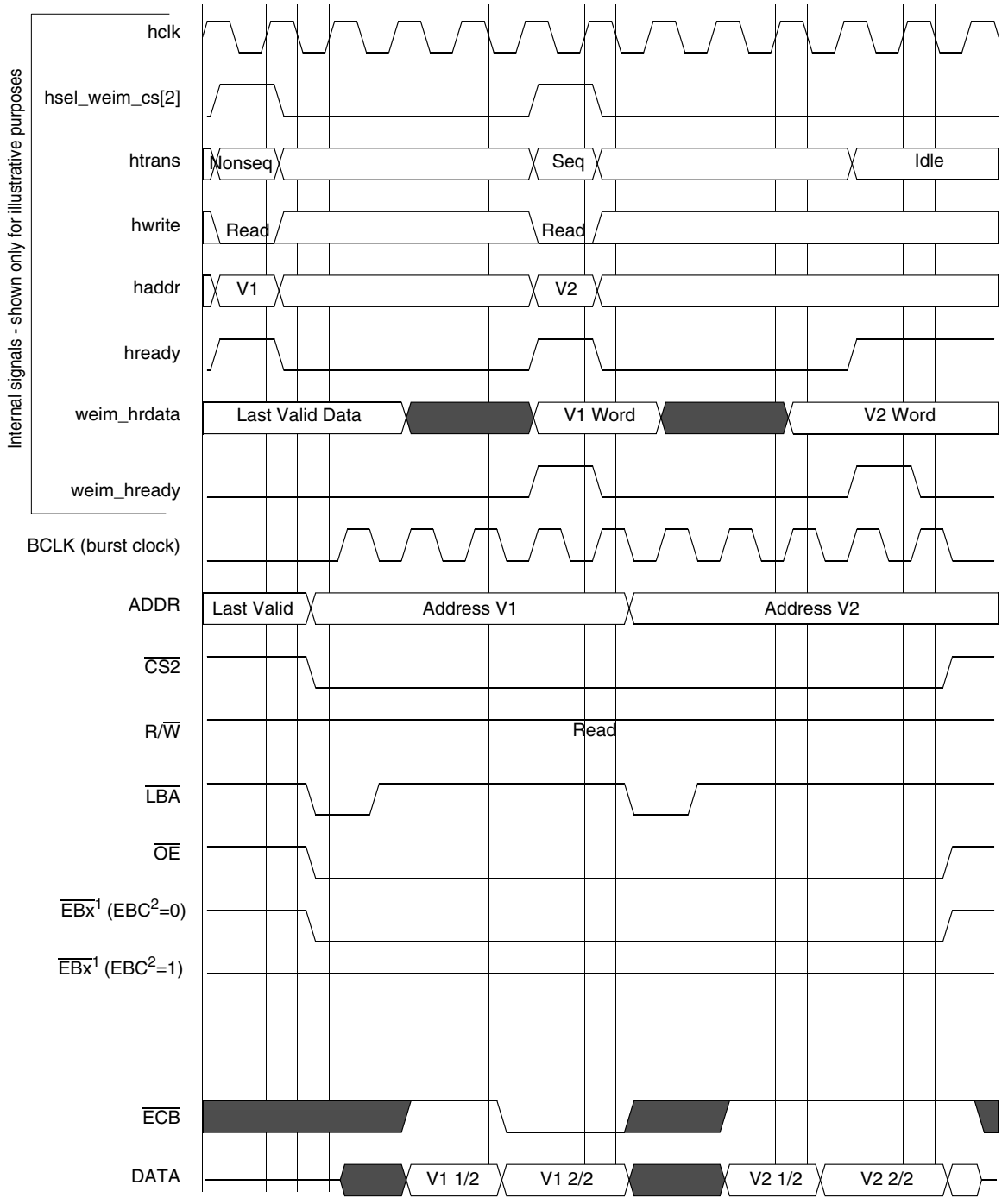

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 25. WSC = 3, CSA = 1, A.HALF/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 28. WSC = 3, SYNC = 1, A.HALF/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF**

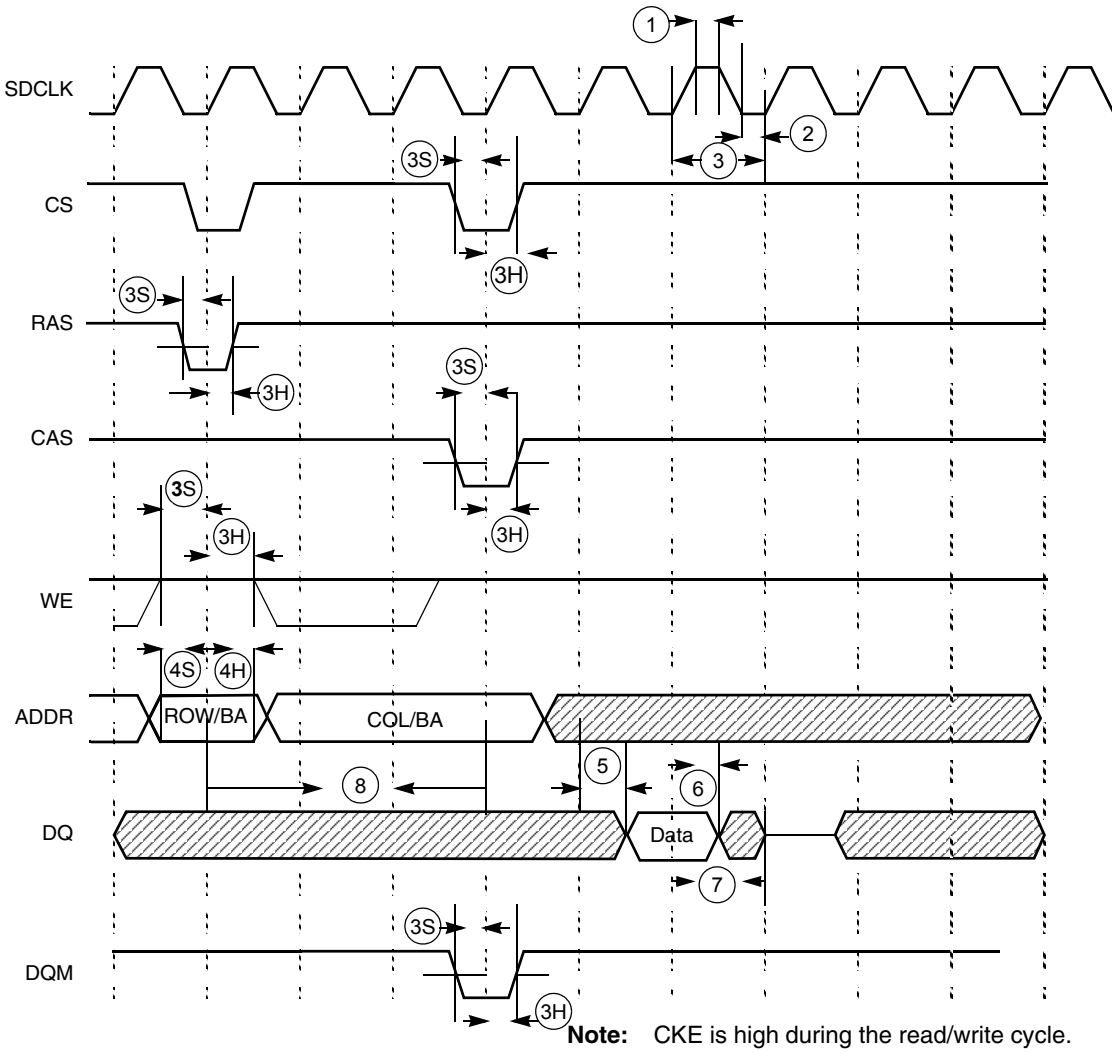
**Table 22. PWM Output Timing Parameter Table**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | System CLK frequency[1] | 0 | 87 | 0 | 100 | MHz |
| 2a | Clock high time[1] | 3.3 | – | 5/10 | – | ns |
| 2b | Clock low time[1] | 7.5 | – | 5/10 | – | ns |
| 3a | Clock fall time[1] | – | 5 | – | 5/10 | ns |
| 3b | Clock rise time[1] | – | 6.67 | – | 5/10 | ns |
| 4a | Output delay time[1] | 5.7 | – | 5 | – | ns |
| 4b | Output setup time[1] | 5.7 | – | 5 | – | ns |

1 $C_L$ of PWMO = 30 pF

## 4.8 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.




**Note:** CKE is high during the read/write cycle.

**Figure 43. SDRAM Read Cycle Timing Diagram**

**Table 23. SDRAM Read Timing Parameter Table**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | SDRAM clock high-level width | 2.67 | – | 4 | – | ns |
| 2 | SDRAM clock low-level width | 6 | – | 4 | – | ns |
| 3 | SDRAM clock cycle time | 11.4 | – | 10 | – | ns |
| 3S | CS, RAS, CAS, WE, DQM setup time | 3.42 | – | 3 | – | ns |
| 3H | CS, RAS, CAS, WE, DQM hold time | 2.28 | – | 2 | – | ns |
| 4S | Address setup time | 3.42 | – | 3 | – | ns |
| 4H | Address hold time | 2.28 | – | 2 | – | ns |
| 5 | SDRAM access time (CL = 3) | – | 6.84 | – | 6 | ns |

**Table 23. SDRAM Read Timing Parameter Table (Continued)**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 5 | SDRAM access time (CL = 2) | – | 6.84 | – | 6 | ns |
| 5 | SDRAM access time (CL = 1) | – | 22 | – | 22 | ns |
| 6 | Data out hold time | 2.85 | – | 2.5 | – | ns |
| 7 | Data out high-impedance time (CL = 3) | – | 6.84 | – | 6 | ns |
| 7 | Data out high-impedance time (CL = 2) | – | 6.84 | – | 6 | ns |
| 7 | Data out high-impedance time (CL = 1) | – | 22 | – | 22 | ns |
| 8 | Active to read/write command period (RC = 1) | $t_{RCD}$[1] | – | $t_{RCD1}$ | – | ns |

[1] $t_{RCD}$ = SDRAM clock cycle time. This settings can be found in the *MC9328MXS reference manual*.

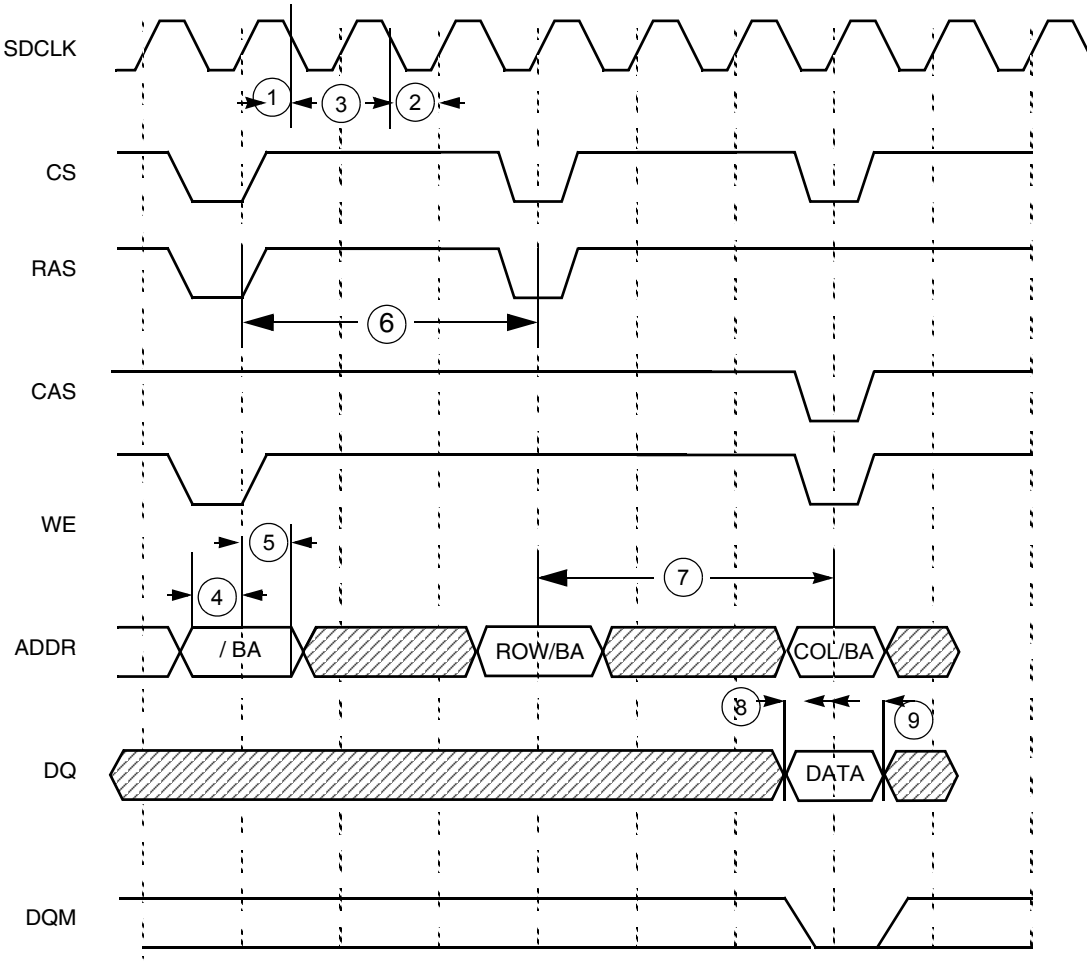



**Figure 44. SDRAM Write Cycle Timing Diagram**

**Table 29. SSI (Port C Primary Function) Timing Parameter Table (Continued)**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Synchronous External Clock Operation (Port C Primary Function[2])** | | | | | | |
| 33 | SRXD setup before STCK falling | 1.14 | – | 1.0 | – | ns |
| 34 | SRXD hold after STCK falling | 0 | – | 0 | – | ns |

1 All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

2 There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

3 bl = bit length; wl = word length.

**Table 30. SSI (Port B Alternate Function) Timing Parameter Table**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Internal Clock Operation[1] (Port B Alternate Function[2])** | | | | | | |
| 1 | STCK/SRCK clock period[1] | 95 | – | 83.3 | – | ns |
| 2 | STCK high to STFS (bl) high[3] | 1.7 | 4.8 | 1.5 | 4.2 | ns |
| 3 | SRCK high to SRFS (bl) high[3] | -0.1 | 1.0 | -0.1 | 1.0 | ns |
| 4 | STCK high to STFS (bl) low[3] | 3.08 | 5.24 | 2.7 | 4.6 | ns |
| 5 | SRCK high to SRFS (bl) low[3] | 1.25 | 2.28 | 1.1 | 2.0 | ns |
| 6 | STCK high to STFS (wl) high[3] | 1.71 | 4.79 | 1.5 | 4.2 | ns |
| 7 | SRCK high to SRFS (wl) high[3] | -0.1 | 1.0 | -0.1 | 1.0 | ns |
| 8 | STCK high to STFS (wl) low[3] | 3.08 | 5.24 | 2.7 | 4.6 | ns |
| 9 | SRCK high to SRFS (wl) low[3] | 1.25 | 2.28 | 1.1 | 2.0 | ns |
| 10 | STCK high to STXD valid from high impedance | 14.93 | 16.19 | 13.1 | 14.2 | ns |
| 11a | STCK high to STXD high | 1.25 | 3.42 | 1.1 | 3.0 | ns |
| 11b | STCK high to STXD low | 2.51 | 3.99 | 2.2 | 3.5 | ns |
| 12 | STCK high to STXD high impedance | 12.43 | 14.59 | 10.9 | 12.8 | ns |
| 13 | SRXD setup time before SRCK low | 20 | – | 17.5 | – | ns |
| 14 | SRXD hold time after SRCK low | 0 | – | 0 | – | ns |

# 5 Pin-Out and Package Information

Table 31 illustrates the package pin assignments for the 225-contact MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 8.

**Table 31. i.MXS 225 MAPBGA Pin Assignments**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | PB13 | PB15 | PB19 | USBD_ ROE | USBD_ SUSPND | USBD_VM | SSI_ RXFS | SSI_ TXCLK | SPI1_ SPI_ RDY | SPI1_ SCLK | REV | PS | LD2 | LD4 | LD5 | **A** |
| **B** | PB11 | PB12 | PB16 | USBD_ AFE | USBD_ RCV | USBD_ VMO | SSI_ RXDAT | UART1_ TXD | SPI1_SS | LSCLK | SPL_ SPR | LD0 | LD3 | LD6 | LD7 | **B** |
| **C** | D31 | PB8 | PB14 | PB18 | PB10 | USBD_ VPO | UART2_ RXD | SSI_ TXFS | UART1_ RTS | CONTRAST | FLM/VSYNC | LD8 | LD9 | LD12 | NVDD2 | **C** |
| **D** | A23 | A24 | PB9 | PB17 | NVDD1 | USBD_ VP | QVDD4 | UART2_ TXD | NVDD3 | SPI1_ MOSI | LP/HSYNC | LD1 | LD11 | TMR2OUT | LD13 | **D** |
| **E** | A21 | A22 | D30 | D29 | NVDD1 | QVSS | UART2_ RTS | UART1_ RXD | UART1_ CTS | SPI1_ MISO | ACD/OE | LD10 | TIN | PA4 | PA3 | **E** |
| **F** | A20 | A19 | D28 | D27 | NVDD1 | NVDD1 | UART2_ CTS | SSI_ RXCLK | SSI_ TXDAT | CLS | QVDD3 | LD14 | LD15 | PA6 | PA8 | **F** |
| **G** | A17 | A18 | D26 | D25 | NVDD1 | NVSS | NVDD4 | NVSS | NVSS | QVSS | PWMO | PA7 | PA11 | PA13 | PA9 | **G** |
| **H** | A15 | A16 | D23 | D24 | D22 | NVSS | NVSS | NVSS | NVSS | NVDD2 | PA5 | PA12 | PA14 | I2C_SDA | TMS | **H** |
| **J** | A14 | A12 | D21 | D20 | NVDD1 | NVSS | NVSS | QVDD1 | NVSS | PA10 | I2C_SCL | TCK | TDO | BOOT1 | BOOT0 | **J** |
| **K** | A13 | A11 | CS2 | D19 | NVDD1 | NVSS | QVSS | NVDD1 | NVSS | D1 | BOOT2 | TDI | BIG_ ENDIAN | RESET_ OUT | XTAL32K | **K** |
| **L** | A10 | A9 | D17 | D18 | NVDD1 | NVDD1 | CS5 | D2 | ECB | NVSS | NVSS | POR | QVSS | XTAL16M | EXTAL32K | **L** |
| **M** | D16 | D15 | D13 | D10 | EB3 | NVDD1 | CS4 | CS1 | BCLK[1] | RW | NVSS | BOOT3 | QVDD2 | RESET_IN | EXTAL16M | **M** |
| **N** | A8 | A7 | D12 | EB0 | D9 | D8 | CS3 | CS0 | PA17 | D0 | DQM2 | DQM0 | SDCKE0 | TRISTATE | TRST | **N** |
| **P** | D14 | A5 | A4 | A3 | A2 | A1 | D6 | D5 | MA10 | MA11 | DQM1 | RAS | SDCKE1 | CLKO | RESET_SF[2] | **P** |
| **R** | A6 | D11 | EB1 | EB2 | OE | D7 | A0 | SDCLK | D4 | LBA | D3 | DQM3 | CAS | SDWE | AVDD1 | **R** |
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | |

1 Burst Clock

2 This signal is not used and should be floated in an actual application.

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