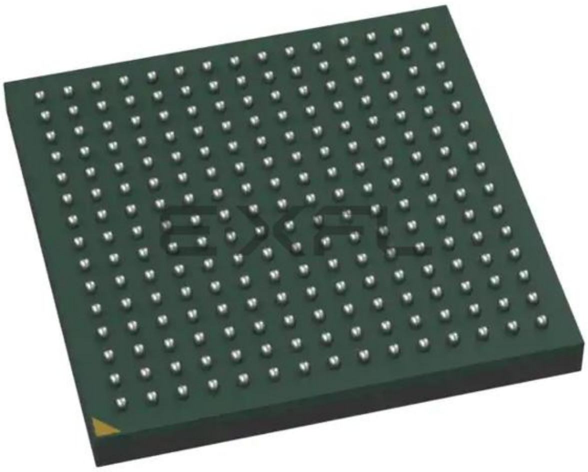

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	225-LFBGA
Supplier Device Package	225-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mxscvp10r2

- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 225-contact MAPBGA Package

1.2 Target Applications

The i.MXS applications processor is designed to meet the needs of medical instrumentation, low-end PDAs, point-of-sale terminals, security systems and other applications requiring a basic device based on ARM technology with support for open operating systems. Like other members of the i.MX family, the i.MXS is designed for high performance and low-power to maximize battery life.

1.3 Ordering Information

Table 1 provides ordering information.

Table 1. i.MXS Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
225-contact MAPBGA	100 MHz	0^{o}C to 70^{o}C	Pb-free	MC9328MXSVP10(R2)
		-40^{o}C to 85^{o}C	Pb-free	MC9328MXSCVP10(R2)

1.4 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - — *Active low* signals change from logic level one to logic level zero.
  - — *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - — *Active low* signals change from logic level zero to logic level one.
  - — *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	P5	A2	O									
NVDD1	M5	$\overline{EB3}$	O									
NVDD1	N6	D8	I/O	69K								
NVDD1	R5	$\overline{OE}$	O									
NVDD1	P6	A1	O									
NVDD1	L7	$\overline{CS5}$	O				PA23	69K				PA23
NVDD1	R6	D7	I/O	69K								
NVDD1	M7	$\overline{CS4}$	O				PA22	69K				PA22
NVDD1	R7	A0	O				PA21	69K				A0
NVDD1	N7	$\overline{CS3}$	O		$\overline{CSD1}$							$\overline{CSD1}$
NVDD1	P7	D6	I/O	69K								
NVDD1	K3	$\overline{CS2}$	O		$\overline{CSD0}$							$\overline{CSD0}$
NVDD1	R8	SDCLK	O									
NVDD1	M8	$\overline{CS1}$	O									
NVDD1	N8	$\overline{CS0}$	O									
NVDD1	P8	D5	I/O	69K								
NVDD1	L9	$\overline{ECB}$	I		ETMTRACEPKT7		PA20	69K				$\overline{ECB}$
NVDD1	R9	D4	I/O	69K								
NVDD1	R10	$\overline{LBA}$	O		ETMTRACEPKT6		PA19	69K				$\overline{LBA}$
NVDD1	R11	D3	I/O	69K								
NVDD1	M9	BCLK			ETMTRACEPKT5		PA18	69K				BCLK
NVDD1	L8	D2	I/O	69K								
NVDD1	N9	PA17			ETMTRACEPKT4		PA17	69K	Reserved		$\overline{DTACK}$	PA17
NVDD1	K10	D1	I/O	69K								
NVDD1	M10	$\overline{RW}$										
NVDD1	P10	MA11	O									
NVDD1	P9	MA10	O									
NVDD1	N10	D0	I/O	69K								
NVDD1	R12	DQM3	O									
NVDD1	N11	DQM2	O									
NVDD1	P11	DQM1	O									
NVDD1	N12	DQM0	O									
NVDD1	P12	$\overline{RAS}$	O									
NVDD1	R13	$\overline{CAS}$	O									
NVDD1	R14	$\overline{SDWE}$	O									

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	N13	SDCKE0	O									
NVDD1	P13	SDCKE1	O									
NVDD1	P15	$\overline{\mathrm{RESET\_SF}}$	O									
NVDD1	P14	CLKO	O									
AVDD1	R15	AVDD1	Static									
QVDD2	M13	QVDD2	Static									
AVDD1	N15	$\overline{\mathrm{TRST}}$	I	69K								
AVDD1	N14	TRISTATE[1]	I									
AVDD1	M15	EXTAL16M	I									
AVDD1	L14	XTAL16M	O									
AVDD1	L15	EXTAL32K	I									
AVDD1	K15	XTAL32K	O									
AVDD1	M14	$\overline{\mathrm{RESET\_IN}}$[2]	I	69K								
AVDD1	K14	$\overline{\mathrm{RESET\_OUT}}$	O									
AVDD1	L12	POR[2]	I									
AVDD1	K13	BIG_ENDIAN[3]	I									
AVDD1	M12	BOOT3[3]	I									
AVDD1	K11	BOOT2[3]	I									
AVDD1	J14	BOOT1[3]	I									
AVDD1	J15	BOOT0[3]	I									
NVDD2	J13	$\overline{\mathrm{TDO}}$[4]	O									
NVDD2	H15	TMS	I	69K								
NVDD2	J12	TCK	I	69K								
NVDD2	K12	TDI	I	69K								
NVDD2	J11	I2C_SCL	O				PA16	69K				PA16
NVDD2	H14	I2C_SDA	I/O				PA15	69K				PA15
NVDD2	H13	Reserved	I				PA14	69K				PA14
NVDD2	G14	Reserved	I				PA13	69K				PA13
NVDD2	H12	Reserved	I				PA12	69K				PA12
NVDD2	G13	Reserved	I				PA11	69K				PA11
NVDD2	J10	Reserved	I				PA10	69K				PA10
NVDD2	G15	Reserved	I				PA9	69K				PA9

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull -Up				
NVDD2	H10	NVDD2	Static									
	G9	NVSS	Static									
QVDD3	F11	QVDD3	Static									
	G10	QVSS	Static									
NVDD2	C15	NVDD2	Static									
	H9	NVSS	Static									
QVDD4	D7	QVDD4	Static									
	L13	QVSS	Static									
NVDD3	D9	NVDD3	Static									
	J9	NVSS	Static									
	K9	NVSS	Static									
NVDD4	G7	NVDD4	Static									
NVDD1	F6	NVDD1	Static									
NVDD1	L6	NVDD1	Static									
NVDD1	M6	NVDD1	Static									
NVDD1	K8	NVDD1	Static									
	L10	NVSS	Static									
	L11	NVSS	Static									
	M11	NVSS	Static									

[1] Pull down this input with 1KΩ resistor to GND.

[2] External circuit required to drive this input.

[3] Tie this input high (to AVDD) or pull down with 1KΩ resistor to GND.

[4] Pull up this output with a resistor to NVDD2.

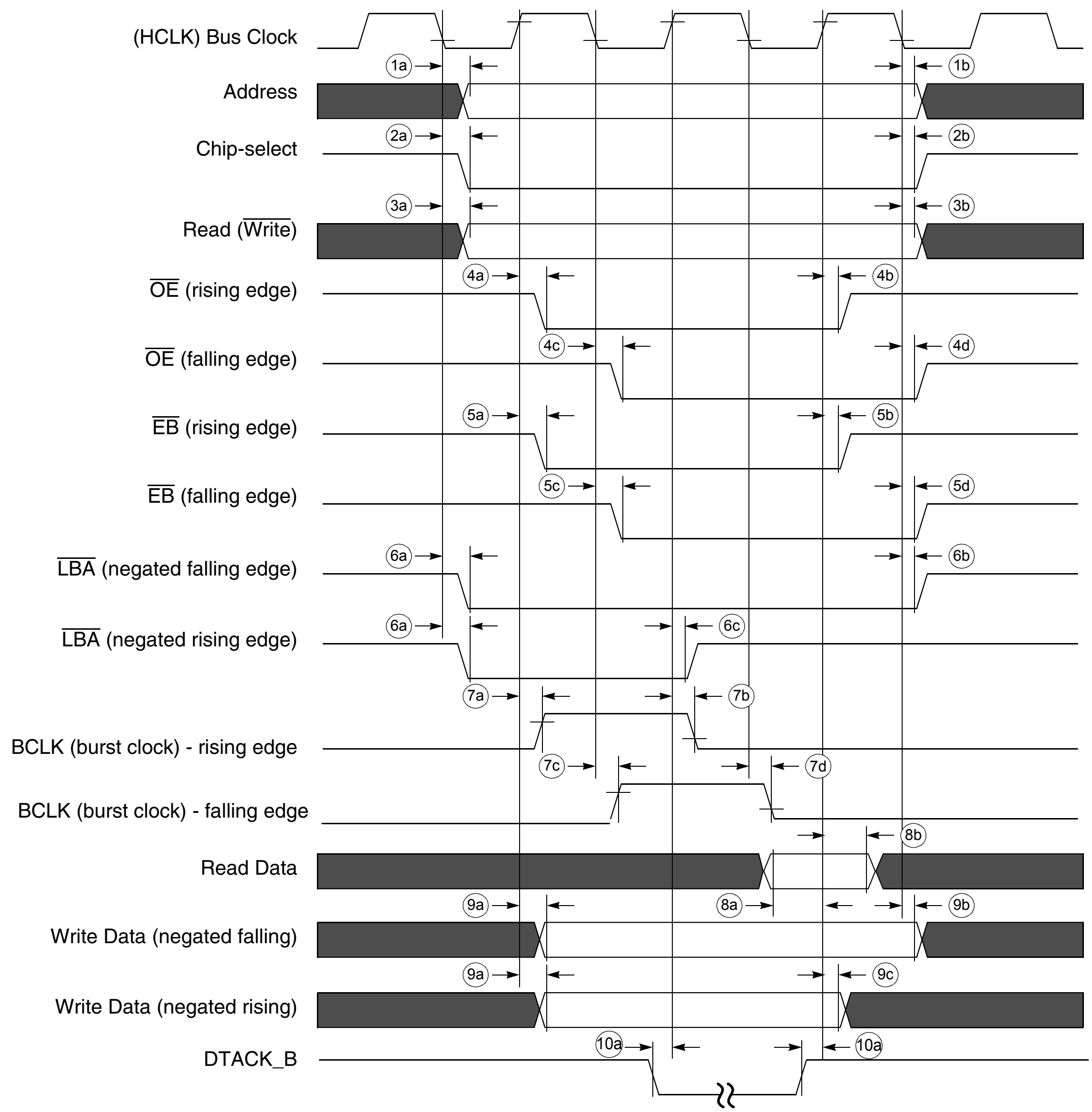


Figure 5. EIM Bus Timing Diagram

Table 12. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	2.48	3.31	9.11	2.4	3.2	8.8	ns
1b	Clock fall to address invalid	1.55	2.48	5.69	1.5	2.4	5.5	ns
2a	Clock fall to chip-select valid	2.69	3.31	7.87	2.6	3.2	7.6	ns
2b	Clock fall to chip-select invalid	1.55	2.48	6.31	1.5	2.4	6.1	ns
3a	Clock fall to Read (Write) Valid	1.35	2.79	6.52	1.3	2.7	6.3	ns
3b	Clock fall to Read (Write) Invalid	1.86	2.59	6.11	1.8	2.5	5.9	ns

4.4.2.2 WAIT Read Cycle DMA Enabled

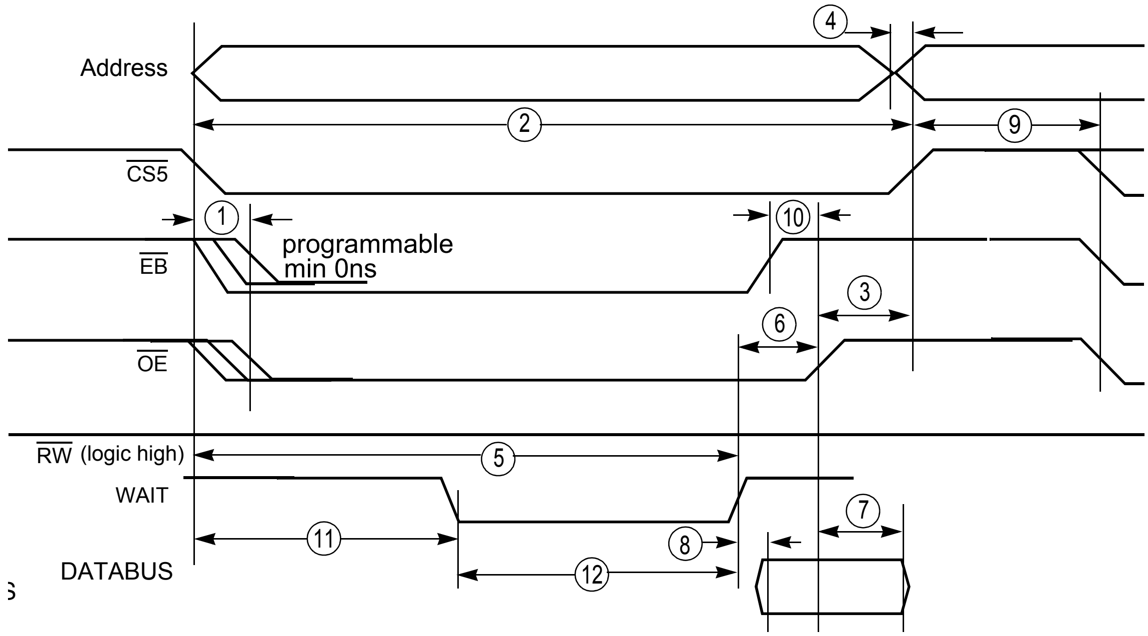


Figure 7. DTACK WAIT Read Cycle DMA Enabled

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated before $\overline{CS5}$ is negated	1.5T-0.68	1.5T-0.06	ns
4	Address inactived before $\overline{CS}$ negated	–	0.05	ns
5	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
6	Wait asserted to $\overline{OE}$ negated	2T+1.57	3T+7.33	ns
7	Data hold timing after $\overline{OE}$ negated	T-1.49	–	ns
8	Data ready after wait is asserted	–	T	ns
9	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
10	OE negate after EB negate	0.06	0.18	ns
11	Wait becomes low after CS5 asserted	0	1019T	ns

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. OE and EB assertion time is programmable by OEA bit in CS5L register. EB assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and CS asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA

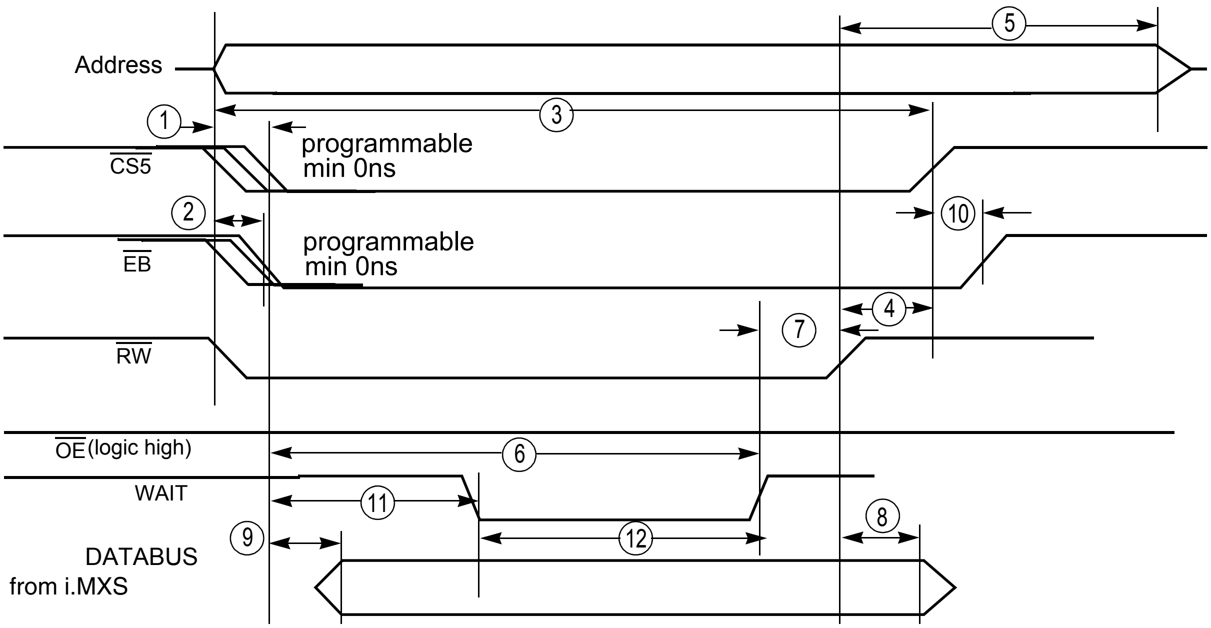


Figure 8. WAIT Write Cycle without DMA

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	CS5 assertion time	See note 2	–	ns
2	EB assertion time	See note 2	–	ns
3	CS5 pulse width	3T	–	ns
4	RW negated before CS5 is negated	2.5T-3.63	2.5T-1.16	ns
5	RW negated to Address inactive	64.22	–	ns
6	Wait asserted after CS5 asserted	–	1020T	ns

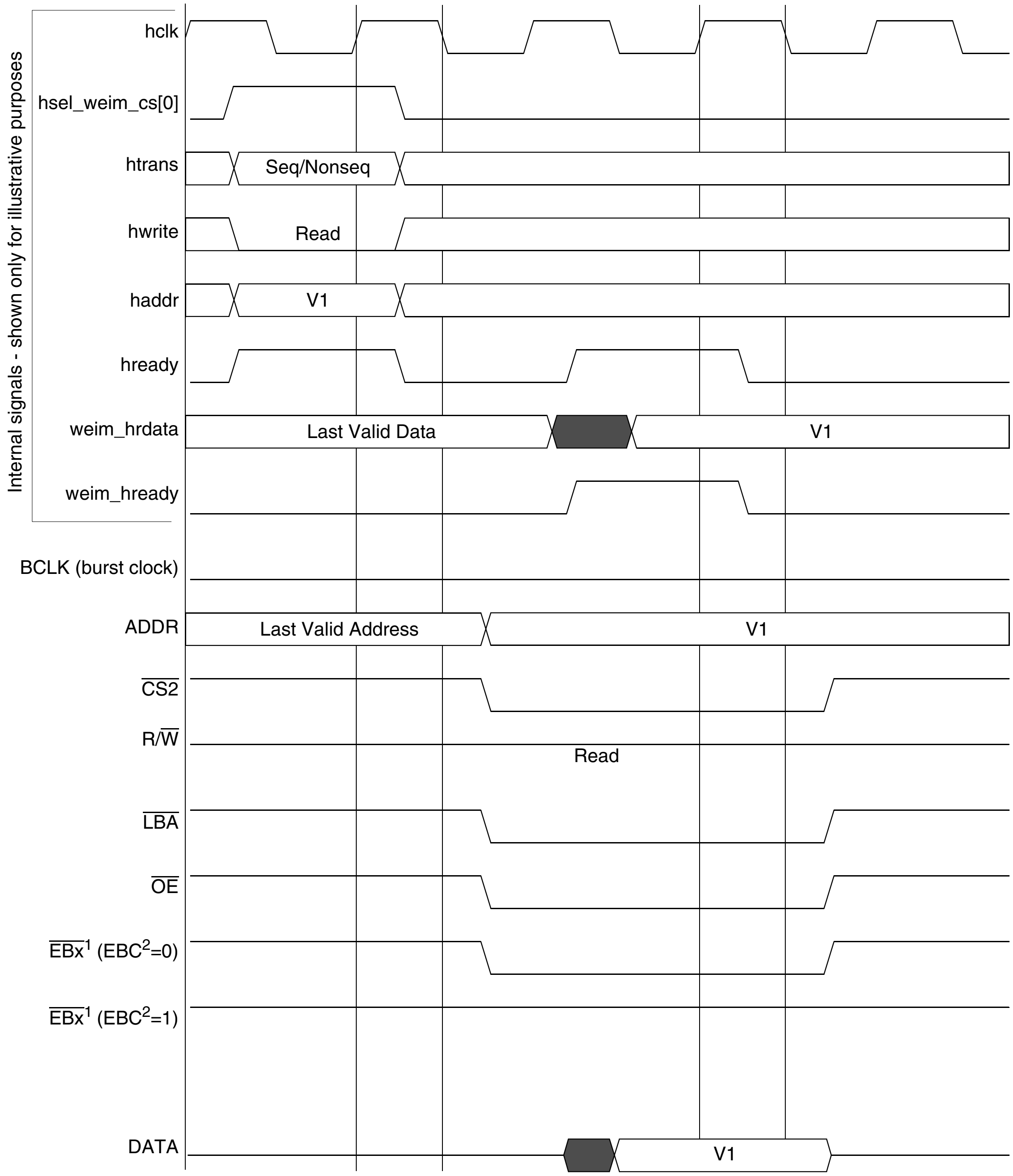
Table 16. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{\text{CS5}}$ assertion time	See note 2	–	ns
2	$\overline{\text{EB}}$ assertion time	See note 2	–	ns
3	$\overline{\text{CS5}}$ pulse width	3T	–	ns
4	$\overline{\text{RW}}$ negated before $\overline{\text{CS5}}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	Address inactived after $\overline{\text{CS}}$ negated	–	0.09	ns
6	Wait asserted after $\overline{\text{CS5}}$ asserted	–	1020T	ns
7	Wait asserted to $\overline{\text{RW}}$ negated	T+2.66	2T+7.96	ns
8	Data hold timing after $\overline{\text{RW}}$ negated	2T+0.03	–	ns
9	Data ready after $\overline{\text{CS5}}$ is asserted	–	T	ns
10	$\overline{\text{CS}}$ deactive to next $\overline{\text{CS}}$ active	T	–	ns
11	$\overline{\text{EB}}$ negate after $\overline{\text{CS}}$ negate	0.5T	0.5T+0.5	
12	Wait becomes low after $\overline{\text{CS5}}$ asserted	0	1019T	ns
13	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{\text{CS5}}$ assertion can be controlled by CSA bits. $\overline{\text{EB}}$ assertion also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{\text{RW}}$ asserts at the start of write access cycle.
4.The external wait input requirement is eliminated when $\overline{\text{CS5}}$ is programmed to use internal wait state.

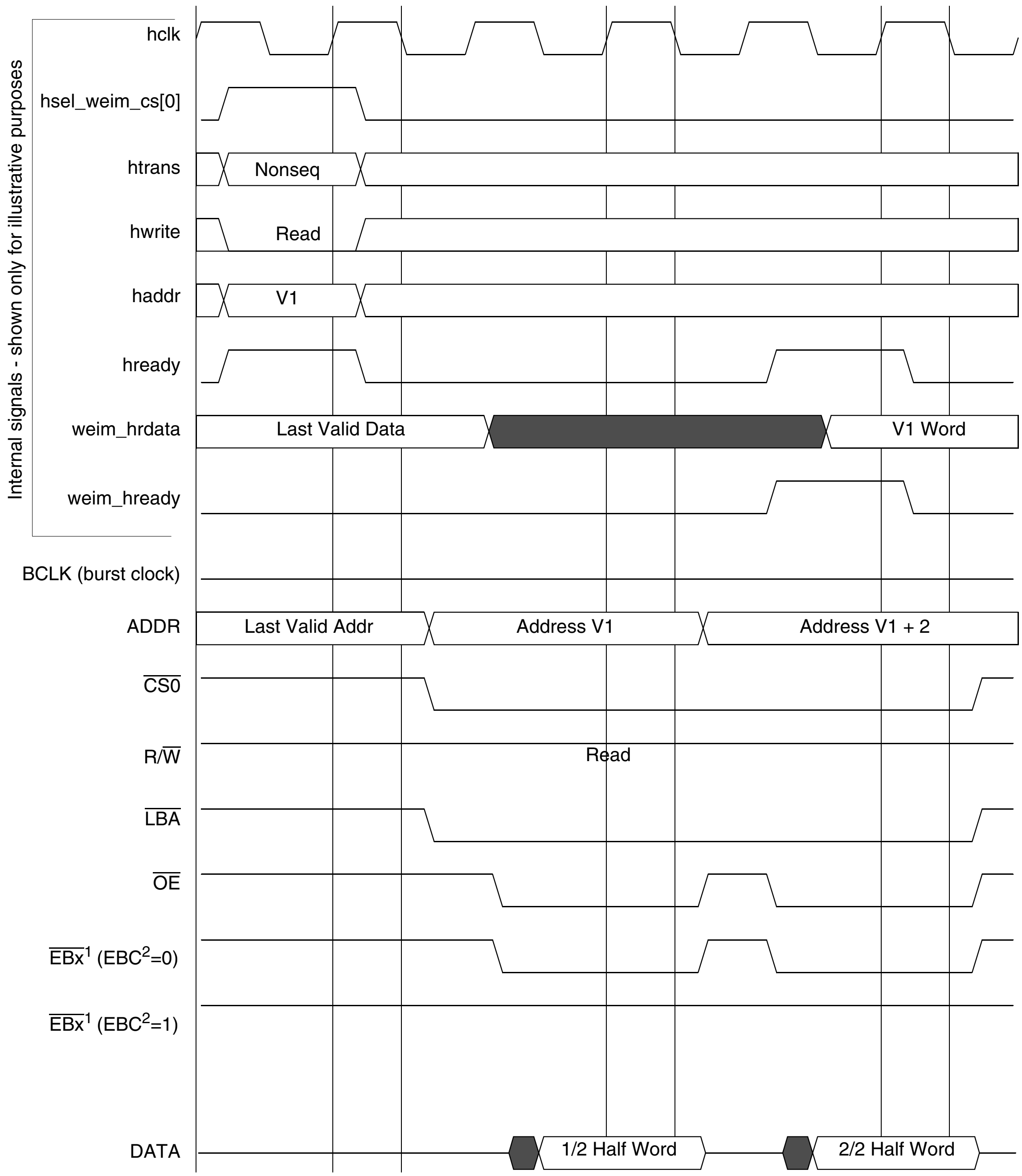
4.4.3 EIM External Bus Timing

The External Interface Module (EIM) is the interface to devices external to the i.MXS, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 10. WSC = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 12. WSC = 1, OEA = 1, A.WORD/E.HALF

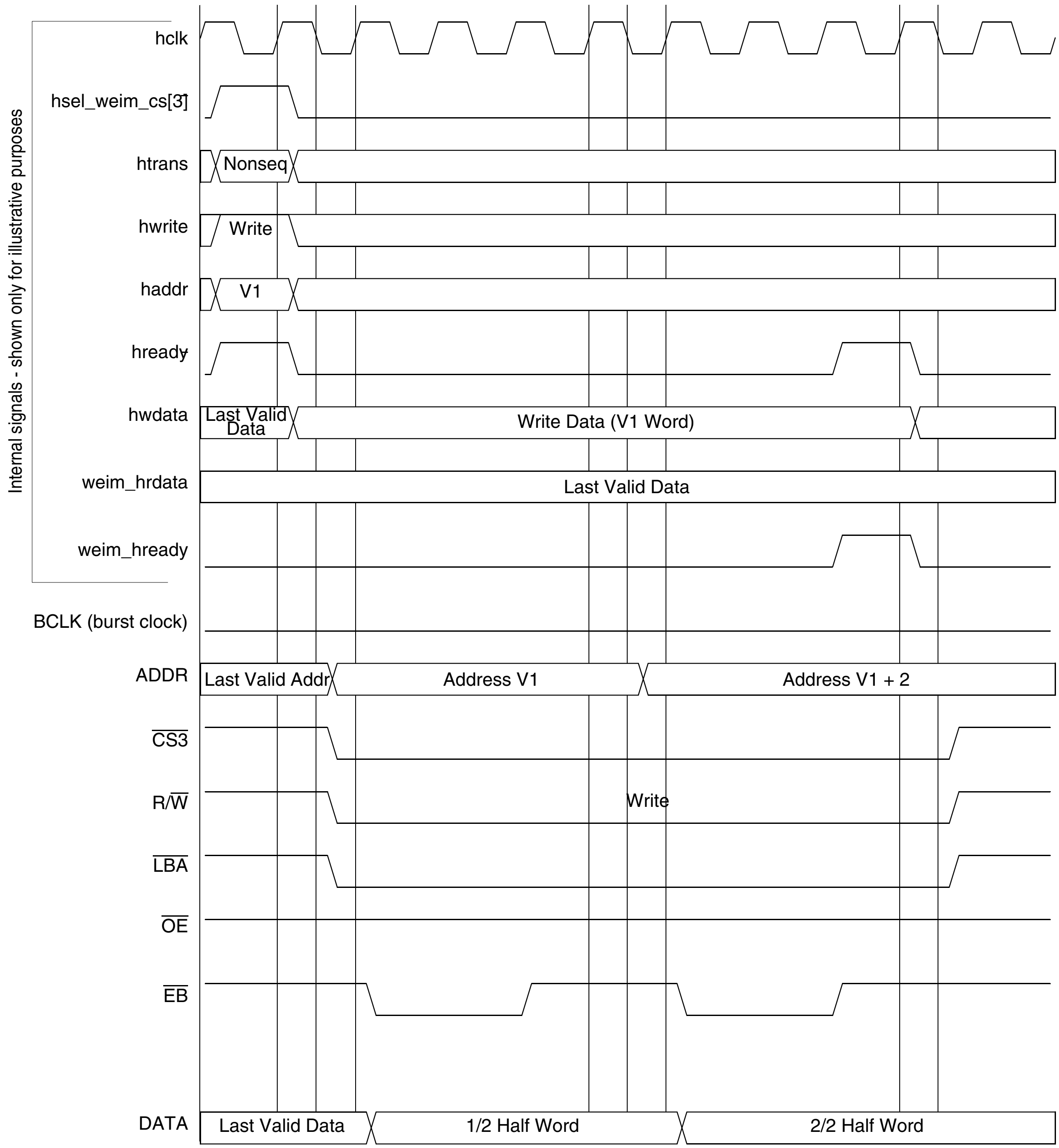
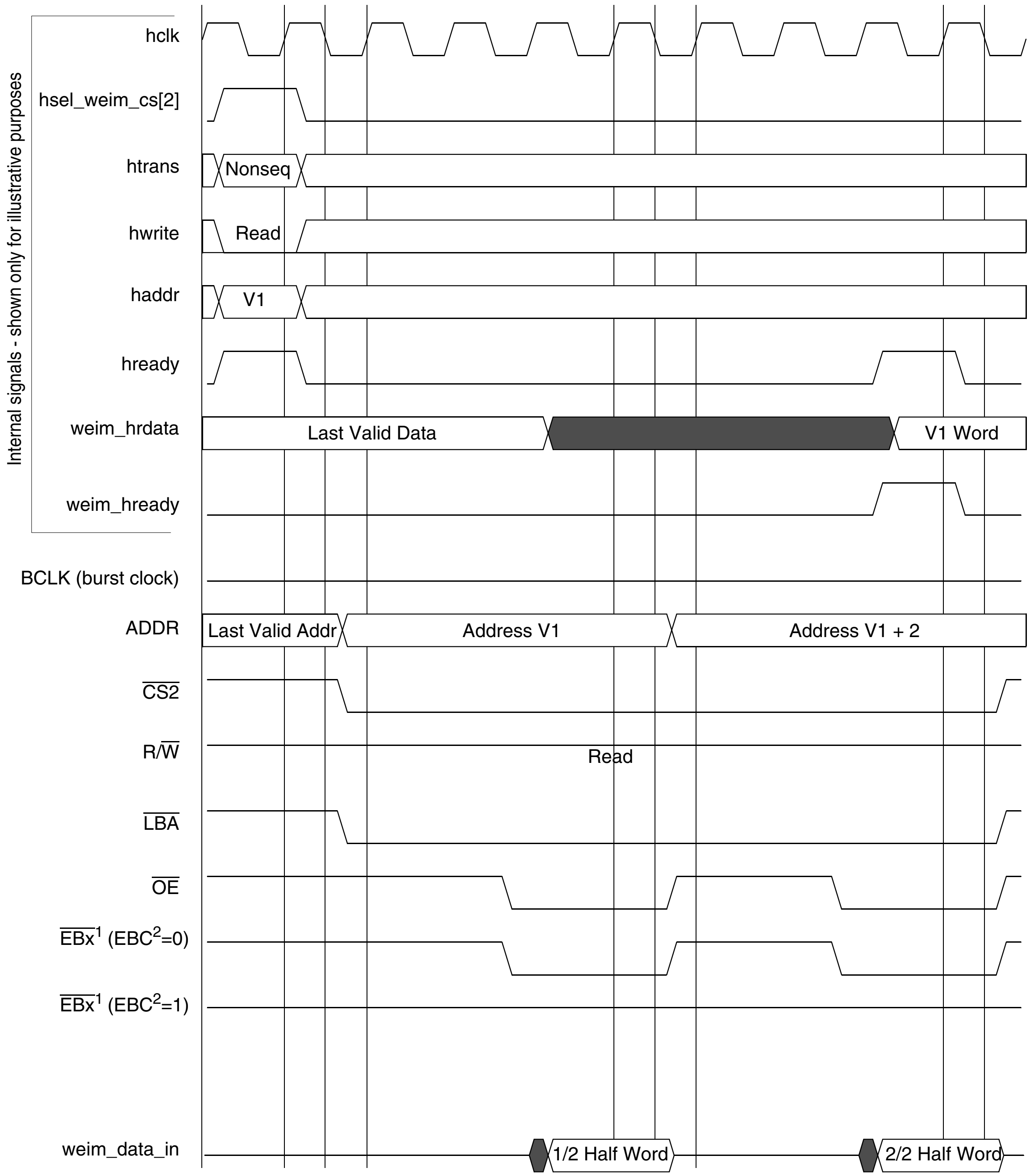
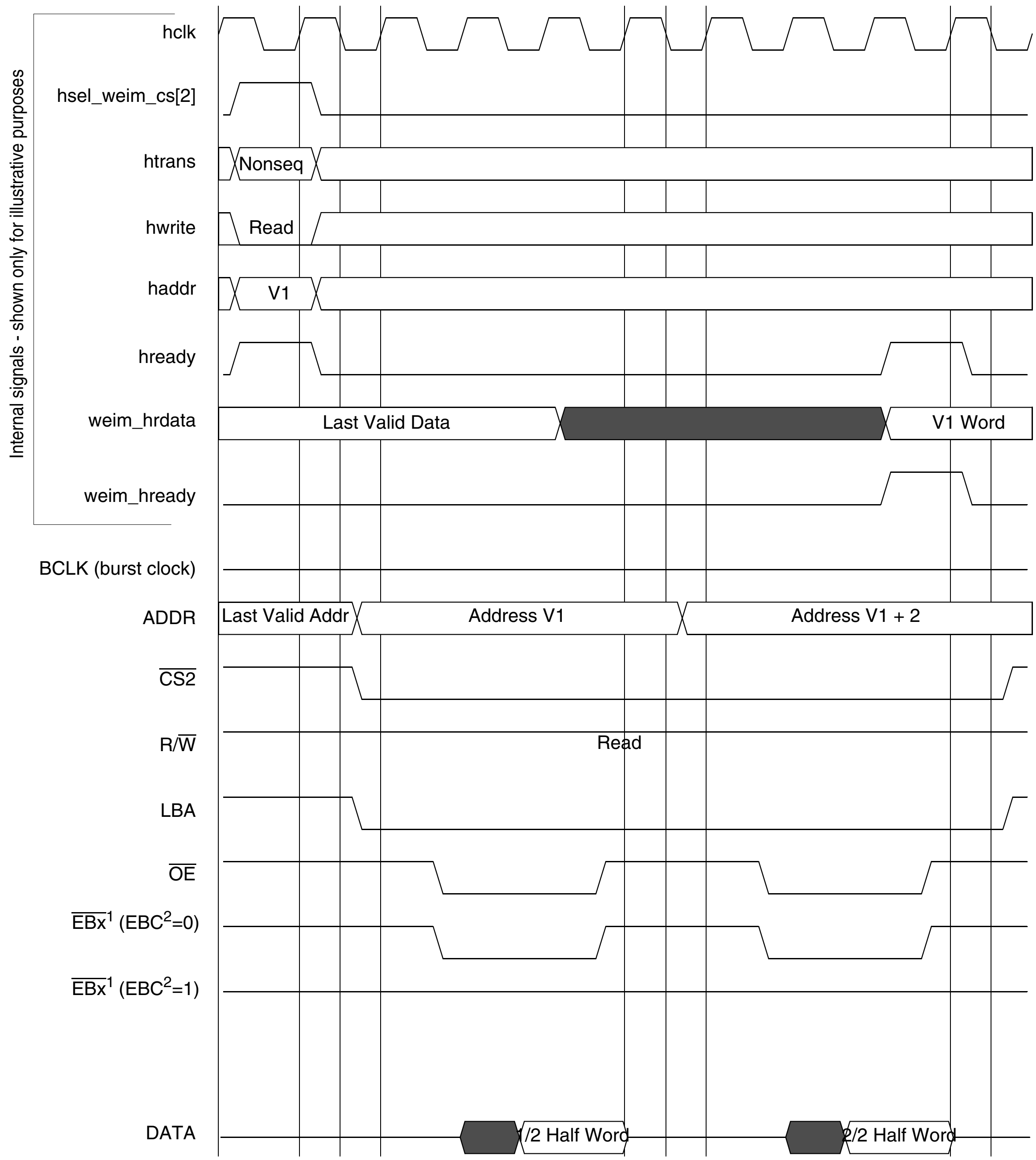


Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 16. WSC = 3, OEA = 4, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

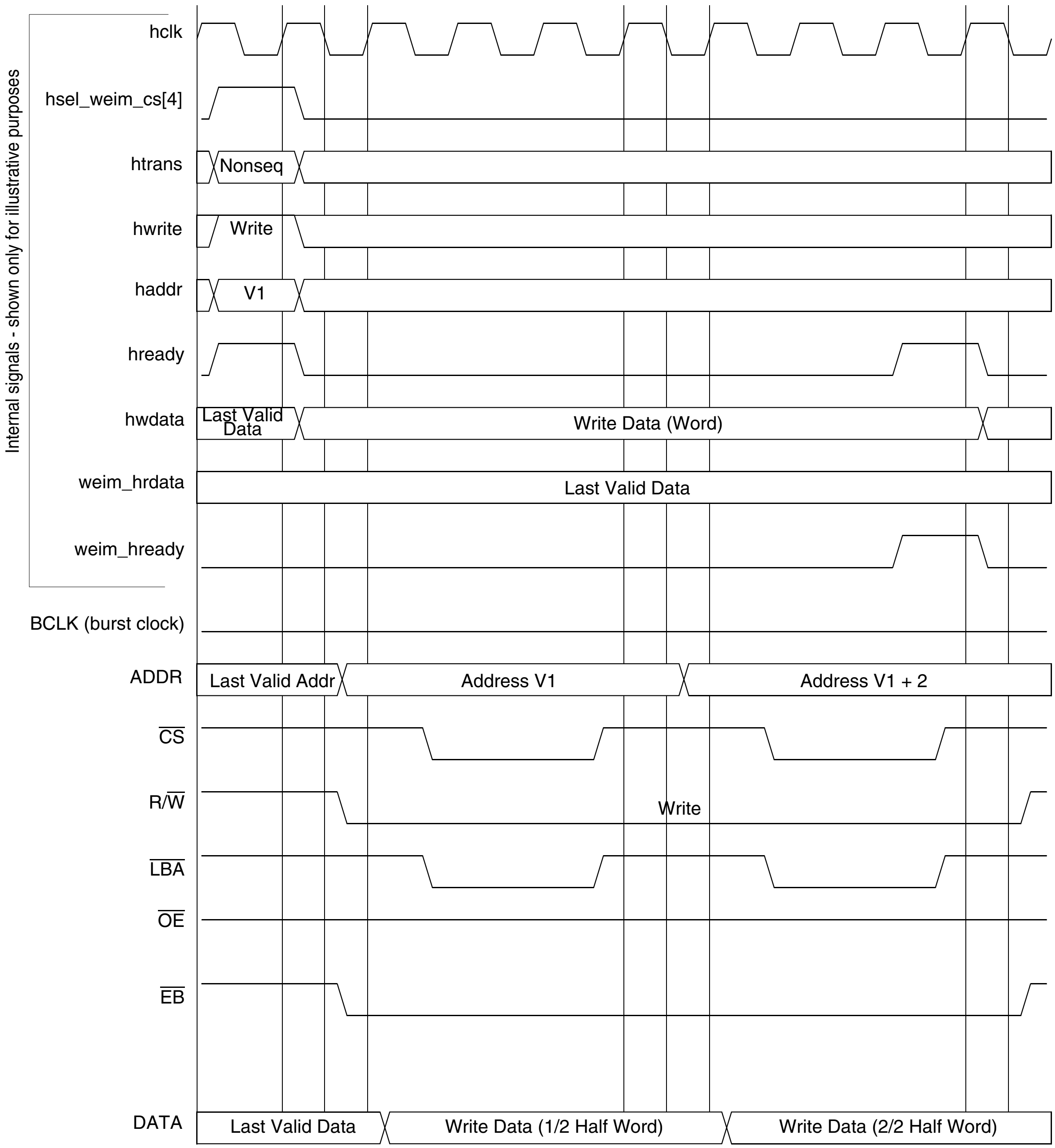
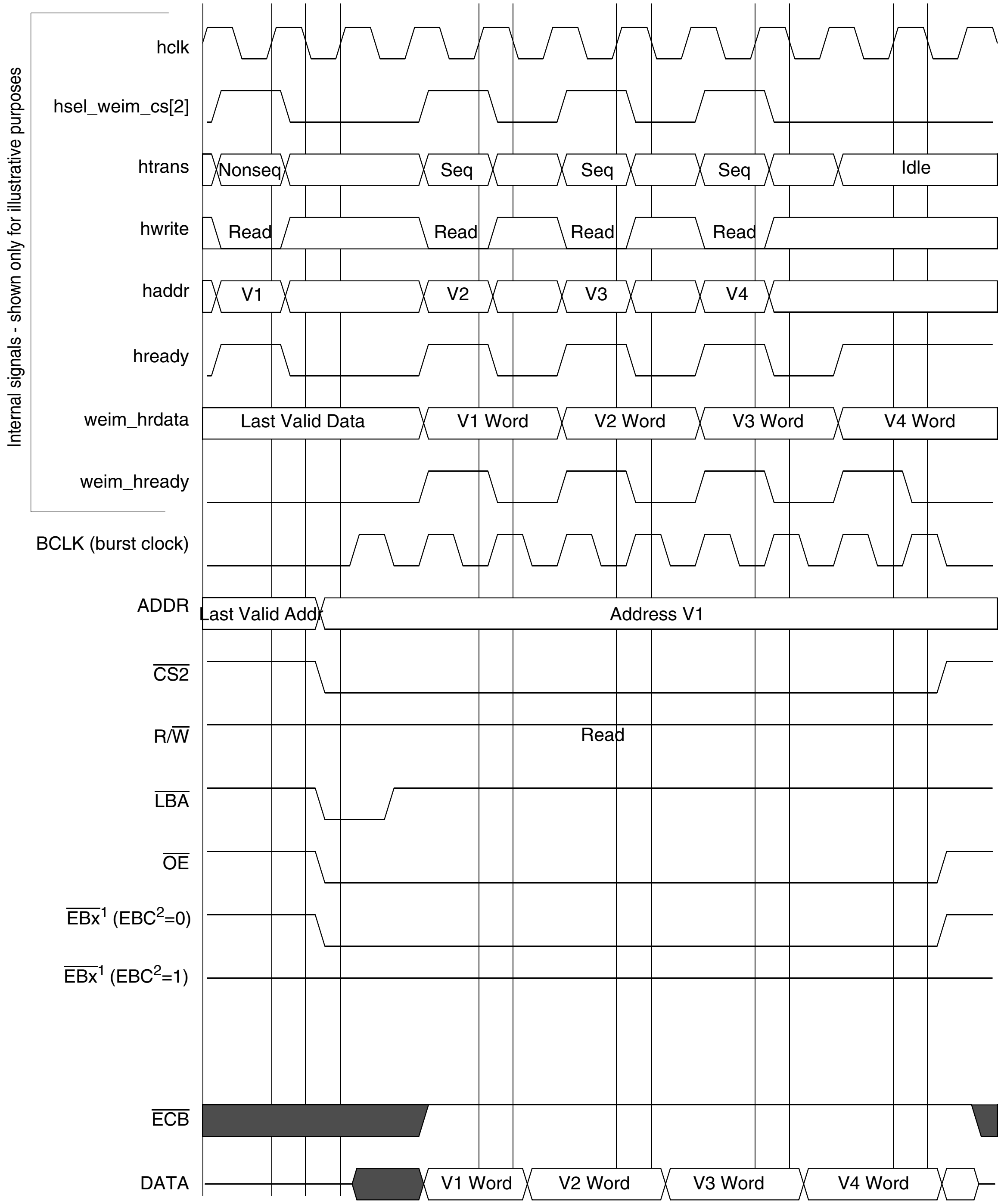


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 29. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

Table 22. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency[1]	0	87	0	100	MHz
2a	Clock high time[1]	3.3	–	5/10	–	ns
2b	Clock low time[1]	7.5	–	5/10	–	ns
3a	Clock fall time[1]	–	5	–	5/10	ns
3b	Clock rise time[1]	–	6.67	–	5/10	ns
4a	Output delay time[1]	5.7	–	5	–	ns
4b	Output setup time[1]	5.7	–	5	–	ns

[1] C_L of PWMO = 30 pF

4.8 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.

Table 25. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP1}	–	ns
7	Auto precharge command period	t_{RC1}	–	t_{RC1}	–	ns

1 t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *MC9328MXS reference manual*.

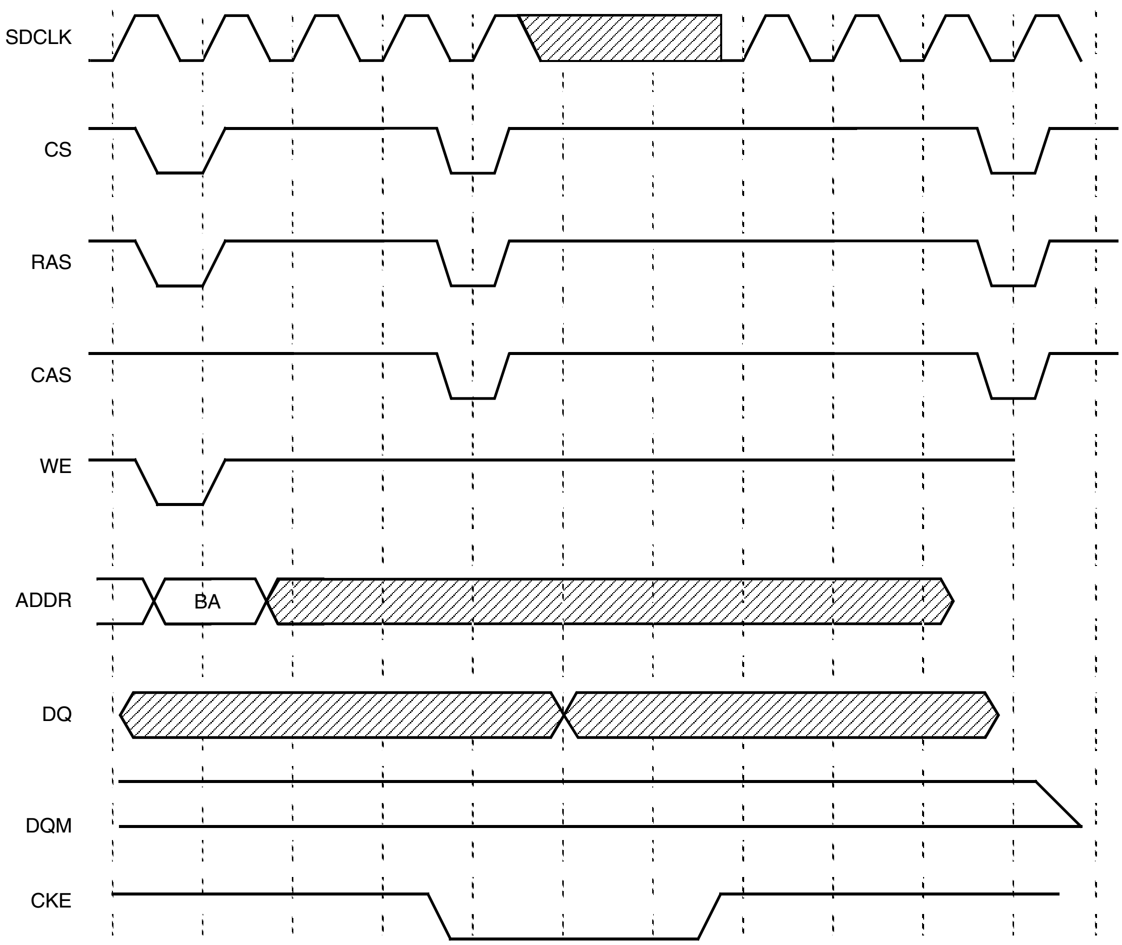


Figure 46. SDRAM Self-Refresh Cycle Timing Diagram

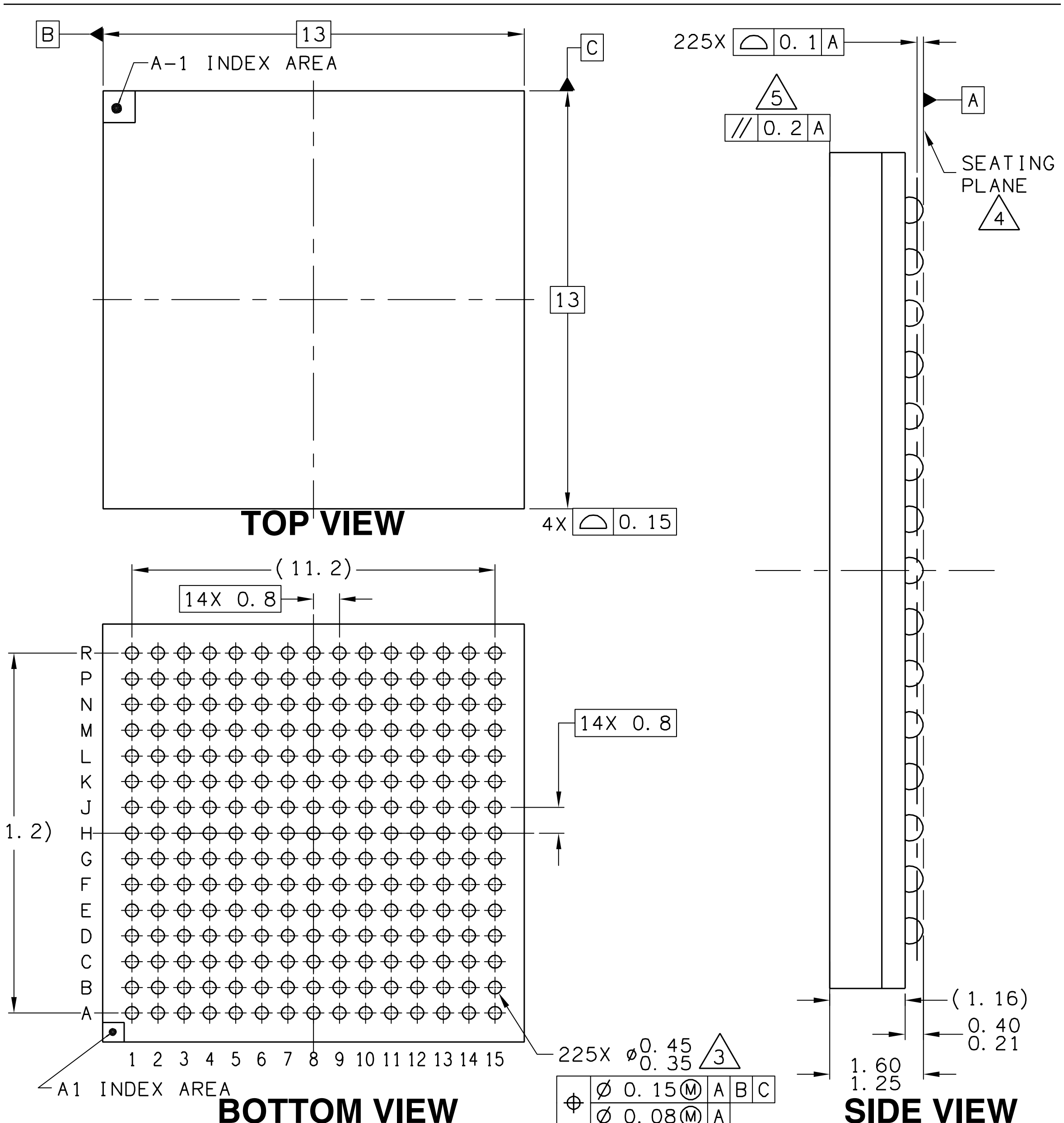
Table 29. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
6	STCK high to STFS (wl) high[3]	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high[3]	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low[3]	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low[3]	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	–	18.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Primary Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function[2])						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns

5.1 MAPBGA 225 Package Dimensions

Figure 54 illustrates the 225 MAPBGA 13 mm × 13 mm package.

Case Outline 1304B



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES PER ASME Y14 5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 54. i.MXS 225 MAPBGA Mechanical Drawing

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