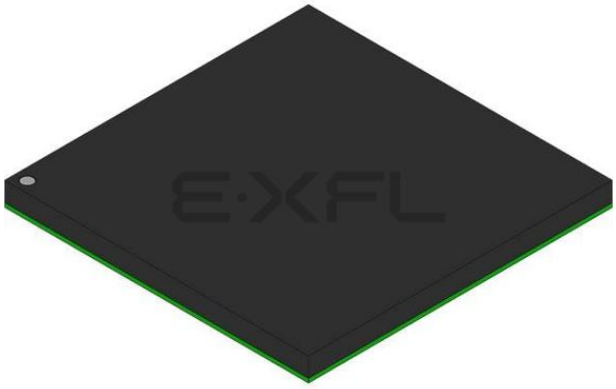

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM920T |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 100MHz |
| Co-Processors/DSP | - |
| RAM Controllers | SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | LCD |
| Ethernet | - |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 1.8V, 3V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 225-LFBGA |
| Supplier Device Package | 225-MAPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mxsvp10 |

# 2 Signals and Connections

Table 2 identifies and describes the i.MXS processor signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

**Table 2. i.MXS Signal Descriptions**

| Signal Name | Function/Notes |
|---|---|
| **External Bus/Chip-Select (EIM)** | |
| A[24:0] | Address bus signals |
| D[31:0] | Data bus signals |
| $\overline{EB0}$ | MSB Byte Strobe—Active low external enable byte signal that controls D [31:24]. |
| $\overline{EB1}$ | Byte Strobe—Active low external enable byte signal that controls D [23:16]. |
| $\overline{EB2}$ | Byte Strobe—Active low external enable byte signal that controls D [15:8]. |
| $\overline{EB3}$ | LSB Byte Strobe—Active low external enable byte signal that controls D [7:0]. |
| $\overline{OE}$ | Memory Output Enable—Active low output enables external data bus. |
| $\overline{CS}$ [5:0] | Chip-Select—The chip-select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default $\overline{CSD}$ [1:0] is selected. |
| $\overline{ECB}$ | Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence. |
| $\overline{LBA}$ | Active low signal sent by a flash device causing the external burst device to latch the starting burst address. |
| BCLK (burst clock) | Clock signal sent to external synchronous memories (such as burst flash) during burst mode. |
| $\overline{RW}$ | $\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a $\overline{WE}$ input signal by external DRAM. |
| $\overline{DTACK}$ | $\overline{DTACK}$ signal—The external input data acknowledge signal. When using the external DTACK signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external DTACK signal after 1022 clock counts have elapsed. |
| **Bootstrap** | |
| BOOT [3:0] | System Boot Mode Select—The operational system boot mode of the i.MXS processor upon system reset is determined by the settings of these pins. |
| **SDRAM Controller** | |
| SDBA [4:0] | SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles. |
| SDIBA [3:0] | SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles. |
| MA [11:10] | SDRAM address signals |
| MA [9:0] | SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles. |
| DQM [3:0] | SDRAM data enable |
| $\overline{CSD0}$ | SDRAM Chip-select signal which is multiplexed with the $\overline{CS2}$ signal. These two signals are selectable by programming the system control register. |

**Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | Primary | | | Alternate | | GPIO | | AIN | BIN | AOUT | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Signal | Dir | Pull-Up | Signal | Dir | Mux | Pull-Up | | | | |
| NVDD1 | G2 | A18 | O | | ETMTRACEPKT2 | O | PA26 | 69K | | | | A18 |
| NVDD1 | G4 | D25 | I/O | 69K | | | | | | | | |
| NVDD1 | G1 | A17 | O | | ETMTRACEPKT1 | O | PA25 | 69K | | | | A17 |
| NVDD1 | H4 | D24 | I/O | 69K | | | | | | | | |
| NVDD1 | H2 | A16 | O | | ETMTRACEPKT0 | O | PA24 | 69K | | | | A16 |
| NVDD1 | H3 | D23 | I/O | 69K | | | | | | | | |
| NVDD1 | H1 | A15 | O | | | | | | | | | |
| NVDD1 | H5 | D22 | I/O | 69K | | | | | | | | |
| NVDD1 | J1 | A14 | O | | | | | | | | | |
| NVDD1 | J3 | D21 | I/O | 69K | | | | | | | | |
| NVDD1 | K1 | A13 | O | | | | | | | | | |
| NVDD1 | J4 | D20 | I/O | 69K | | | | | | | | |
| NVDD1 | J2 | A12 | O | | | | | | | | | |
| NVDD1 | K4 | D19 | I/O | 69K | | | | | | | | |
| NVDD1 | K2 | A11 | O | | | | | | | | | |
| NVDD1 | L4 | D18 | I/O | 69K | | | | | | | | |
| NVDD1 | L1 | A10 | O | | | | | | | | | |
| NVDD1 | L3 | D17 | I/O | 69K | | | | | | | | |
| NVDD1 | L2 | A9 | O | | | | | | | | | |
| NVDD1 | M1 | D16 | I/O | 69K | | | | | | | | |
| NVDD1 | N1 | A8 | O | | | | | | | | | |
| NVDD1 | M2 | D15 | I/O | 69K | | | | | | | | |
| NVDD1 | N2 | A7 | O | | | | | | | | | |
| NVDD1 | P1 | D14 | I/O | 69K | | | | | | | | |
| NVDD1 | R1 | A6 | O | | | | | | | | | |
| NVDD1 | M3 | D13 | I/O | 69K | | | | | | | | |
| NVDD1 | P2 | A5 | O | | | | | | | | | |
| NVDD1 | N3 | D12 | I/O | 69K | | | | | | | | |
| NVDD1 | P3 | A4 | O | | | | | | | | | |
| NVDD1 | R2 | D11 | I/O | 69K | | | | | | | | |
| NVDD1 | N4 | $\overline{EB0}$ | O | | | | | | | | | |
| NVDD1 | M4 | D10 | I/O | 69K | | | | | | | | |
| NVDD1 | P4 | A3 | O | | | | | | | | | |
| NVDD1 | R3 | $\overline{EB1}$ | O | | | | | | | | | |
| NVDD1 | N5 | D9 | I/O | 69K | | | | | | | | |
| NVDD1 | R4 | $\overline{EB2}$ | O | | | | | | | | | |

## 4.2 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table, $T_{ref}$ is a reference clock period after the pre-divider and $T_{dck}$ is the output double clock period.

**Table 10. DPLL Specifications**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| DPLL input clock freq range | Vcc = 1.8V | 5 | – | 100 | MHz |
| Pre-divider output clock freq range | Vcc = 1.8V | 5 | – | 30 | MHz |
| DPLL output clock freq range | Vcc = 1.8V | 80 | – | 220 | MHz |
| Pre-divider factor (PD) | – | 1 | – | 16 | – |
| Total multiplication factor (MF) | Includes both integer and fractional parts | 5 | – | 15 | – |
| MF integer part | – | 5 | – | 15 | – |
| MF numerator | Should be less than the denominator | 0 | – | 1022 | – |
| MF denominator | – | 1 | – | 1023 | – |
| Pre-multiplier lock-in time | – | – | – | 312.5 | µsec |
| Freq lock-in time after full reset | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 250 | 280 (56 µs) | 300 | $T_{ref}$ |
| Freq lock-in time after partial reset | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 220 | 250 (50 µs) | 270 | $T_{ref}$ |
| Phase lock-in time after full reset | FPL mode and integer MF (does not include pre-multi lock-in time) | 300 | 350 (70 µs) | 400 | $T_{ref}$ |
| Phase lock-in time after partial reset | FPL mode and integer MF (does not include pre-multi lock-in time) | 270 | 320 (64 µs) | 370 | $T_{ref}$ |
| Freq jitter (p-p) | – | – | 0.005 (0.01%) | 0.01 | $2 \bullet T_{dck}$ |
| Phase jitter (p-p) | Integer MF, FPL mode, Vcc=1.8V | – | 1.0 (10%) | 1.5 | ns |
| Power supply voltage | – | 1.7 | – | 2.5 | V |
| Power dissipation | FOL mode, integer MF, $f_{dck}$ = 100 MHz, Vcc = 1.8V | – | – | 4 | mW |

## 4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4.

**NOTE**

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

**Table 11. Reset Module Timing Parameter Table**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 1 | Width of input POWER_ON_RESET | note[1] | – | note[1] | – | – |
| 2 | Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz) | 300 | 300 | 300 | 300 | ms |
| 3 | 7K to 32K-cycle stretcher for SDRAM reset | 7 | 7 | 7 | 7 | Cycles of CLK32 |
| 4 | 14K to 32K-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$ | 14 | 14 | 14 | 14 | Cycles of CLK32 |
| 5 | Width of external hard-reset $\overline{\text{RESET\_IN}}$ | 4 | – | 4 | – | Cycles of CLK32 |
| 6 | 4K to 32K-cycle qualifier | 4 | 4 | 4 | 4 | Cycles of CLK32 |

[1] POR width is dependent on the 32 or 32.768 kHz crystal oscillator start-up time. Design margin should allow for crystal tolerance, i.MX chip variations, temperature impact, and supply voltage influence. Through the process of supplying crystals for use with CMOS oscillators, crystal manufacturers have developed a working knowledge of start-up time of their crystals. Typically, start-up times range from 400 ms to 1.2 seconds for this type of crystal.
If an external stable clock source (already running) is used instead of a crystal, the width of POR should be ignored in calculating timing for the start-up process.

## 4.4 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the i.MXS processor, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.

### 4.4.2.1 WAIT Read Cycle without DMA

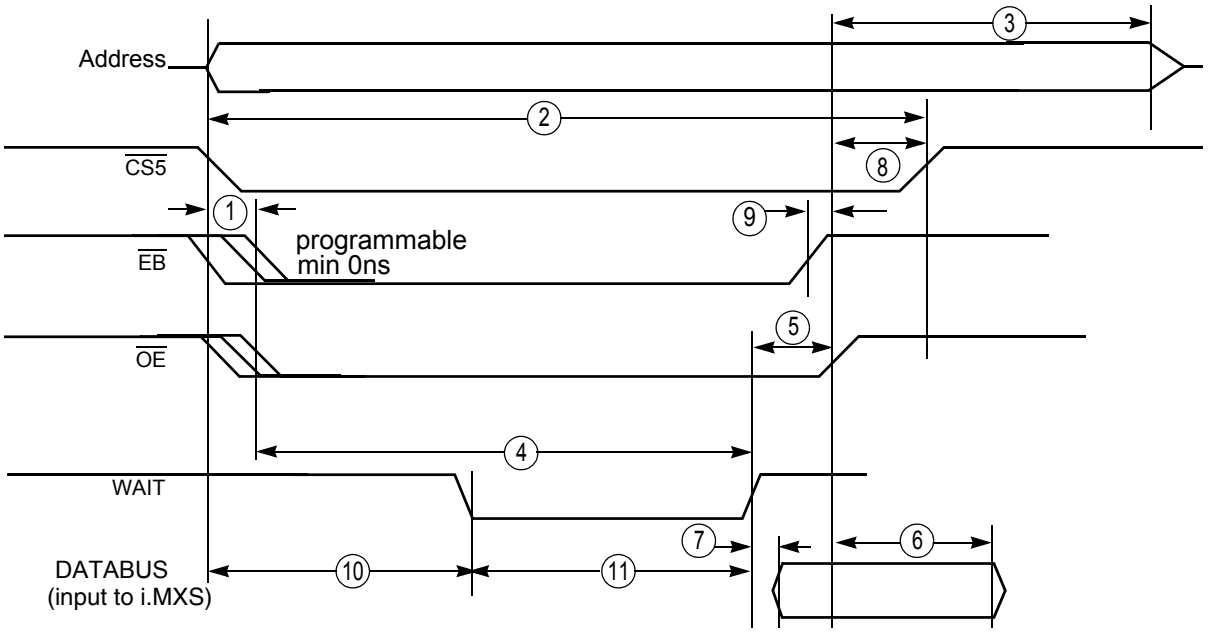



**Figure 6. WAIT Read Cycle without DMA**

**Table 13. WAIT Read Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz**

| Number | Characteristic | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $\overline{OE}$ and $\overline{EB}$ assertion time | See note 2 | – | ns |
| 2 | $\overline{CS5}$ pulse width | 3T | – | ns |
| 3 | $\overline{OE}$ negated to address inactive | 56.81 | 57.28 | ns |
| 4 | Wait asserted after $\overline{OE}$ asserted | – | 1020T | ns |
| 5 | Wait asserted to $\overline{OE}$ negated | 2T+1.57 | 3T+7.33 | ns |
| 6 | Data hold timing after $\overline{OE}$ negated | T-1.49 | – | ns |
| 7 | Data ready after wait asserted | 0 | T | ns |
| 8 | OE negated to CS negated | 1.5T-0.68 | 1.5T-0.06 | ns |
| 9 | OE negated after EB negated | 0.06 | 0.18 | ns |
| 10 | Become low after CS5 asserted | 0 | 1019T | ns |
| 11 | Wait pulse width | 1T | 1020T | ns |

**Note**:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

### 4.4.2.2 WAIT Read Cycle DMA Enabled

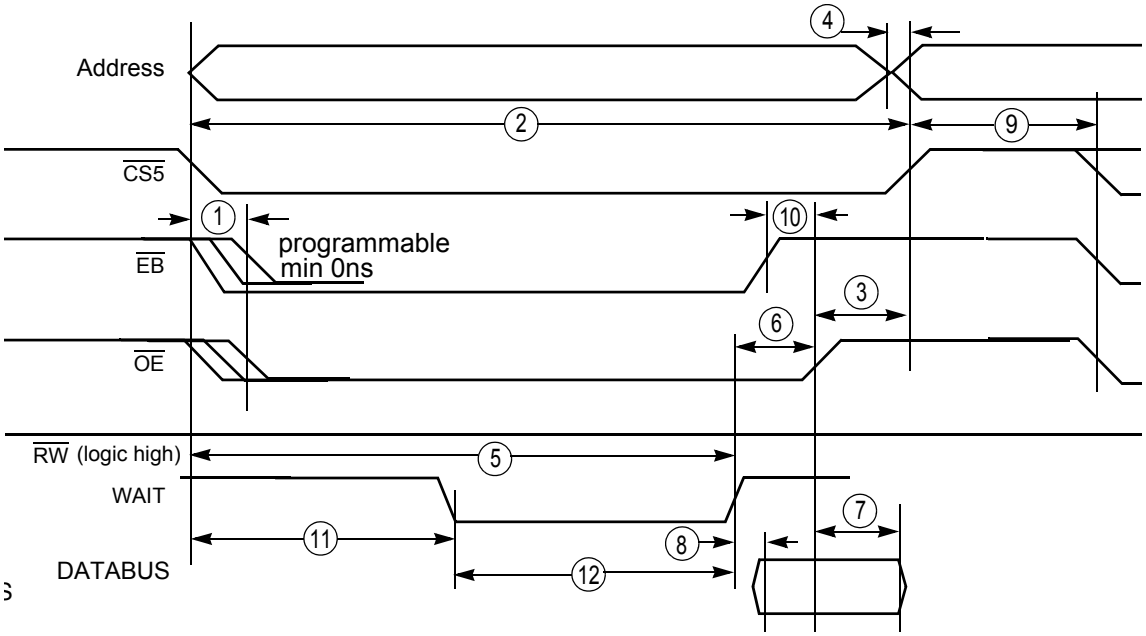
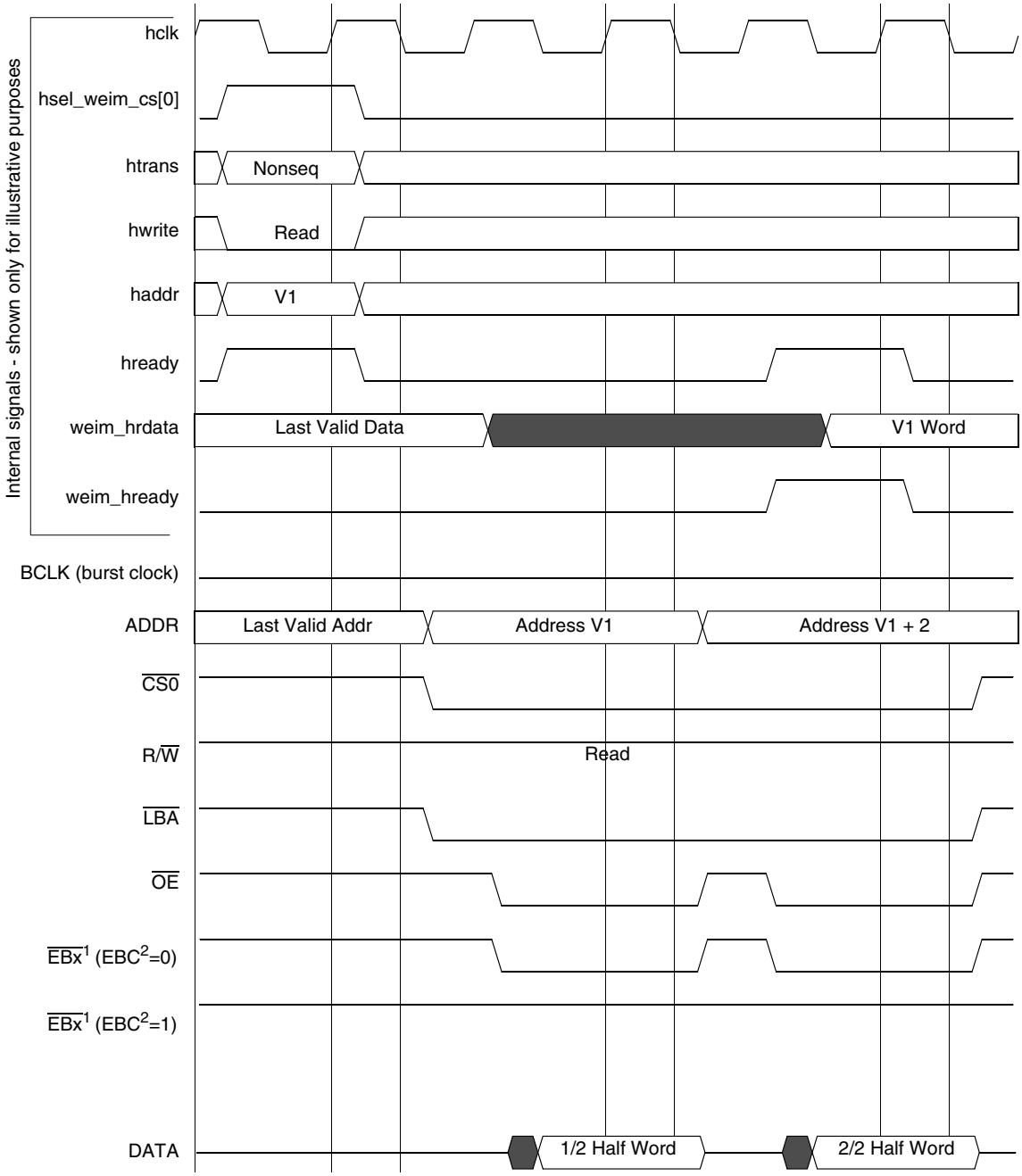



**Figure 7. DTACK WAIT Read Cycle DMA Enabled**

**Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz**

| Number | Characteristic | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $\overline{OE}$ and $\overline{EB}$ assertion time | See note 2 | – | ns |
| 2 | $\overline{CS}$ pulse width | 3T | – | ns |
| 3 | $\overline{OE}$ negated before $\overline{CS5}$ is negated | 1.5T-0.68 | 1.5T-0.06 | ns |
| 4 | Address inactived before $\overline{CS}$ negated | – | 0.05 | ns |
| 5 | Wait asserted after $\overline{CS5}$ asserted | – | 1020T | ns |
| 6 | Wait asserted to $\overline{OE}$ negated | 2T+1.57 | 3T+7.33 | ns |
| 7 | Data hold timing after $\overline{OE}$ negated | T-1.49 | – | ns |
| 8 | Data ready after wait is asserted | – | T | ns |
| 9 | $\overline{CS}$ deactive to next $\overline{CS}$ active | T | – | ns |
| 10 | OE negate after EB negate | 0.06 | 0.18 | ns |
| 11 | Wait becomes low after CS5 asserted | 0 | 1019T | ns |




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 12. WSC = 1, OEA = 1, A.WORD/E.HALF**

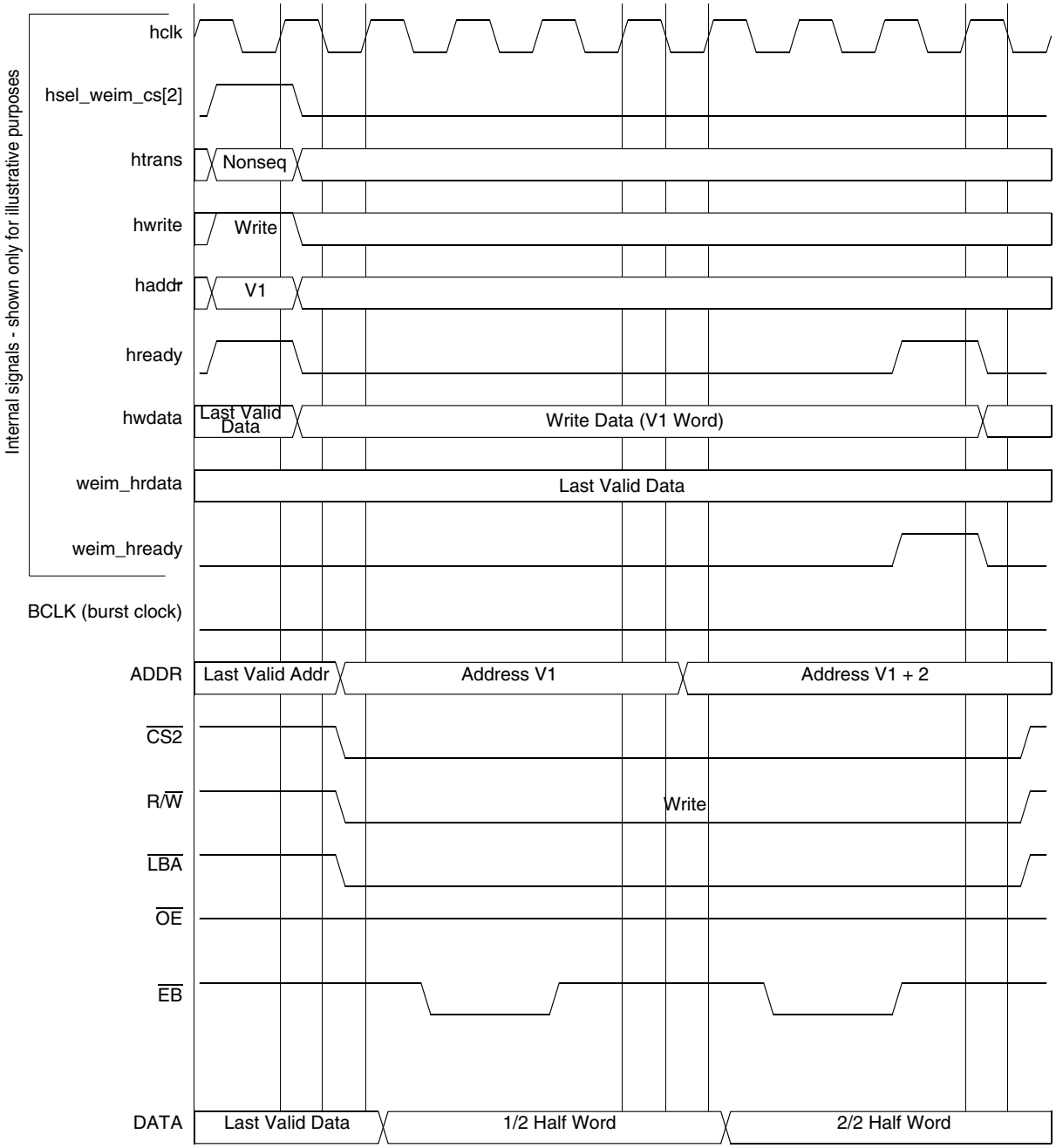
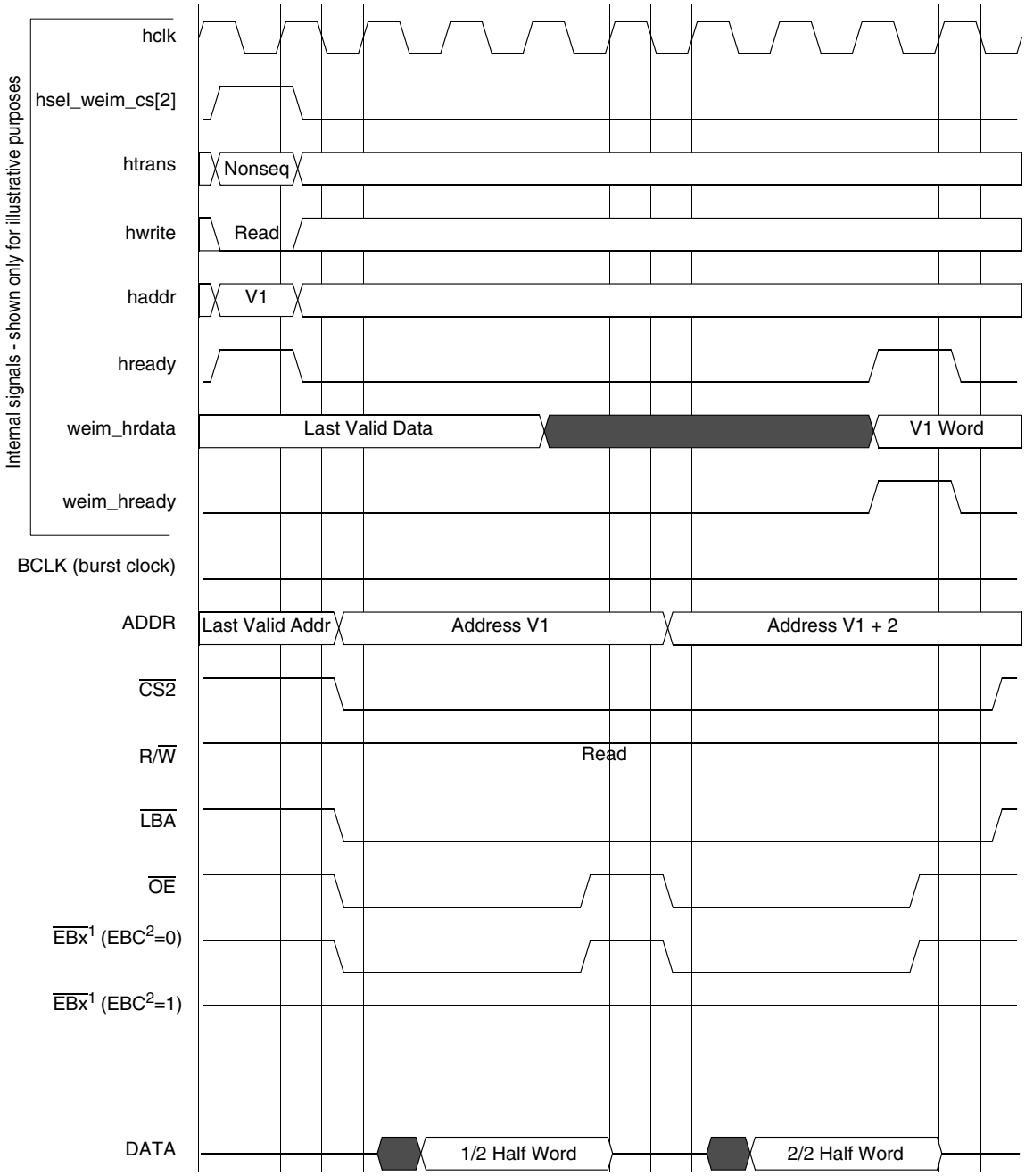
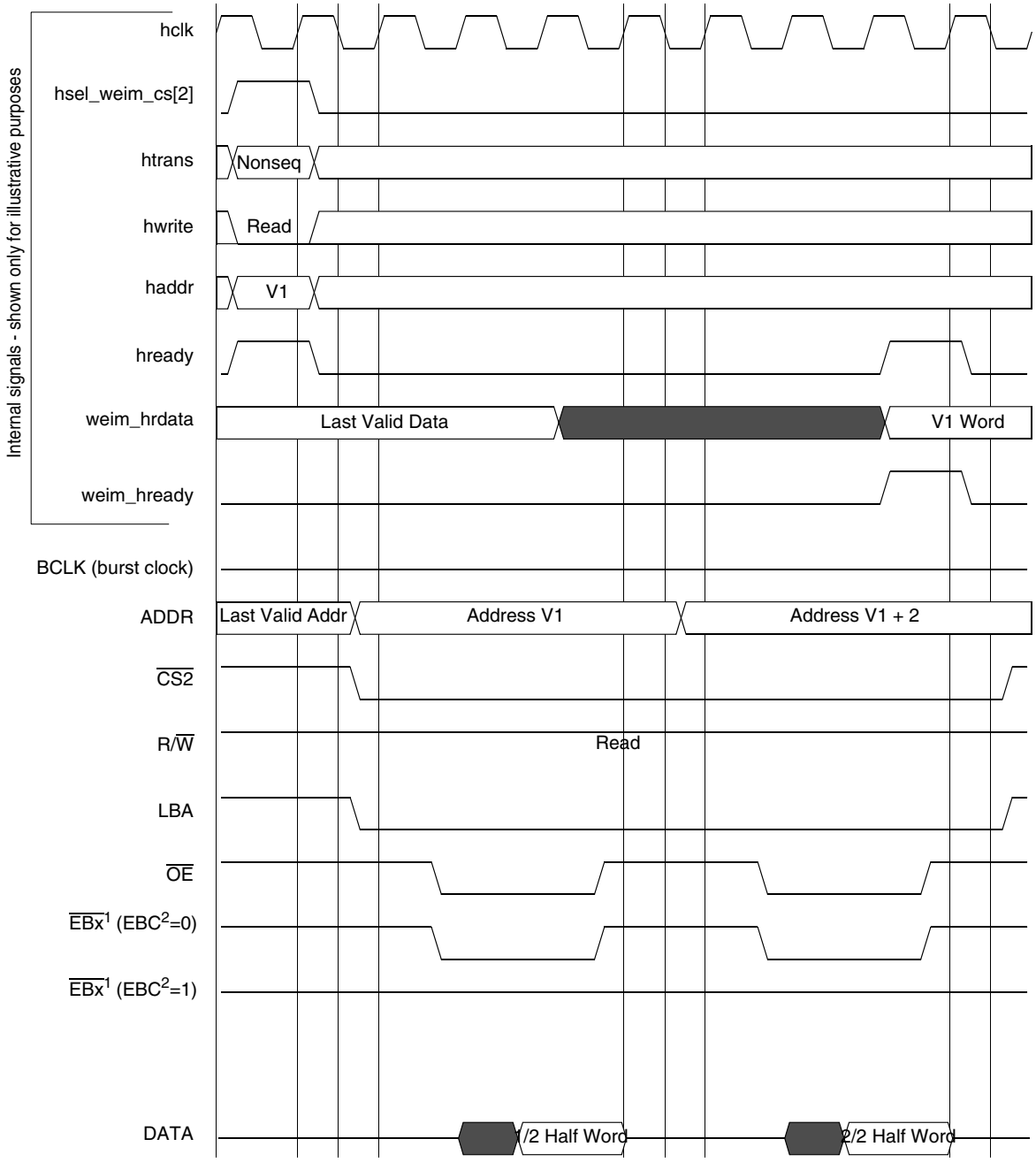



**Figure 17. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF**



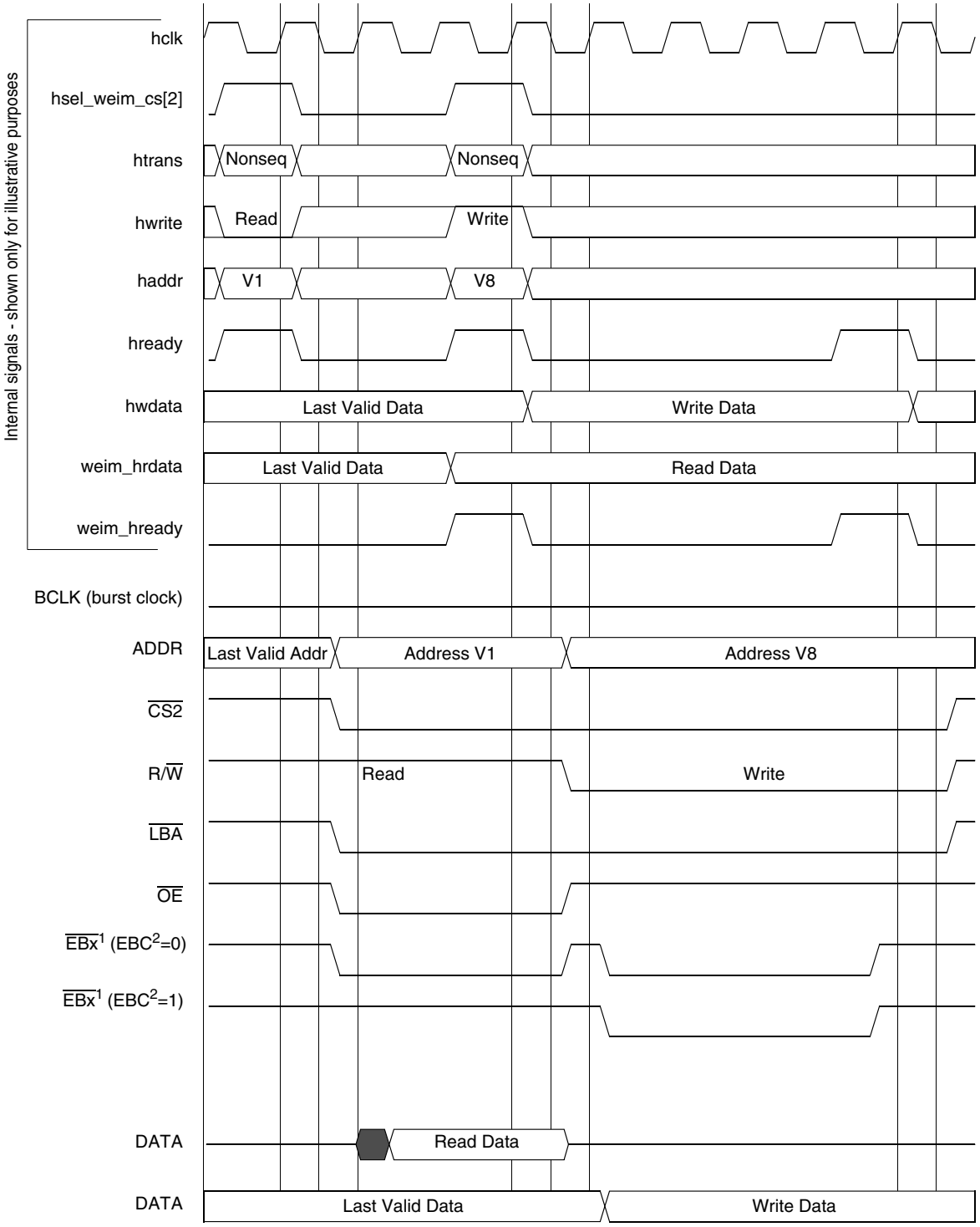

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF**



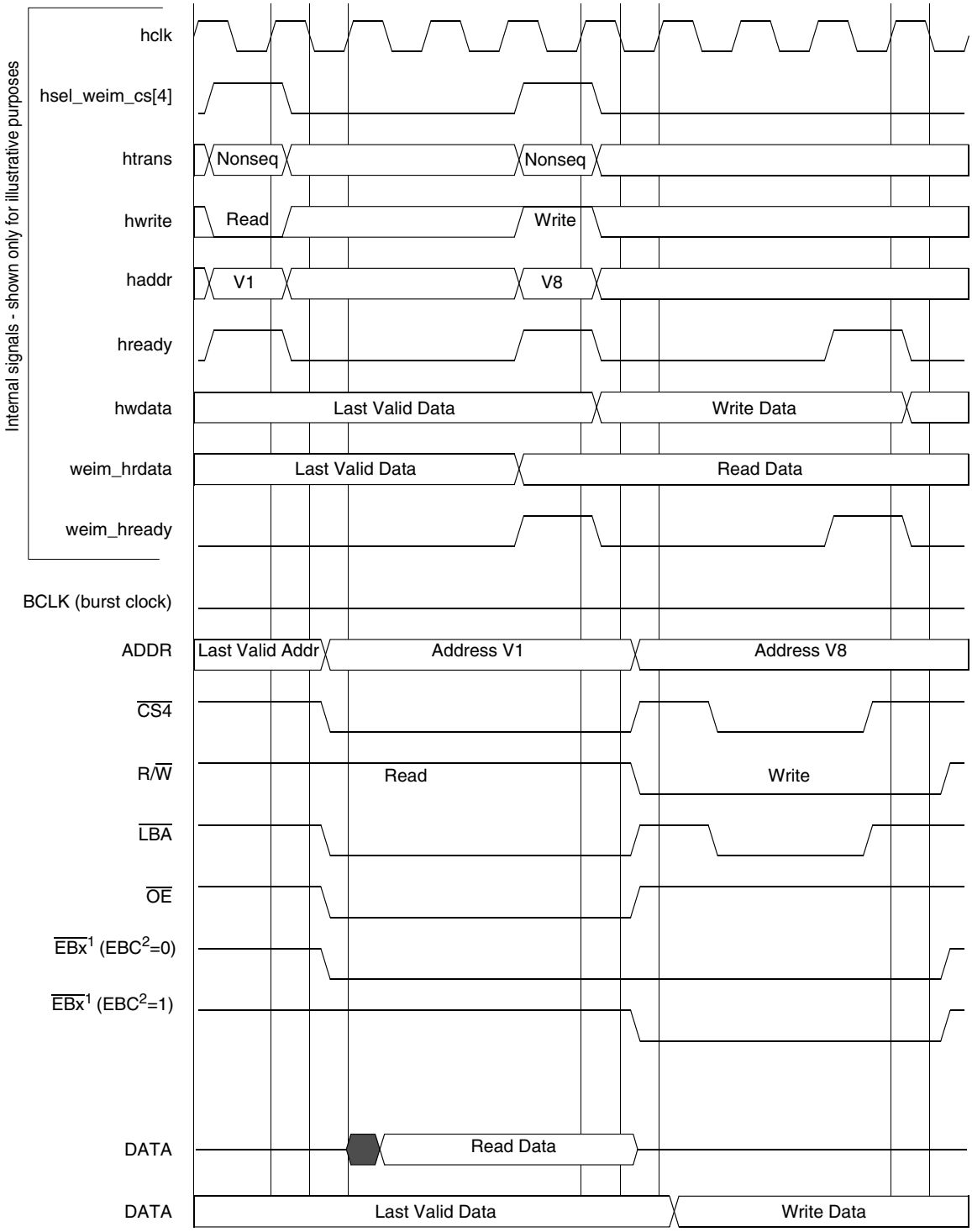

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF**



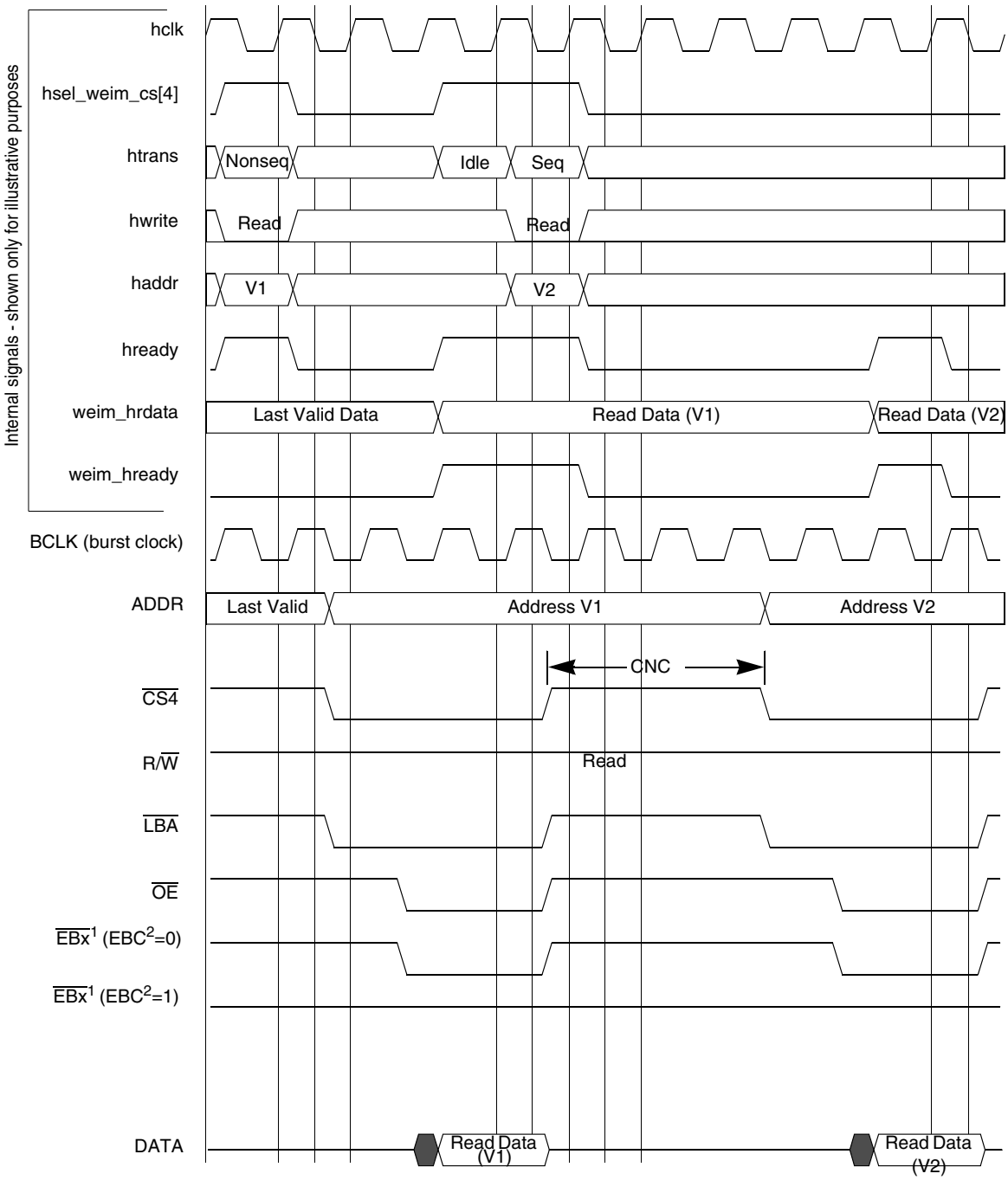

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF**



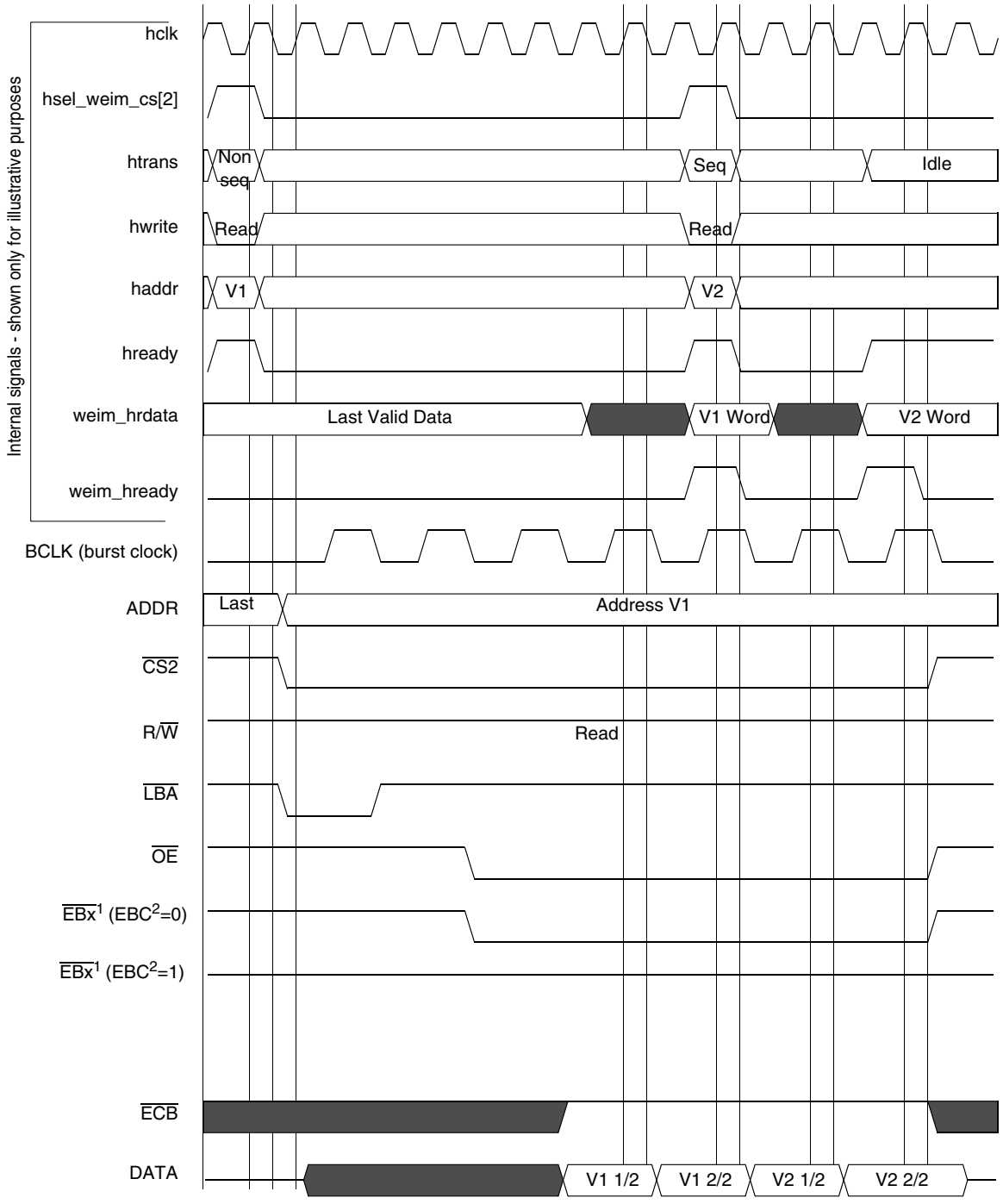

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 25. WSC = 3, CSA = 1, A.HALF/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF**

### 4.4.4 Non-TFT Panel Timing

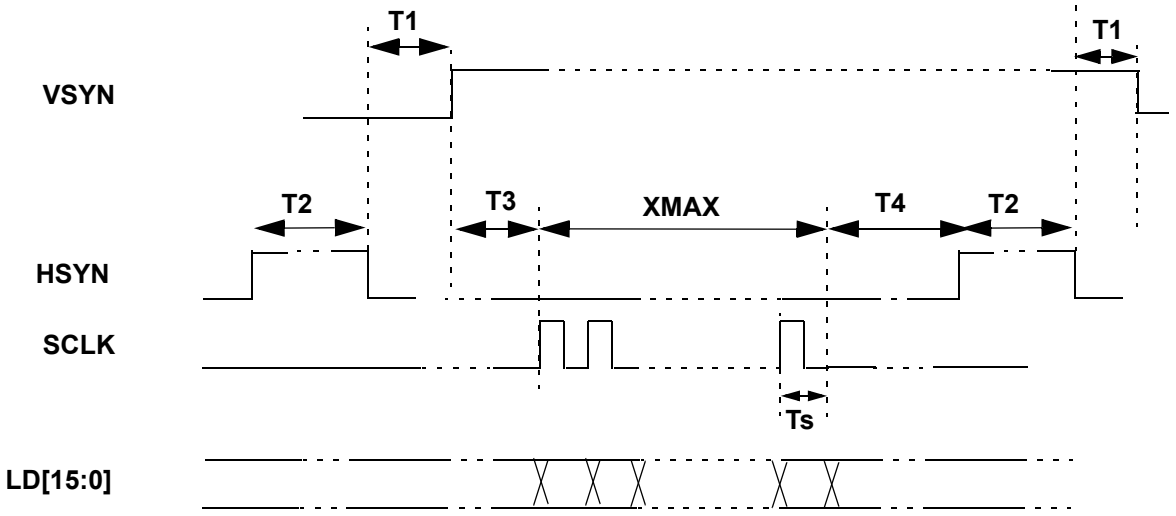



Figure 33. Non-TFT Panel Timing

Table 17. Non TFT Panel Timing Diagram

| Symbol | Parameter | Allowed Register Minimum Value[1, 2] | Actual Value | Unit |
|---|---|---|---|---|
| T1 | HSYN to VSYN delay[3] | 0 | HWAIT2+2 | Tpix[4] |
| T2 | HSYN pulse width | 0 | HWIDTH+1 | Tpix |
| T3 | VSYN to SCLK | – | 0 ≤ T3 ≤ Ts[5] | – |
| T4 | SCLK to HSYN | 0 | HWAIT1+1 | Tpix |

1 Maximum frequency of LCDC_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.

2 Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.

3 VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.

4 Tpix is the pixel clock period which equals LCDC_CLK period * (PCD + 1).

5 Ts is the shift clock period. Ts = Tpix * (panel data bus width).

## 4.5 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI\_RDY}$ signal (input). The SPI1 Sample Period Control Register (PERIODREG1) can also be programmed to a fixed data transfer rate. When the SPI module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, $\overline{SS}$ becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 34 through Figure 38 show the timing relationship of the master SPI using different triggering mechanisms.

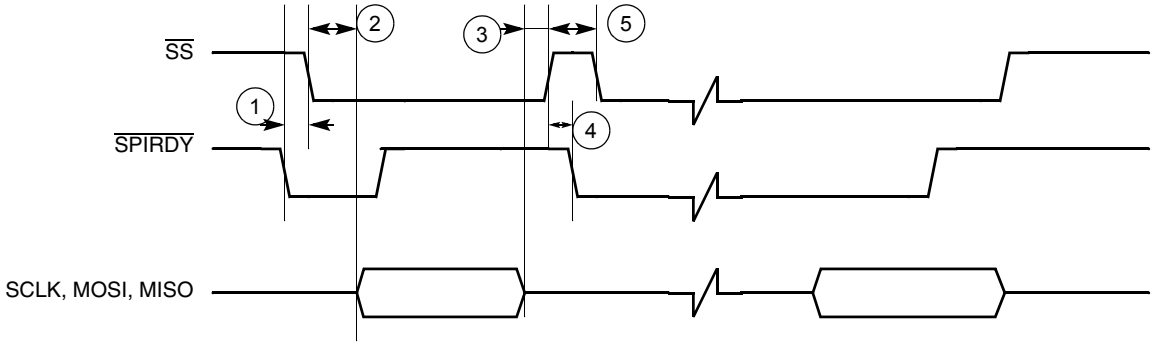



**Figure 34. Master SPI Timing Diagram Using SPI_RDY Edge Trigger**

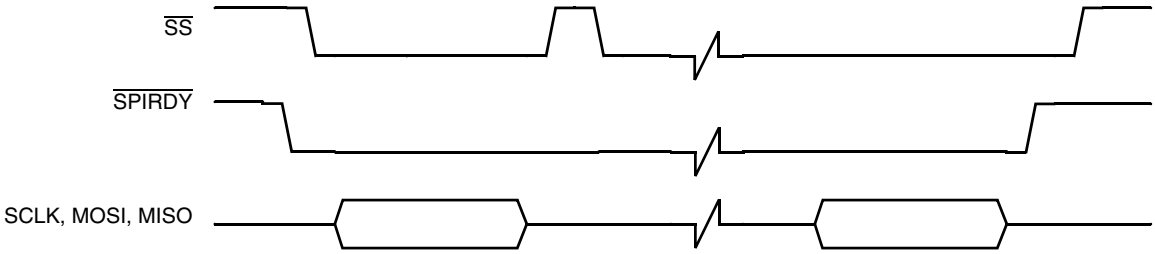



**Figure 35. Master SPI Timing Diagram Using SPI_RDY Level Trigger**

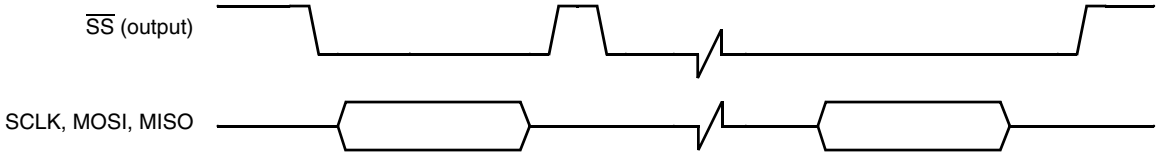



**Figure 36. Master SPI Timing Diagram Ignore SPI_RDY Level Trigger**

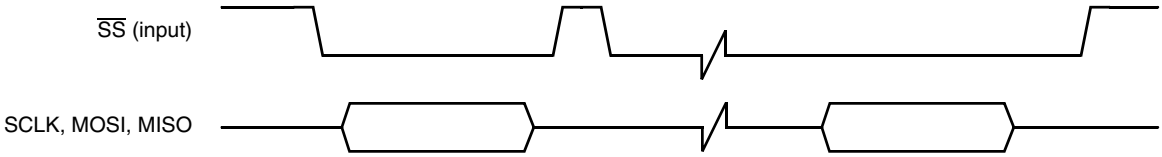



**Figure 37. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT**

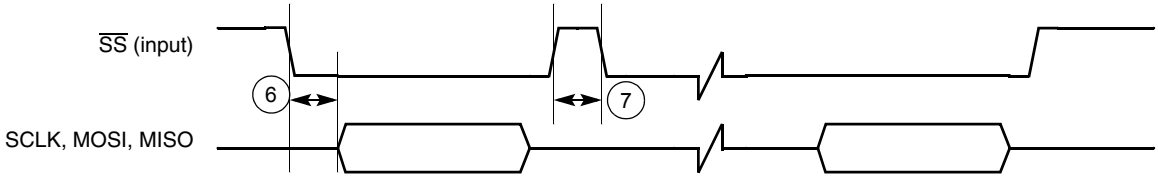



**Figure 38. Slave SPI Timing Diagram FIFO Advanced by SS Rising Edge**

**Table 18. Timing Parameter Table for Figure 34 through Figure 38**

| Ref No. | Parameter | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low | 2T[1] | – | ns |
| 2 | $\overline{\text{SS}}$ output low to first SCLK edge | 3 • Tsclk[2] | – | ns |
| 3 | Last SCLK edge to $\overline{\text{SS}}$ output high | 2 • Tsclk | – | ns |
| 4 | $\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low | 0 | – | ns |
| 5 | $\overline{\text{SS}}$ output pulse width | Tsclk + WAIT [3] | – | ns |
| 6 | $\overline{\text{SS}}$ input low to first SCLK edge | T | – | ns |
| 7 | $\overline{\text{SS}}$ input pulse width | T | – | ns |

1 T = CSPI system clock period (PERCLK2).
2 Tsclk = Period of SCLK.
3 WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

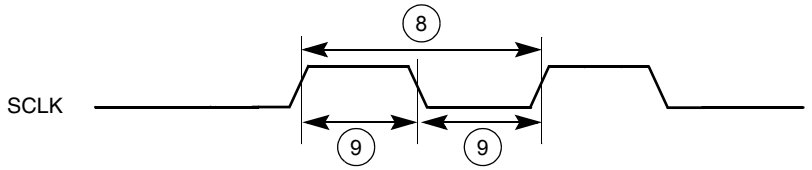



**Figure 39. SPI SCLK Timing Diagram**

**Table 19. Timing Parameter Table for SPI SCLK**

| Ref No. | Parameter | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 8 | SCLK frequency | 0 | 10 | MHz |
| 9 | SCLK pulse width | 100 | – | ns |

## 4.6 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *MC9328MXS Reference Manual*.

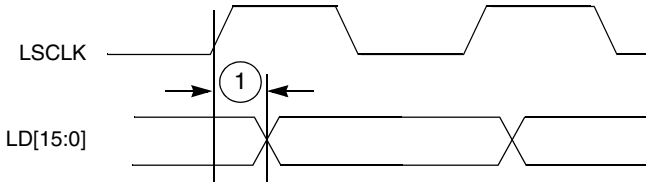
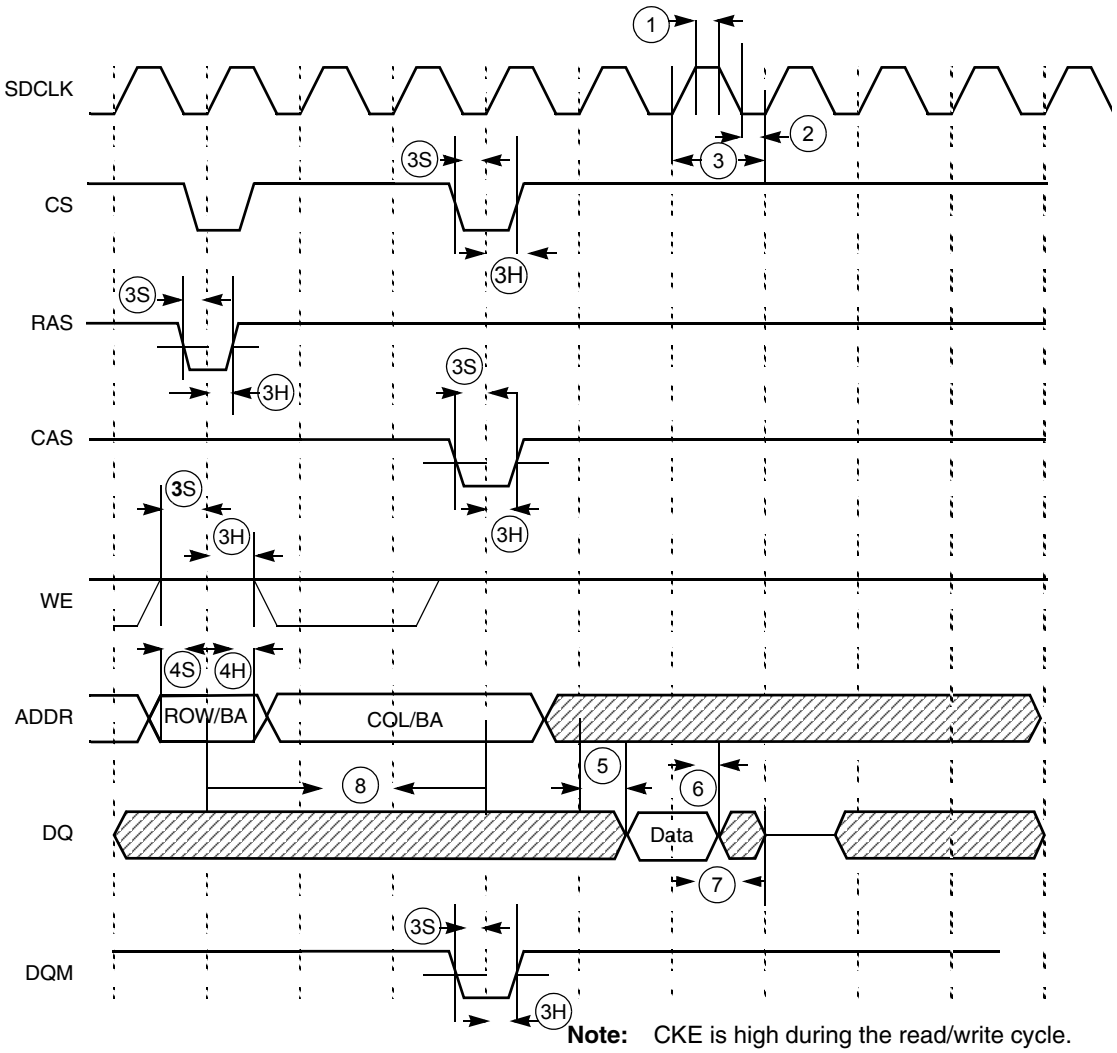



**Figure 40. SCLK to LD Timing Diagram**




**Note:** CKE is high during the read/write cycle.

**Figure 43. SDRAM Read Cycle Timing Diagram**

**Table 23. SDRAM Read Timing Parameter Table**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | SDRAM clock high-level width | 2.67 | – | 4 | – | ns |
| 2 | SDRAM clock low-level width | 6 | – | 4 | – | ns |
| 3 | SDRAM clock cycle time | 11.4 | – | 10 | – | ns |
| 3S | CS, RAS, CAS, WE, DQM setup time | 3.42 | – | 3 | – | ns |
| 3H | CS, RAS, CAS, WE, DQM hold time | 2.28 | – | 2 | – | ns |
| 4S | Address setup time | 3.42 | – | 3 | – | ns |
| 4H | Address hold time | 2.28 | – | 2 | – | ns |
| 5 | SDRAM access time (CL = 3) | – | 6.84 | – | 6 | ns |

**Table 26. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX) (Continued)**

| Ref No. | Parameter | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 5 | $t_{FEOPT}$; SE0 interval of EOP | 160.00 | 175.00 | ns |
| 6 | $t_{PERIOD}$; Data transfer rate | 11.97 | 12.03 | Mb/s |

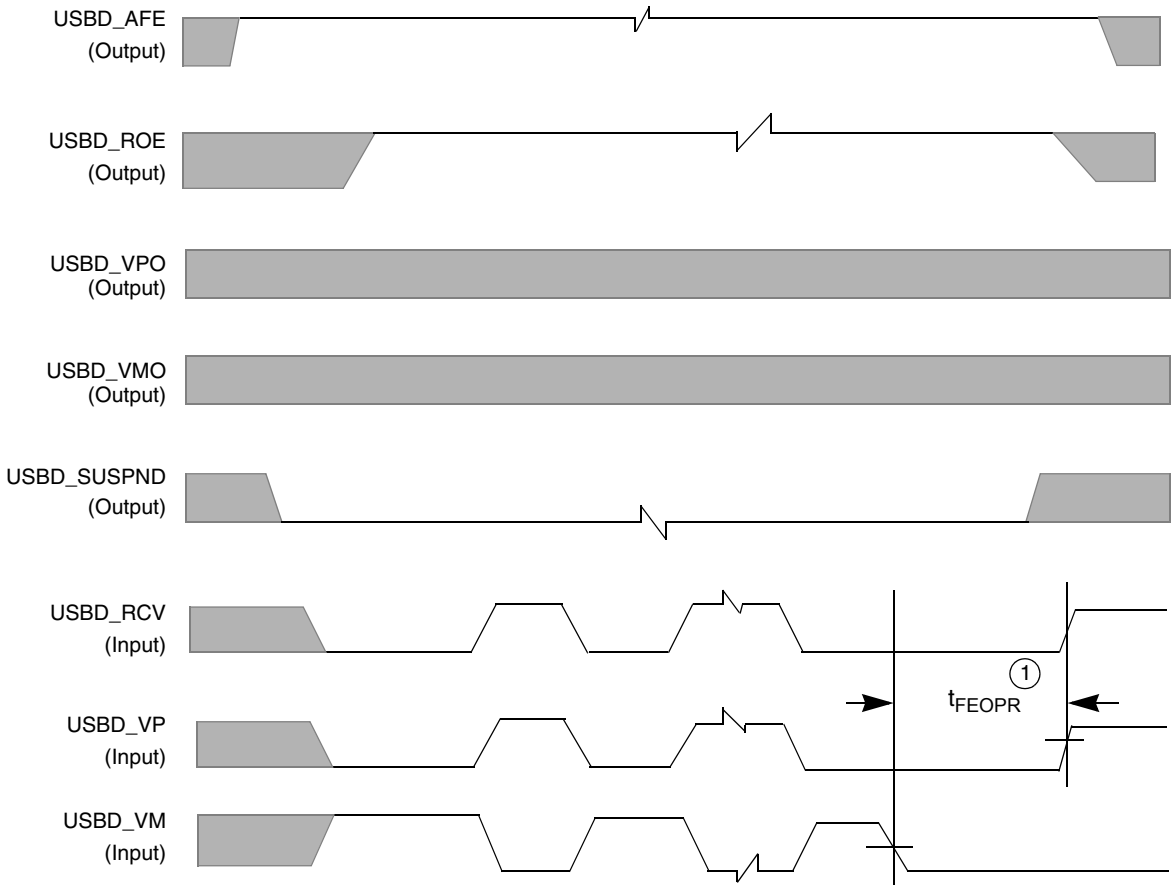


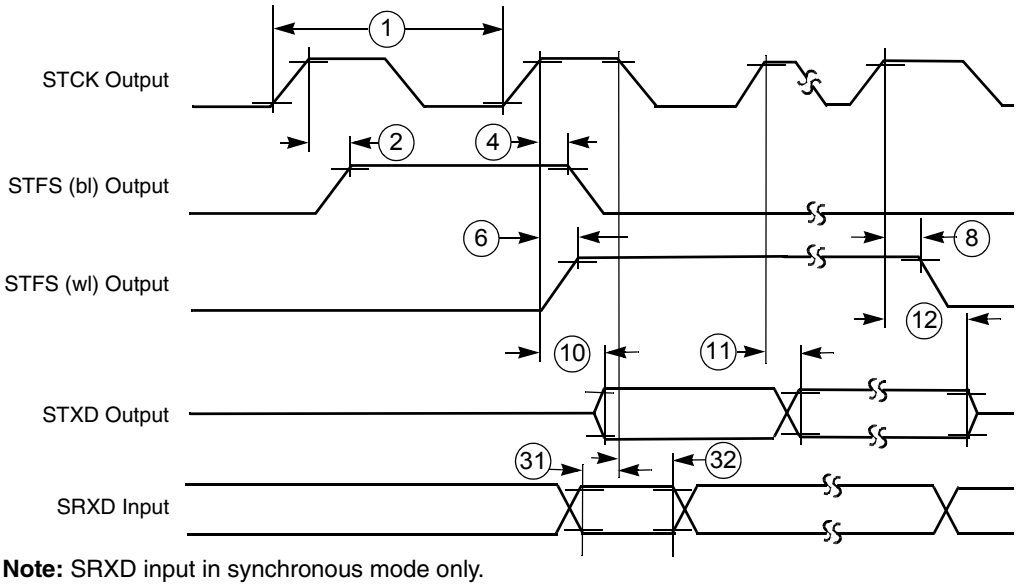

**Figure 48. USB Device Timing Diagram for Data Transfer from USB Transceiver (RX)**

**Table 27. USB Device Timing Parameter Table for Data Transfer from USB Transceiver (RX)**

| Ref No. | Parameter | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $t_{FEOPR}$; Receiver SE0 interval of EOP | 82 | – | ns |

## 4.10 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.




**Note:** SRXD input in synchronous mode only.

**Figure 50. SSI Transmitter Internal Clock Timing Diagram**

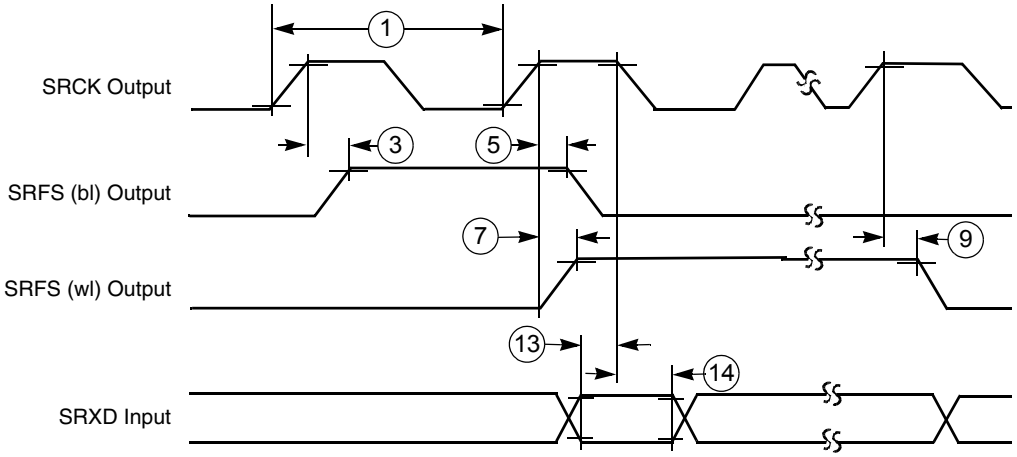



**Figure 51. SSI Receiver Internal Clock Timing Diagram**