Renesas Electronics America Inc - UPD78F1500AGC-GAD-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1500agc-gad-ax

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
78K0R/Lx3 User's Manual Hardware	This manual
78K0R Microcontrollers Instructions User's Manual	R01US0029E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
CC78K0R Ver. 2.00 C Compiler	Operation	U18549E
	Language	U18548E
RA78K0R Ver. 1.20 Assembler Package	Operation	U18547E
	Language	U18546E
SM+ System Simulator	Operation	U18601E
	User Open Interface	U18212E
PM+ Ver. 6.30		U18416E
ID78K0R-QB Ver. 3.20 Integrated Debugger	Operation	U17839E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
QB-78K0RLX3 In-Circuit Emulator	U19336E
QB-MINI2 On-Chip Debug Emulator with Programming Function	U18371E

Documents Related to Flash Memory Programming (User's Manuals)

Document Name		Document No.
PG-FP5 Flash Memory Programmer		R20UT0008E
QB-Programmer Programming GUI	Operation	U18527E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

(2) Non-port functions (2/4) : 78K0R/LG3

Function Name	I/O	Function	After Reset	Alternate Function
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output	–
COM4 to COM7				SEG0 to SEG3
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
V_{LC3}			Input port	P02
CAPH	–	Connecting a capacitor for LCD controller/driver	Input port	P00
CAPL				P01
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P30/TI03/TO00/ RTC1HZ
INTP2				P31/TI00/TO03/ RTCDIV/RTCCL/ PCLBUZ1
INTP3				P33/TI07/TO07
INTP4				P14/SI10/RxD1/ SDA10
INTP5				P32/TI01/TO01/ PCLBUZ0
INTP6				P11/SI20/RxD2/ SDA20
INTP7				P15/$\overline{\text{SCK10}}$/SCL10
INTP8				P34/TI06/TO06
INTP9				P81/RxD0/SI00
INTP10				P16/TI05/TO05
INTP11				P80/$\overline{\text{SCK00}}$
PCLBUZ0	Output	Clock output/buzzer output	Input port	P32/TI01/TO01/ INTP5
PCLBUZ1				P31/TI00/TO03/ RTCDIV/RTCCL/INTP2
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P31/TI00/TO03/ PCLBUZ1/RTCCL/ INTP2
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P31/TI00/TO03/ PCLBUZ1/RTCDIV/ INTP2
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/TI03/TO00/ INTP1
$\overline{\text{RESET}}$	Input	System reset input	–	–

2.2 Description of Pin Functions

Remark The pins mounted depend on the product. Refer to **1.3 Pin Configuration (Top View)** and **2.1 Pin Function List**.

2.2.1 P00 to P02

P00 to P02 function as an I/O port. This port can also be used for connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P00/CAPH	√		
P01/CAPL	√		
P02/V_{LC3}	√		

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 to P02 function as an I/O port. P00 to P02 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P02 function as connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

(a) CAPH, CAPL

These are the pins for connecting a capacitor for LCD controller/driver.

(b) V_{LC3}

This is the pin for inputting a power supply voltage pin for driving the LCD.

Caution To use P00/CAPH, P01/CAPL, and P02/V_{LC3} as a general-purpose port, set bit 5 (MDSET1) and bit 4 (MDSET0) of LCD mode register (LCDMD) to "0", which is the same as their default status setting.

2.2.14 P130

P130 functions as an output port.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P130	√		

Remark The P130 pin outputs a low level when it is used as a port function pin and a reset is effected. If P130 is set to output a high level before reset is effected, the output signal of P130 can be dummy-output as the CPU reset signal (see the figure for **Remark** in **4.2.14 Port 13**).

2.2.15 P140 to P147

P140 to P147 function as an I/O port. This port can also be used for segment output of LCD controller/driver.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P140/SEGxx	√ (xx = 19)	√ (xx = 23)	√ (xx = 37)
P141/SEGxx	√ (xx = 18)	√ (xx = 22)	√ (xx = 36)
P142/SEGxx	√ (xx = 17)	√ (xx = 21)	√ (xx = 35)
P143/SEGxx	√ (xx = 16)	√ (xx = 20)	√ (xx = 34)
P144/SEGxx	√ (xx = 15)	√ (xx = 19)	√ (xx = 33)
P145/SEGxx	√ (xx = 14)	√ (xx = 18)	√ (xx = 32)
P146/SEGxx	√ (xx = 13)	√ (xx = 17)	√ (xx = 31)
P147/SEGxx	√ (xx = 12)	√ (xx = 16)	√ (xx = 30)

The following operation modes can be specified in 1-bit units.

(1) Port mode

P140 to P147 function as an I/O port. P140 to P147 can be set to input or output port in 1-bit units using port mode register 14 (PM14). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 14 (PU14).

(2) Control mode

P140 to P147 function as segment output of LCD controller/driver (SEGxx).

Figure 2-1. Pin I/O Circuit List (1/5)

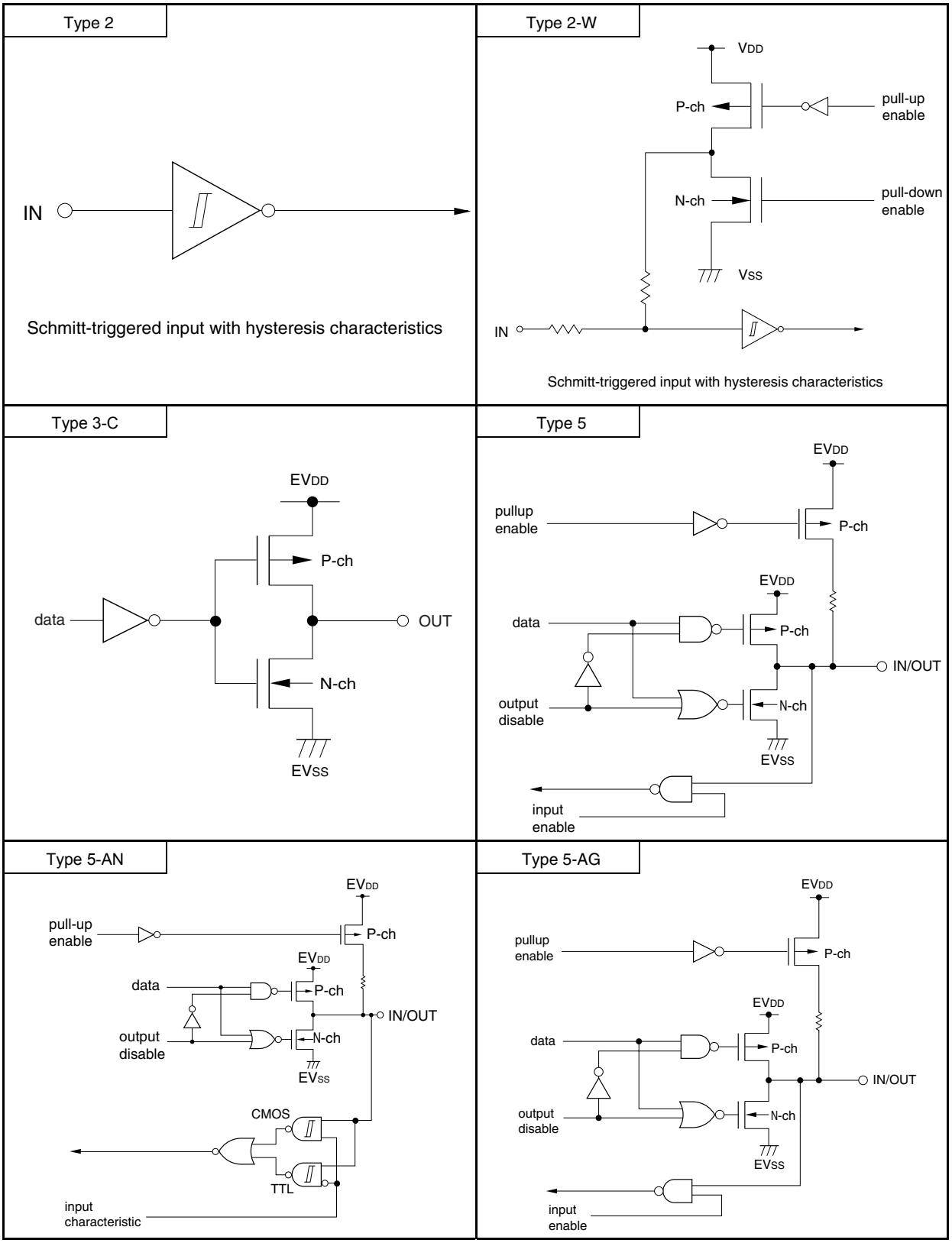


Table 3-6. Extended SFR (2nd SFR) List (5/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
					1-bit	8-bit	16-bit				
F01A6H	Timer status register 03	TSR03L	TSR03	R	–	√	√	0000H	√	√	√
F01A7H		–			–	–			√	√	√
F01A8H	Timer status register 04	TSR04L	TSR04	R	–	√	√	0000H	√	√	√
F01A9H		–			–	–			√	√	√
F01AAH	Timer status register 05	TSR05L	TSR05	R	–	√	√	0000H	–	√	√
F01ABH		–			–	–			–	√	√
F01ACH	Timer status register 06	TSR06L	TSR06	R	–	√	√	0000H	–	√	√
F01ADH		–			–	–			–	√	√
F01AEH	Timer status register 07	TSR07L	TSR07	R	–	√	√	0000H	√	√	√
F01AFH		–			–	–			√	√	√
F01B0H	Timer channel enable status register 0	TE0L	TE0	R	√	√	√	0000H	√	√	√
F01B1H		–			–	–			√	√	√
F01B2H	Timer channel start register 0	TS0L	TS0	R/W	√	√	√	0000H	√	√	√
F01B3H		–			–	–			√	√	√
F01B4H	Timer channel stop register 0	TT0L	TT0	R/W	√	√	√	0000H	√	√	√
F01B5H		–			–	–			√	√	√
F01B6H	Timer clock select register 0	TPS0L	TPS0	R/W	–	√	√	0000H	√	√	√
F01B7H		–			–	–			√	√	√
F01B8H	Timer output register 0	TO0L	TO0	R/W	–	√	√	0000H	√	√	√
F01B9H		–			–	–			√	√	√
F01BAH	Timer output enable register 0	TOE0L	TOE0	R/W	√	√	√	0000H	√	√	√
F01BBH		–			–	–			√	√	√
F01BCH	Timer output level register 0	TOL0L	TOL0	R/W	–	√	√	0000H	√	√	√
F01BDH		–			–	–			√	√	√
F01BEH	Timer output mode register 0	TOM0L	TOM0	R/W	–	√	√	0000H	√	√	√
F01BFH		–			–	–			√	√	√
F01C0H	Timer counter register 10	TCR10		R	–	–	√	FFFFH	√	√	√
F01C1H											
F01C2H	Timer counter register 11	TCR11		R	–	–	√	FFFFH	√	√	√
F01C3H											
F01C4H	Timer counter register 12	TCR12		R	–	–	√	FFFFH	√	√	√
F01C5H											
F01C6H	Timer counter register 13	TCR13		R	–	–	√	FFFFH	√	√	√
F01C7H											
F01C8H	Timer mode register 10	TMR10		R/W	–	–	√	0000H	√	√	√
F01C9H											
F01CAH	Timer mode register 11	TMR11		R/W	–	–	√	0000H	√	√	√
F01CBH											
F01CCH	Timer mode register 12	TMR12		R/W	–	–	√	0000H	√	√	√
F01CDH											

Table 4-11. Settings of Port Mode Register and Output Latch When Using Alternate Function (4/5)

LF3	LG3	LH3	Pin Name	Alternate Function		PFALL	ISC	PM××	P××
				Function Name	I/O	(PFxxx)	(ISCx)		
–	–	√	P86	TI12	Input	–	–	1	×
				TO12	Output	–	–	0	0
–	–	√	P87	TI13	Input	–	–	1	×
				TO13	Output	–	–	0	0
√	√	√	P110, P111	ANO0, ANO1	Output	–	–	0	×
√	√	√	P120	INTP0[Note 1]	Input	–	ISC0 = 0	1	×
				EXLVI[Note 1]	Input	–	–	1	×
√	√	√	P121	X1[Note 1]	–	–	–	×	×
√	√	√	P122	X2[Note 1]	–	–	–	×	×
				EXCLK[Note 1]	Input	–	–	×	×
√	√	√	P123	XT1[Note 1]	–	–	–	×	×
√	√	√	P124	XT2[Note 1]	–	–	–	×	×
–	√	√	P150[Note 2]	ANI8	Input	–	–	1	×
				AMP2+	Input	–	–	1	×
–	√	√	P151, P152[Note 2]	ANI9, ANI10	Input	–	–	1	×
√	√	√	P157[Note 2]	ANI15	Input	–	–	1	×
				AV_{REFM}	Input	–	–	1	×

Notes 1. To use the P121 to P124 pins for main system clock resonator connection (X1, X2), subsystem clock resonator connection (XT1, XT2), or main system clock external clock input (EXCLK), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set, respectively, by using the clock operation mode control register (CMC). CMC can be written only once after reset release (for details, refer to **5.3 (1) Clock operation mode control register (CMC)**). The reset value of CMC is 00H (both P121 to P124 are input port pins).

2. The P150/ANI8/AMP2+, P151/ANI9, P152/ANI10, P157/ANI15/AV_{REFM} pins are as shown below depending on the settings of the A/D port configuration register (ADPC), port mode register 2 (PM2), analog input channel specification register (ADS), operational amplifier control register (OAC), and analog reference voltage control register (ADVRC). Refer to **4.2.16 Port 15**.

Remark ×: don't care
–: Not applicable
PFALL: Port function register
ISC: Input switch control register
PM××: Port mode register
P××: Port output latch

8.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 8-1. Configuration of Watchdog Timer

Item	Configuration
Control register	Watchdog timer enable register (WDTE)

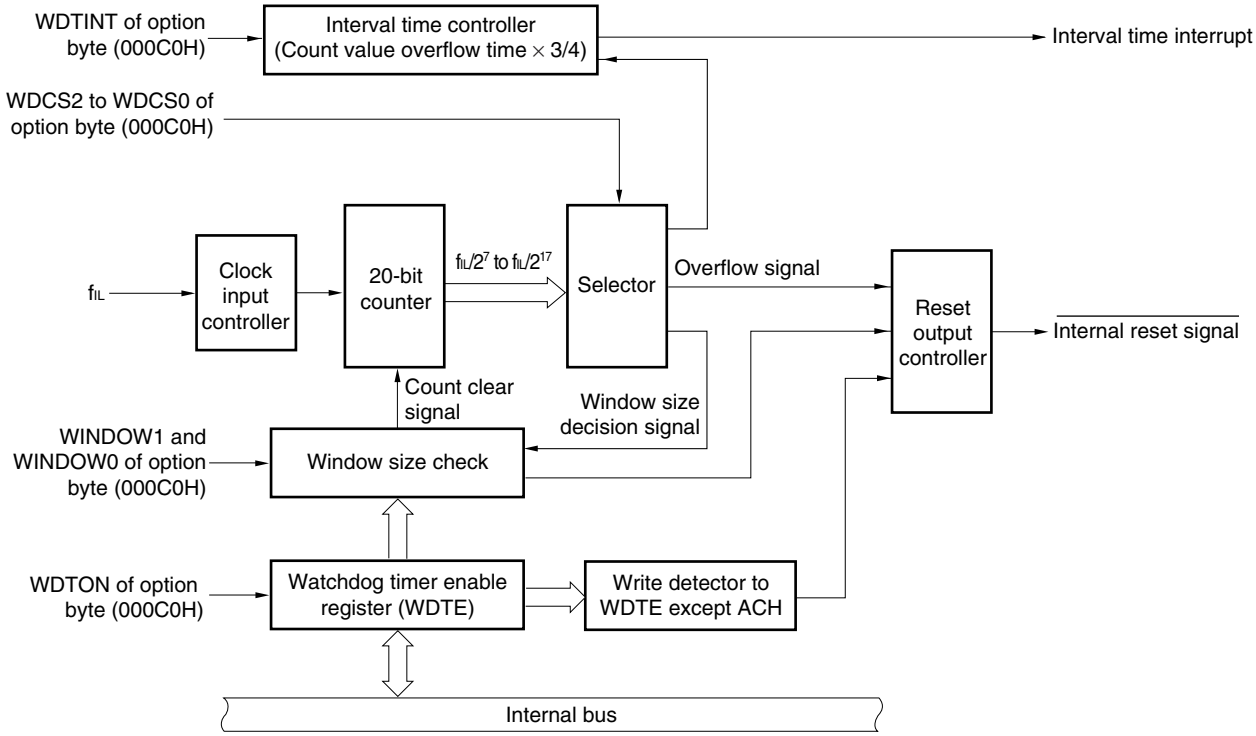
How the counter operation is controlled, overflow time, window open period, and interval interrupt are set by the option byte.

Table 8-2. Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (000C0H)
Watchdog timer interval interrupt	Bit 7 (WDTINT)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)
Controlling counter operation of watchdog timer (in HALT/STOP mode)	Bit 0 (WDSTBYON)

Remark For the option byte, see **CHAPTER 26 OPTION BYTE**.

Figure 8-1. Block Diagram of Watchdog Timer



14.5.4 Slave transmission

Slave transmission is that the 78K0R/Lx3 microcontrollers transmit data to another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	$\overline{SCK00}$, SO00	$\overline{SCK01}$, SO01	$\overline{SCK10}$, SO10	$\overline{SCK20}$, SO20
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.			
Error detection flag	Overrun error detection flag (OVFmn) only			
Transfer data length	7 or 8 bits			
Transfer rate	Max. f_{MCK}/6 [MHz]Notes 1, 2			
Data phase	Selectable by DAPmn bit • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.			
Clock phase	Selectable by CKPmn bit • CKPmn = 0: Forward • CKPmn = 1: Reverse			
Data direction	MSB or LSB first			

Notes 1. Because the external serial clock input to pins $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, and $\overline{SCK20}$ is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [MHz].

2. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 31 ELECTRICAL SPECIFICATIONS**).

Remarks 1. f_{MCK}: Operation clock (MCK) frequency of target channel

2. For 78K0R/LF3, CSI00 and CSI01 are not mounted.

3. For 78K0R/LG3, CSI01 is not mounted.

14.7.2 Data transmission

Data transmission is an operation to transmit data to the target for transfer (slave) after transmission of an address field. After all data are transmitted to the slave, a stop condition is generated and the bus is released.

Simplified I^2C	IIC10	IIC20
Target channel	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL10, SDA10 Note	SCL20, SDA20 Note
Interrupt	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)	
Error detection flag	Parity error detection flag (PEFmn)	
Transfer data length	8 bits	
Transfer rate	Max. f_{CLK}/4 [MHz] (SDRmn [15:9] = 1 or more) f_{CLK}: System clock frequency However, the following condition must be satisfied in each mode of I^2C. • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)	
Data level	Forward output (default: high level)	
Parity bit	No parity bit	
Stop bit	Appending 1 bit (for ACK reception timing)	
Data direction	MSB first	

Note To perform communication via simplified I^2C, set the data I/O pins (SDA10, SDA20) in the N-ch open-drain output (V_{DD} tolerance) mode (POM14 = 1, POM11 = 1) by using the port output mode register 1 (POM1) (see **4.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM15 = 1, POM10 = 1) also for the clock input/output pins (SCL10, SCL20) (see **4.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

Table 14-8. Relationship between register settings and pins (Channel 3 of unit 0: UART1 reception)

SE03 Note1	MD032	MD031	TXE03	RXE03	PM14 Note2	P14 Note2	Operation mode	Pin Function
								RxD1/SI10/SDA10/INTP4/P14 Note2
0	0	1	0	0	× Note3	× Note3	Operation stop mode	SI10/SDA10/INTP4/P14 Note2
1	0	1	0	1	1	×	UART1 reception Note4, 5	RxD1

Notes 1. The SE0 register is a read-only status register which is set using the SS0 and ST0 registers.

2. When channel 3 of unit 0 is set to UART1 reception, this pin becomes an RxD1 function pin. In this case, set channel 2 of unit 0 to operation stop mode or UART1 transmission (refer to **Table 14-7**).
When channel 2 of unit 0 is set to CSI10 or IIC10, this pin cannot be used as an RxD1 function pin. In this case, set channel 3 of unit 0 to operation stop mode.

3. This pin can be set as a port function pin.

4. When using UART1 transmission and reception in a pair, set channel 2 of unit 0 to UART1 transmission (refer to **Table 14-7**).

5. The SMR02 register of channel 2 of unit 0 must also be set during UART1 reception. For details, refer to **14.5.2 (1) Register setting**.

Remark X: Don't care

Table 14-11. Relationship between register settings and pins (Channel 2 of unit 1: UART3 transmission)

SE12 Note1	MD122	MD121	SOE12	SO12	TXE12	RXE12	PM51	P51	Operation mode	Pin Function
										TxD3/SEG52/P51
0	0	1	0	1	0	0	× Note2	× Note2	Operation stop mode	SEG52/P51
1	0	1	1	0/1 Note3	1	0	0	1	UART3 transmission Note4	TxD3

Notes 1. The SE1 register is a read-only status register which is set using the SS1 and ST1 registers.

2. This pin can be set as a port function pin.

3. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

4. When using UART3 transmission and reception in a pair, set channel 3 of unit 1 to UART3 reception (refer to **Table 14-12**).

Remark X: Don't care

Table 14-12. Relationship between register settings and pins (Channel 3 of unit 1: UART3 reception)

SE13 Note1	MD132	MD131	TXE13	RXE13	PM50	P50	Operation mode	Pin Function
								RxD3/SEG53/P50
0	0	1	0	0	× Note2	× Note2	Operation stop mode	SEG53/P50
1	0	1	0	1	1	×	UART3 reception Note3, 4	RxD3

Notes 1. The SE1 register is a read-only status register which is set using the SS1 and ST1 registers.

2. This pin can be set as a port function pin.

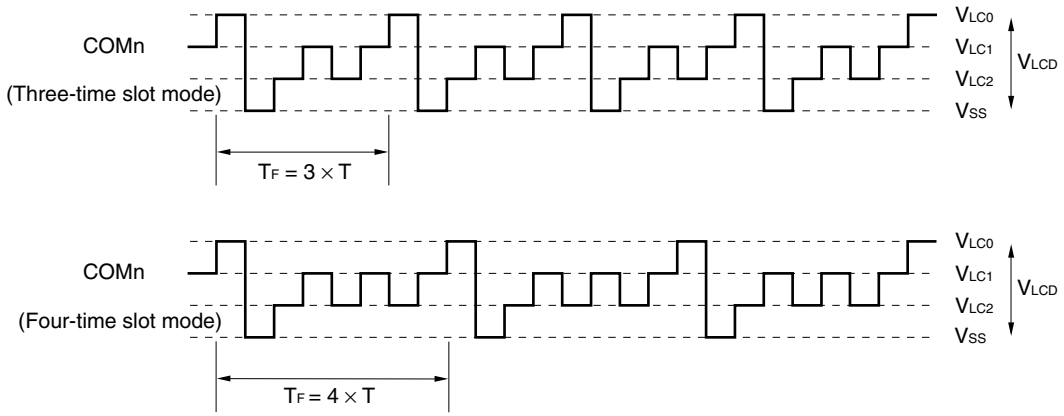
3. When using UART3 transmission and reception in a pair, set channel 2 of unit 1 to UART3 transmission (refer to **Table 14-11**).

4. The SMR12 register of channel 2 of unit 1 must also be set during UART3 reception. For details, refer to **14.5.2 (1) Register setting**.

Remark X: Don't care

Figure 16-13. Common Signal Waveforms (2/2)

(c) 1/3 bias method



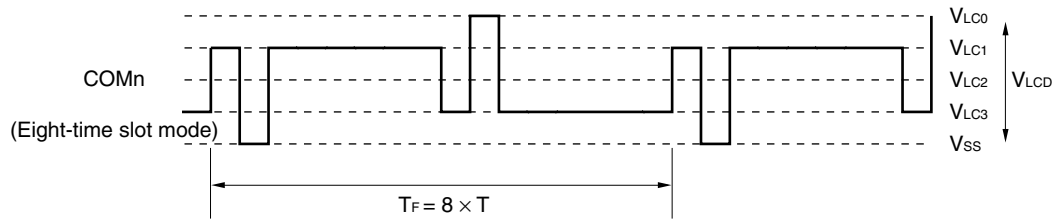
T: One LCD clock period T_F: Frame frequency

< Example of calculation of LCD frame frequency (When four-time slot mode is used) >

LCD clock: $32768/2^8$ = 256 Hz (When setting to LCDC0 = 04H)

LCD frame frequency: 64 Hz

(d) 1/4 bias method



T: One LCD clock period T_F: Frame frequency

< Example of calculation of LCD frame frequency (When eight-time slot mode is used) >

LCD clock: $32768/2^8$ = 256 Hz (When setting to LCDC0 = 04H)

LCD frame frequency: 32 Hz

Figure 19-8. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (78K0R/LF3) (2/2)

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01H	TMPR004	SREPR02	SRPR02	CSIPR020 IICPR020 STPR02	1	RTCIPR0	RTCPR0	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11H	TMPR104	SREPR12	SRPR12	CSIPR120 IICPR120 STPR12	1	RTCIPR1	RTCPR1	ADPR1

Address: FFFD8H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR02L	1	1	1	PPR07	PPR06	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR12L	1	1	1	PPR17	PPR16	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	0
PR02H	1	1	MDPR0	TMPR013	TMPR012	TMPR011	TMPR010	1

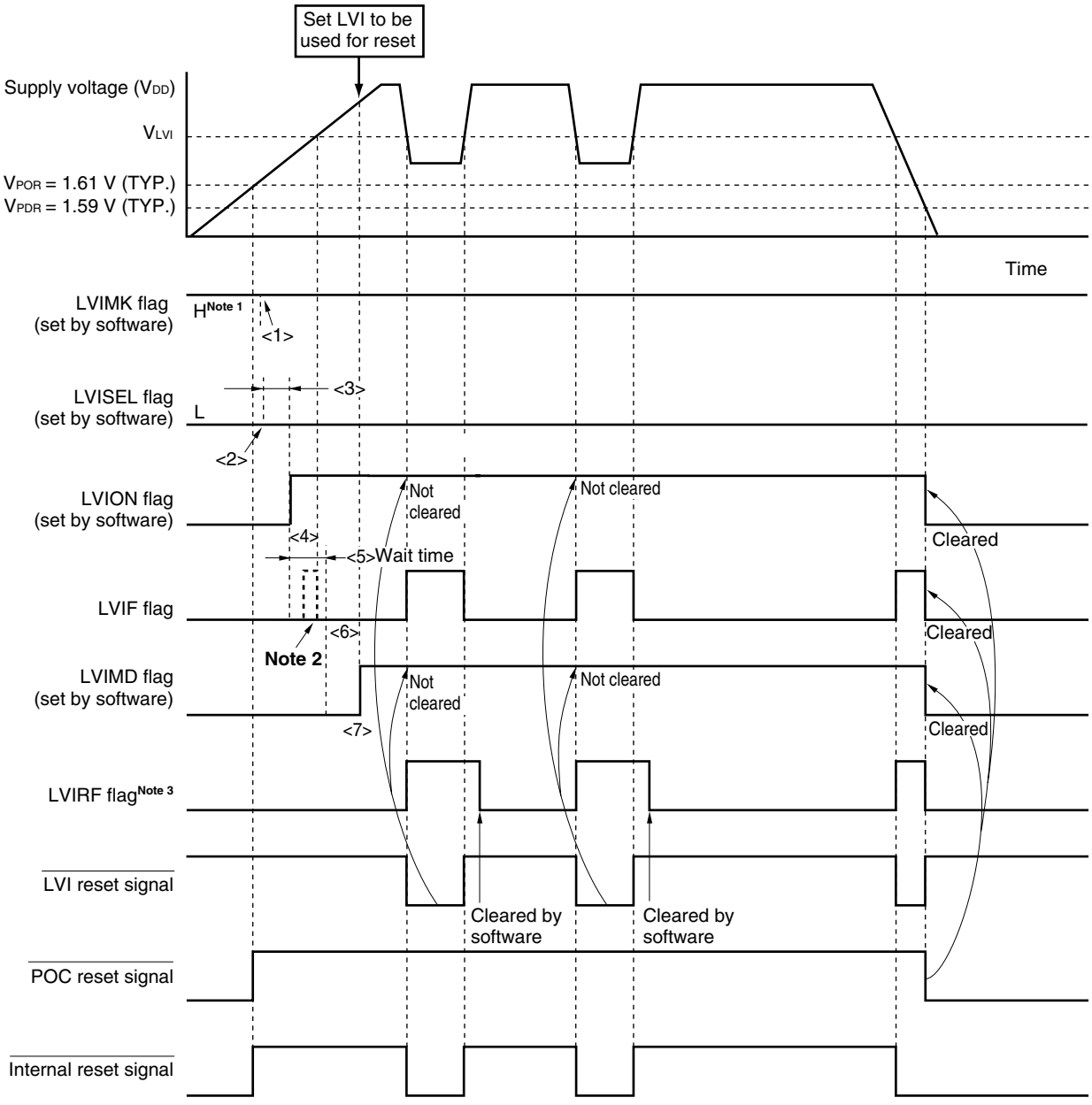
Address: FFFDDH After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	0
PR12H	1	1	MDPR1	TMPR113	TMPR112	TMPR111	TMPR110	1

XXPR1X	XXPR0X	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Caution Be sure to set bit 3 of PR01H and PR11H, bits 5 to 7 of PR02L and PR12L, bits 0, 6, 7 of PR02H and PR12H to 1.

Figure 24-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

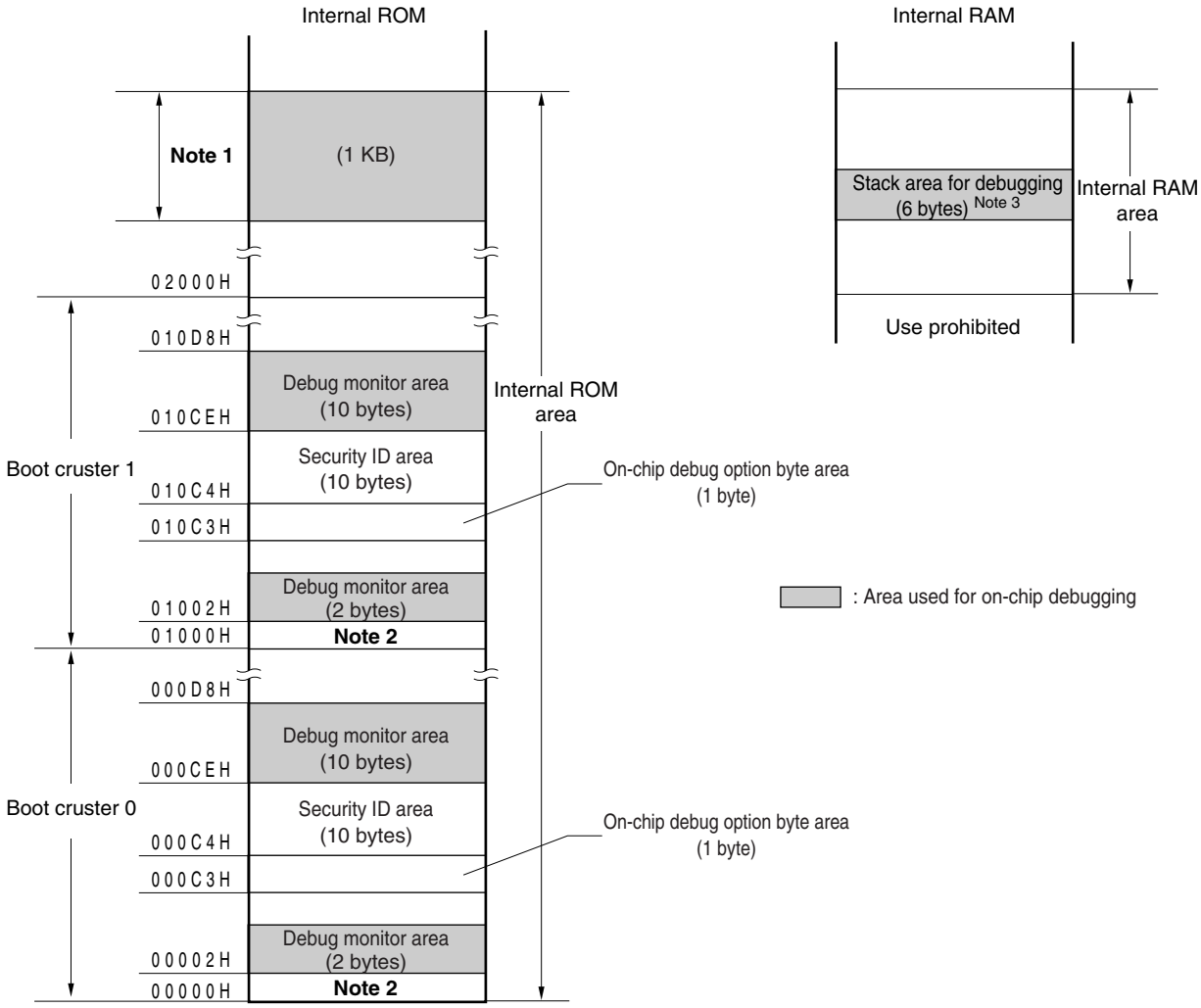
2. The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 22 RESET FUNCTION**.

Remarks 1. <1> to <7> in Figure 24-5 above correspond to <1> to <7> in the description of "When starting operation" in **24.4.1 (1) (a) When LVI default start function stopped is set (LVIOFF = 1).**

2. V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

Figure 28-2. Memory Spaces Where Debug Monitor Programs Are Allocated



Notes 1. Address differs depending on products as follows.

Products	Internal ROM	Address
<R> μPD78F1500A, 78F1503A, 78F1506A, 78F1510A, 78F1513A, 78F1516A	64 KB	0FC00H to 0FFFFH
μPD78F1501A, 78F1504A, 78F1507A	96 KB	17C00H to 17FFFH
<R> μPD78F1502A, 78F1505A, 78F1508A, 78F1512A, 78F1515A, 78F1518A	128 KB	1FC00H to 1FFFFH

2. In debugging, reset vector is rewritten to address allocated to a monitor program.

3. Since this area is allocated immediately before the stack area, the address of this area varies depending on the stack increase and decrease. That is, 6 extra bytes are consumed for the stack area used.

For details of the way to secure of the memory space, refer to the **QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E)**.

LCD Characteristics (4/4)

(3) Capacitor split method

- **1/3 bias method (T_A = –40 to +85°C, 2.2 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{LC0} voltage	V_{LC0}	C1 to C4 = 0.47 μF[Note 3]		V_{DD}		V
V_{LC1} voltage	V_{LC1}	C1 to C4 = 0.47 μF[Note 3]	2/3 V_{LC0} –0.1	2/3 V_{LC0}	2/3 V_{LC0} +0.1	V
V_{LC2} voltage	V_{LC2}	C1 to C4 = 0.47 μF[Note 3]	1/3 V_{LC0} –0.1	1/3 V_{LC0}	1/3 V_{LC0} +0.1	V
Capacitor split wait time[Note 1]	t_{VAWAIT}		100			ms
LCD output resistor[Note 2] (Common)	R_{ODC}	I_O = ±5 μA			40	kΩ
LCD output resistor[Note 2] (Segment)	R_{OCS}	I_O = ±1 μA			200	kΩ

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. The output resistor is a resistor connected between one of the V_{LC0}, V_{LC1}, V_{LC2} and V_{SS} pins, and either of the SEG and COM pins.

3. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{LC0} and GND
C3: A capacitor connected between V_{LC1} and GND
C4: A capacitor connected between V_{LC2} and GND
C1 = C2 = C3 = C4 = 0.47 pF±30 %

R

S

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 6	Soft	Timer array unit	TMRmn: Timer mode register mn	Be sure to clear bits 14, 13, 5, and 4 to “0”.	pp.264 to 266 ☐
				Channel 5 of timer array unit 0 and channels 0 to 3 of timer array unit 1 of the 78K0R/LF3 can be set only to the interval mode.	pp.266, 271 ☐
				Channel 6 of timer array unit 0 of the 78K0R/LF3 can be set only to the interval mode and one-count mode (when using as master).	pp.266, 271 ☐
				Channels 0 to 3 of timer array unit 1 of the 78K0R/LG3 can be set only to the interval mode.	pp.266, 271 ☐
			TSm: Timer channel start register m	Be sure to clear bits 15 to 8 of TS0 and bits 15 to 4 of TS1 to “0”.	p.270 ☐
			Start Timing (In Interval Timer Mode)	In the first cycle operation of count clock after writing TSmn, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDmn0 = 1.	p.272 ☐
			Start Timing (In Capture Mode)	In the first cycle operation of count clock after writing TSpq, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDpq0 = 1.	p.273 ☐
			Start Timing (In One-count Mode and In Capture & One-count Mode)	An input signal sampling error is generated since operation starts upon start trigger detection (The error is one count clock when TIpq is used).	pp.275, 276 ☐
			TTm: Timer channel stop register m	Be sure to clear bits 15 to 8 of TT0 and bits 15 to 4 of TT1 to “0”.	p.277 ☐
			TISp: Timer input select register p	When the LIN-bus communication function is used, select the input signal of the RxD3 pin by setting ISC1 to 1 and TIS07 = 0.	p.279 ☐
			TOEp: Timer output enable register p	For 78K0R/LF3, be sure to clear bits 15 to 8, 6 and 5 of TOE0 to “0”.	p.279 ☐
				For 78K0R/LG3, be sure to clear bits 15 to 8 of TOE0 to “0”.	p.279 ☐
				For 78K0R/LH3, be sure to clear bit 15 to 8 of TOE0, bits 15 to 4 of TOE1 to “0”.	p.279 ☐
			TOp: Timer output register p	For 78K0R/LF3, be sure to clear bits 15 to 8, 6 and 5 of TO0 to “0”.	p.280 ☐
				For 78K0R/LG3, be sure to clear bits 15 to 8 of TO0 to “0”.	p.280 ☐
				For 78K0R/LH3, be sure to clear bit 15 to 8 of TO0, bits 15 to 4 of TO1 to “0”.	p.280 ☐
			TOLp: Timer output level register p	For 78K0R/LF3, be sure to clear bits 15 to 8, 6 and 5 of TOL0 to “0”.	p.281 ☐
				For 78K0R/LG3, be sure to clear bits 15 to 8 of TOL0 to “0”.	p.281 ☐
				For 78K0R/LH3, be sure to clear bit 15 to 8 of TOL0, bits 15 to 4 of TOL1 to “0”.	p.281 ☐
			TOMp: Timer output mode register p	For 78K0R/LF3, be sure to clear bits 15 to 8, 6 and 5 of TOM0 to “0”.	p.282 ☐
				For 78K0R/LG3, be sure to clear bits 15 to 8 of TOM0 to “0”.	p.282 ☐
				For 78K0R/LH3, be sure to clear bit 15 to 8 of TOM0, bits 15 to 4 of TOM1 to “0”.	p.282 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 18	Soft	DMA controller	Priority	During DMA transfer, a request from the other DMA channel is held pending even if generated. The pending DMA transfer is started after the ongoing DMA transfer is completed. If two DMA requests are generated at the same time, however, DMA channel 0 takes priority over DMA channel 1. If a DMA request and an interrupt request are generated at the same time, the DMA transfer takes precedence, and then interrupt servicing is executed.	p.738 ☐
	Hard		Response time	The response time of DMA transfer is as follows. (See Table 18-2.)	p.738 ☐
	Soft		Operation in standby mode	The DMA controller operates as follows in the standby mode. (See Table 18-3.)	p.739 ☐
			DMA pending instruction	Even if a DMA request is generated, DMA transfer is held pending immediately after the following instructions. • CALL !addr16 • CALL $!addr20 • CALL !!addr20 • CALL rp • CALLT [addr5] • BRK • Bit manipulation instructions for registers IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H and PSW each.	p.739 ☐
			Operation if address in general-purpose register area or other than those of internal RAM area is specified	The address indicated by DRA0n is incremented during DMA transfer. If the address is incremented to an address in the general-purpose register area or exceeds the area of the internal RAM, the following operation is performed. ● In mode of transfer from SFR to RAM The data of that address is lost. ● In mode of transfer from RAM to SFR Undefined data is transferred to SFR. In either case, malfunctioning may occur or damage may be done to the system. Therefore, make sure that the address is within the internal RAM area other than the general-purpose register area.	p.739 ☐
Chapter 19	Soft	Interrupt functions	IF0L, IF0H, IF1L, IF1H, IF2L, IF2H: Interrupt request flag registers	When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.	p.748 ☐