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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1500agk-gak-ax

2.2.8 P70 to P77

P70 to P77 function as an I/O port. This port can also be used for key return input, serial interface clock I/O, and data I/O.

Input to the P75, and P76 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 7 (PIM7).

Output from the P75, and P77 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 7 (POM7).

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P70/KR0	–		√
P71/KR1	–		√
P72/KR2	–		√
P73/KR3	–		√
P74/KR4	–		√
P75/$\overline{\text{SCK01}}$	–		√
P76/KR6/SI01	–		√
P77/KR7/SO01	–		√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P70 to P77 function as an I/O port. P70 to P77 can be set to input or output port in 1-bit units using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

(2) Control mode

P70 to P77 function as key interrupt input, serial interface clock I/O, and data I/O.

(a) KR0 to KR7

These are the key return input pins

(b) $\overline{\text{SCK01}}$

This is a clock I/O pin of serial interface CSI01.

(c) SI01

This is a serial data input pin of serial interface CSI01.

(d) SO01

This is a serial data output pin of serial interface CSI01.

Caution To use P75/$\overline{\text{SCK01}}$/KR5, P76/SI01/KR6, and P77/SO01/KR7, as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 14-6 Relationship Between Register Settings and Pins (Channel 1 of unit 0: CSI01, UART0 Reception).

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flags (ISP1, ISP0)

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 by a priority specification flag register (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H) (see **19.3 (3)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

Remark n = 0, 1

(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

Figure 3-10. Format of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves data as shown in Figure 3-11.

Cautions 1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

2. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as a stack area.

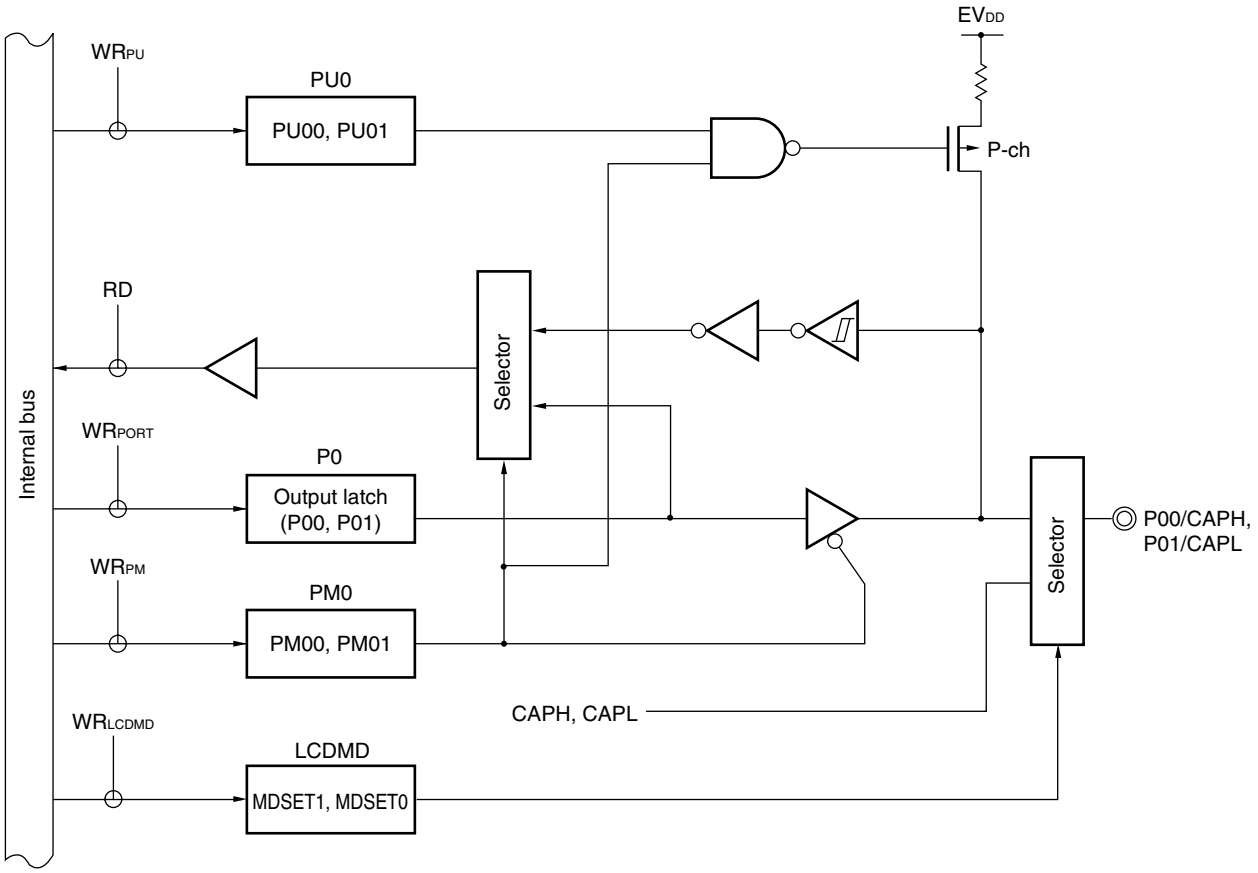
3. While using the self-programming function, the area of FFE20H to FFEFFH cannot be used as a stack memory.

Table 3-5. SFR List (3/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
				1-bit	8-bit	16-bit				
FFF5CH	D/A converter mode register	DAM	R/W	√	√	–	00H	√	√	√
FFF64H	Timer data register 02	TDR02	R/W	–	–	√	0000H	√	√	√
FFF65H										
FFF66H	Timer data register 03	TDR03	R/W	–	–	√	0000H	√	√	√
FFF67H										
FFF68H	Timer data register 04	TDR04	R/W	–	–	√	0000H	√	√	√
FFF69H										
FFF6AH	Timer data register 05	TDR05	R/W	–	–	√	0000H	√	√	√
FFF6BH										
FFF6CH	Timer data register 06	TDR06	R/W	–	–	√	0000H	√	√	√
FFF6DH										
FFF6EH	Timer data register 07	TDR07	R/W	–	–	√	0000H	√	√	√
FFF6FH										
FFF70H	Timer data register 10	TDR10	R/W	–	–	√	0000H	√	√	√
FFF71H										
FFF72H	Timer data register 11	TDR11	R/W	–	–	√	0000H	√	√	√
FFF73H										
FFF74H	Timer data register 12	TDR12	R/W	–	–	√	0000H	√	√	√
FFF75H										
FFF76H	Timer data register 13	TDR13	R/W	–	–	√	0000H	√	√	√
FFF77H										
FFF90H	Sub-count register	RSUBC	R	–	–	√	0000H	√	√	√
FFF91H										
FFF92H	Second count register	SEC	R/W	–	√	–	00H	√	√	√
FFF93H	Minute count register	MIN	R/W	–	√	–	00H	√	√	√
FFF94H	Hour count register	HOUR	R/W	–	√	–	12H[Note]	√	√	√
FFF95H	Week count register	WEEK	R/W	–	√	–	00H	√	√	√
FFF96H	Day count register	DAY	R/W	–	√	–	01H	√	√	√
FFF97H	Month count register	MONTH	R/W	–	√	–	01H	√	√	√
FFF98H	Year count register	YEAR	R/W	–	√	–	00H	√	√	√
FFF99H	Watch error correction register	SUBCUD	R/W	–	√	–	00H	√	√	√
FFF9AH	Alarm minute register	ALARMWM	R/W	–	√	–	00H	√	√	√
FFF9BH	Alarm hour register	ALARMWH	R/W	–	√	–	12H	√	√	√
FFF9CH	Alarm week register	ALARMWW	R/W	–	√	–	00H	√	√	√

Note The value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Figure 4-1. Block Diagram of P00 and P01



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
LCDMD: LCD mode register
RD: Read signal
WR××: Write signal

4.2.3 Port 2

<R>

	μPD78F150xA			μPD78F151xA		
	78K0R/LF3 (80 pins)	78K0R/LG3 (100 pins)	78K0R/LH3 (128 pins)	78K0R/LF3 (80 pins)	78K0R/LG3 (100 pins)	78K0R/LH3 (128 pins)
P20/ANI0/AMP0-	√			P20/ANI0		
P21/ANI1/AMP0O	√			P20/ANI1		
P22/ANI2/AMP0+	√			P20/ANI2		
P23/ANI3/AMP1-	√			P20/ANI3		
P24/ANI4/AMP1O	√			P20/ANI4		
P25/ANI5/AMP1+	√			P20/ANI5		
P26/ANI6/AMP2-	P26/ANI6	√		P26/ANI6		
P27/ANI7/AMP2O	–	√		–	P27/ANI7	

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for A/D converter analog input, and operational amplifier I/O.

To use P20/ANI0/AMP0- to P27/ANI7/AMP2O as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using PM2. Use these pins starting from the lower bit.

To use P20/ANI0/AMP0- to P27/ANI7/AMP2O as digital output pins, set them in the digital I/O mode by using ADPC and in the output mode by using PM2.

To use P20/ANI0/AMP0- to P27/ANI7/AMP2O as analog input pins, set them in the analog input mode by using the A/D port configuration register (ADPC) and in the input mode by using PM2. Use these pins starting from the upper bit.

All P20/ANI0/AMP0- to P27/ANI7/AMP2O are set in the digital input mode when the reset signal is generated.

Figures 4-7 to 4-9 show block diagrams of port 2.

Caution Make the AV_{DD0} pin the same potential as the EV_{DD} or V_{DD} pin when port 2 is used as a digital port.

Table 4-6. Setting Functions of ANI0/AMP0-/P20, ANI2/AMP0+/P22, ANI3/AMP1-/P23, ANI5/AMP1+/P25, and ANI6/AMP2-/P26 Pins

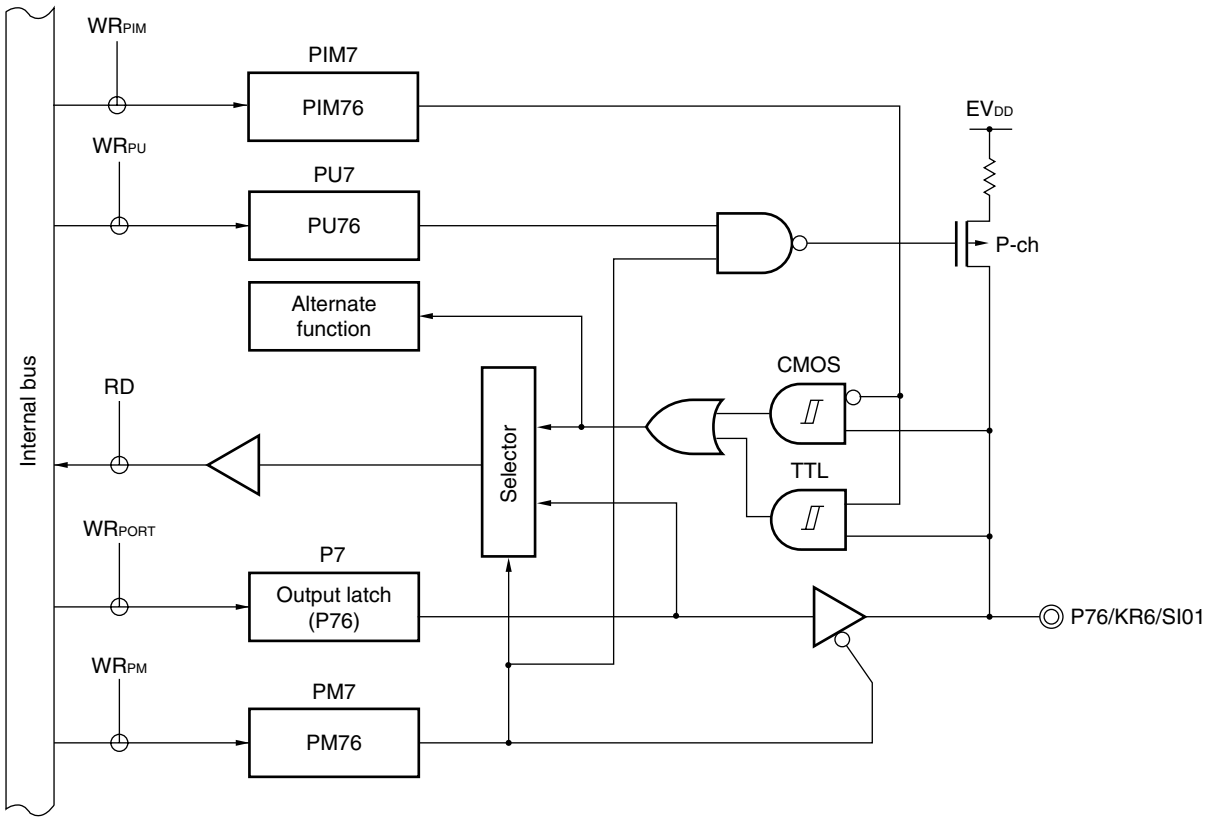
ADPC register	PM2 registers	OAENn bit	ADS register	ANI0/AMP0-/P20, ANI2/AMP0+/P22, ANI3/AMP1-/P23, ANI5/AMP1+/P25, and ANI6/AMP2-/P26 Pins
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	Selects ANI.	Setting prohibited
			Does not select ANI.	Operational amplifier input
	Output mode	–	–	Setting prohibited

Table 4-7. Setting Functions of ANI1/AMP0O/P21, ANI4/AMP1O/P24, and ANI7/AMP2O/P27 Pins

ADPC register	PM2 register	OAENn bit	ADS register	ANI1/AMP0O/P21, ANI4/AMP1O/P24, and ANI7/AMP2O/P27 Pins
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	Selects ANI.	Operational amplifier output (to be converted)
			Does not select ANI.	Operational amplifier output (not to be converted)
	Output mode	–	–	Setting prohibited

Remark 78K0R/LF3: n = 0, 1
78K0R/LG3, 78K0R/LH3: n = 0 to 2

Figure 4-18. Block Diagram of P76



P7: Port register 7
PU7: Pull-up resistor option register 7
PIM7: Port input mode register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

Remarks 1. f_{IH}: Internal high-speed oscillation clock frequency
f_{IH20}: 20 MHz Internal high-speed oscillation clock frequency
f_{MX}: High-speed system clock frequency
f_{SUB} Subsystem clock frequency
2. ×: don't care

Cautions 1. The clock set by CSS, MCM0, SDIV, and MDIV2 to MDIV0 is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time counter, timer array unit (when $f_{SUB}/2$, $f_{SUB}/4$, the valid edge of TI0mn input, or the valid edge of INTRTCI is selected as the count clock), clock output/buzzer output, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral operating hardware clock.
2. If the peripheral hardware clock is used as the subsystem clock, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 31 ELECTRICAL SPECIFICATIONS.

The fastest instruction can be executed in 1 clock of the CPU clock in the 78K0R/Lx3 microcontrollers. Therefore, the relationship between the CPU clock (f_{CLK}) and the minimum instruction execution time is as shown in Table 5-3.

Table 5-3. Relationship Between CPU Clock and Minimum Instruction Execution Time

CPU Clock (Value set by the SDIV, and MDIV2 to MDIV0 bits)	Minimum Instruction Execution Time: $1/f_{CLK}$				
	Main System Clock (CSS = 0)				Subsystem Clock (CSS = 1)
	High-Speed System Clock (MCM0 = 1)		Internal High-Speed Oscillation Clock (MCM0 = 0)		
	At 10 MHz Operation	At 20 MHz Operation	At 8 MHz (TYP.) Operation	At 20 MHz (TYP.) Operation	At 32.768 kHz Operation
f_{MAIN}	0.1 μs	0.05 μs	0.125 μs (TYP.)	0.05 μs (TYP.)	–
$f_{MAIN}/2$	0.2 μs	0.1 μs	0.25 μs (TYP.) (default)	0.1 μs (TYP.)	–
$f_{MAIN}/2^2$	0.4 μs	0.2 μs	0.5 μs (TYP.)	0.2 μs (TYP.)	–
$f_{MAIN}/2^3$	0.8 μs	0.4 μs	1.0 μs (TYP.)	0.4 μs (TYP.)	–
$f_{MAIN}/2^4$	1.6 μs	0.8 μs	2.0 μs (TYP.)	0.8 μs (TYP.)	–
$f_{MAIN}/2^5$	3.2 μs	1.6 μs	4.0 μs (TYP.)	1.6 μs (TYP.)	–
f_{SUB}	–		–		30.5 μs
$f_{SUB}/2$	–		–		61 μs

Remark f_{MAIN}: Main system clock frequency (f_{IH}, f_{IH20}, or f_{MX})
f_{SUB}: Subsystem clock frequency

(3) Timer mode register mn (TMRmn)

TMRmn sets an operation mode of channel n of timer array unit m. It is used to select an operation clock (MCK), a count clock, whether the timer operates as the master or a slave, a start trigger and a capture trigger, the valid edge of the timer input, and an operation mode (interval, capture, event counter, one-count, or capture & one-count).

Rewriting TMRmn is prohibited when the register is in operation (when TEm = 1). However, bits 7 and 6 (CISmn1, CISmn0) can be rewritten even while the register is operating with some functions (when TEm = 1) (for details, see **6.7 Operation of Timer Array Unit as Independent Channel** and **6.8 Operation of Plural Channels of Timer Array Unit**).

TMRmn can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 6-7. Format of Timer Mode Register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKSmn	0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

CKSmn	Selection of operation clock (MCK) of channel n
0	Operation clock CKm0 set by TPSm register
1	Operation clock CKm1 set by TPSm register
Operation clock MCK is used by the edge detector. A count clock (TCLK) and a sampling clock are generated depending on the setting of the CCSmn bit.	

CCSmn	Selection of count clock (TCLK) of channel n
0	Operation clock MCK specified by CKSmn bit
1	Valid edge of input signal input from TIpq pin, $f_{SUB}/2$, $f_{SUB}/4$, or INTRTC1 (the timer input used with channel x is selected by using TISm register).
Count clock TCLK is used for the timer/counter, output controller, and interrupt controller. If CCSmn = 1, use the count clock under the following condition. • The frequency of the operating clock selected by using CKSmn ≥ The frequency of the clock selected by using TISmn × 2	

Caution Be sure to clear bits 14, 13, 5, and 4 to "0".

Remark mn: Unit number + Channel number, pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 04, 07
78K0R/LG3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 07
78K0R/LH3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 07, 10 to 13

Cautions 1. Make sure the period of <4> to <8> is 1 μs or more.

2. <4> may be done between <5> and <7>.

3. <4> can be omitted. However, ignore data of the first conversion after <8> in this case.

4. The period from <9> to <13> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM. The period from <12> to <13> is the conversion time set using FR2 to FR0, LV1, and LV0.

5. To use an operational amplifier output for an analog input, start operating the operational amplifier before setting the A/D conversion operation (see CHAPTER 12 OPERATIONAL AMPLIFIER). Furthermore, do not change the operational amplifier setting during the A/D conversion operation.

6. To use an output voltage of the voltage reference for a positive reference voltage of A/D converter, start operating the voltage reference before setting the A/D conversion operation (see CHAPTER 13 VOLTAGE REFERENCE). Furthermore, do not change the voltage reference setting during the A/D conversion operation.

7. When using the A/D converter in normal mode 2 (LV1 = 0, LV0 = 1) or low voltage mode (LV1 = 1, LV0 = 0), enable the input gate voltage boost circuit for the A/D converter by using the analog reference voltage control register (ADVRC), and then set ADCE and ADCS to 1. After the voltage boost circuit stabilization time (10 μs) passes after the input gate voltage boost circuit for the A/D converter has been enabled, set ADCS to 1.

10.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 12 bits.

$1LSB = 1/2^{12} = 1/4096$

<R> $= 0.024\ \%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.

Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.

Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.

Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 10-22. Overall Error

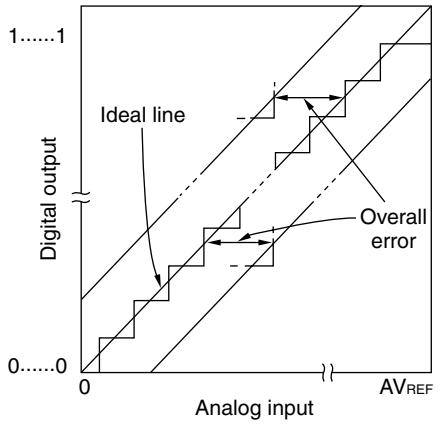
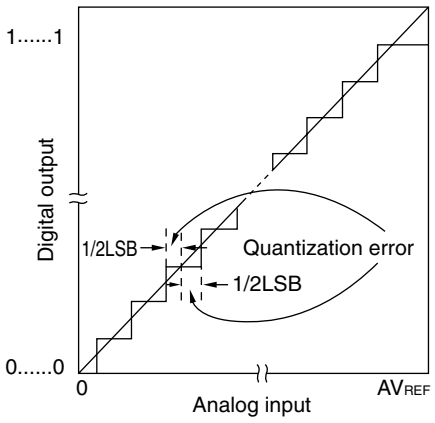


Figure 10-23. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.

If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

(10) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to A/D converter mode register (ADM), A/D converter mode register 1 (ADM1), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADM1, ADS, or ADPC. Using a timing other than the above may cause an incorrect conversion result to be read.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 10-30. Internal Equivalent Circuit of ANIn Pin

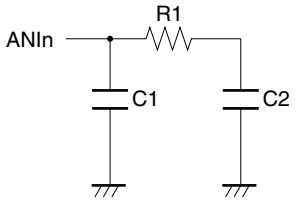


Table 10-8. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

R1	C1	C2
11.5 kΩ	8.0 pF	8.0 pF

Remarks 1. The resistance and capacitance values shown in Table 10-8 are not guaranteed values.

2. 78K0R/LF3: n = 0 to 6, 15, 78K0R/LG3, 78K0R/LH3: n = 0 to 10, 15

(12) Rewriting DACSWn during A/D conversion

Rewriting DACSWn (n = 0, 1) during A/D conversion is prohibited when both the positive reference voltage of A/D converter (AD_{REFP}) and the positive reference voltage of the D/A converter (DA_{REFP}) are the voltage reference output (V_{REFOUT}) (VRSEL = 1 and DAREF = 1). Rewrite it when conversion operation is stopped (ADCS = 0).

(8) Serial channel enable status register m (SEm)

SEm indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register 0 (SSm), the corresponding bit of this register is set to 1.

When 1 is written a bit of serial channel stop register 0 (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of CKOmn of the serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of CKOmn of the SOm register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

SEm can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of SEm can be set with an 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears this register to 0000H.

Figure 14-11. Format of Serial Channel Enable Status Register m (SEm)

Address: F0120H, F0121H (SE0), F0160H, F0161H (SE1) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEm	0	0	0	0	0	0	0	0	0	0	0	0	SEm3	SEm2	SEm1	SEm0

SEmn	Indication of operation enable/stop status of channel n
0	Operation stops (stops with the values of the control register and shift register, and the statuses of the serial clock I/O pin, serial data output pin, and the FEF, PEF, and OVF error flags retained[Note]).
1	Operation is enabled.

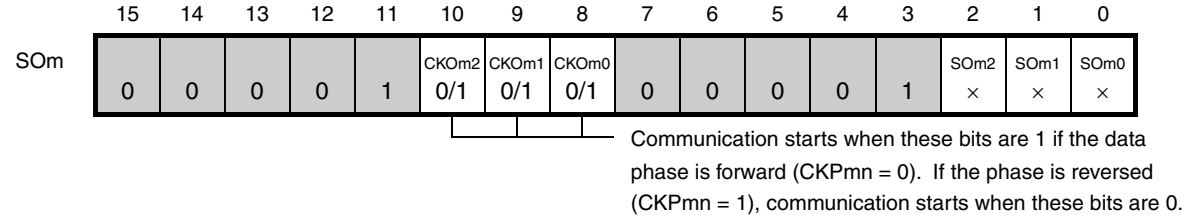
Note Bits 6 and 5 (TSFmn, BFFmn) of the SSRmn register are cleared.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

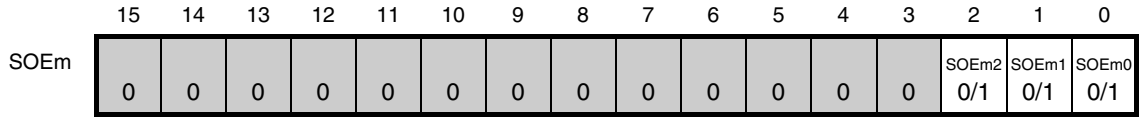
(1) Register setting

Figure 14-32. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20)

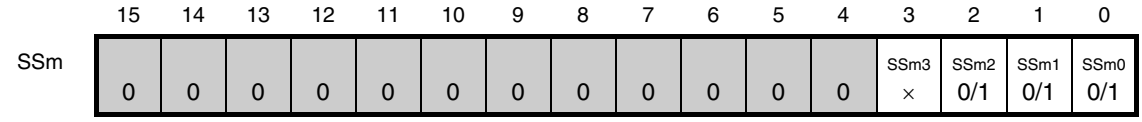
(a) Serial output register m (SOm) … Sets only the bits of the target channel.



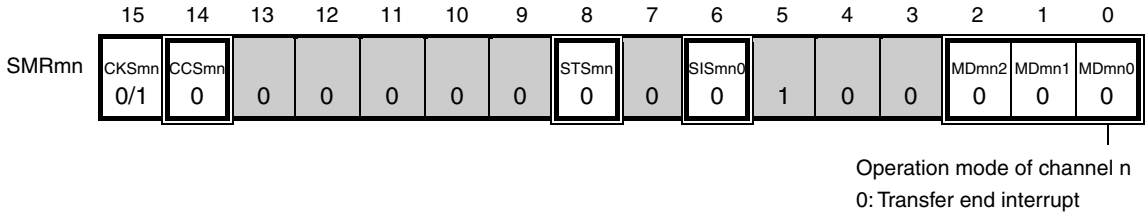
(b) Serial output enable register m (SOEm) … Clears only the bits of the target channel to 0.



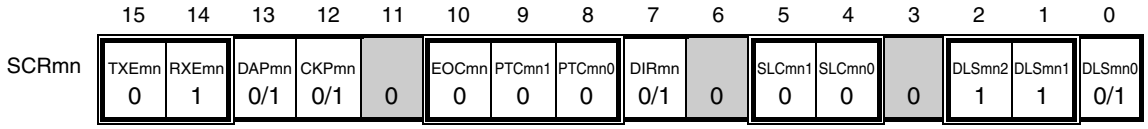
(c) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.



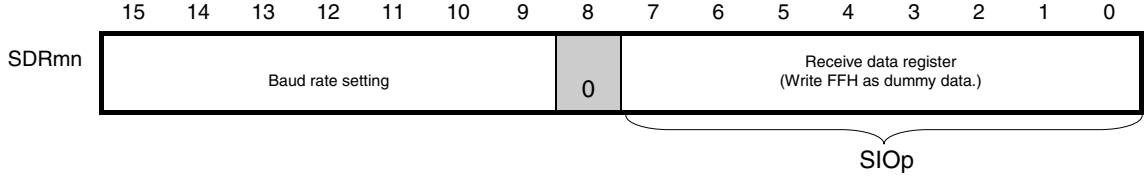
(d) Serial mode register mn (SMRmn)



(e) Serial communication operation setting register mn (SCRmn)



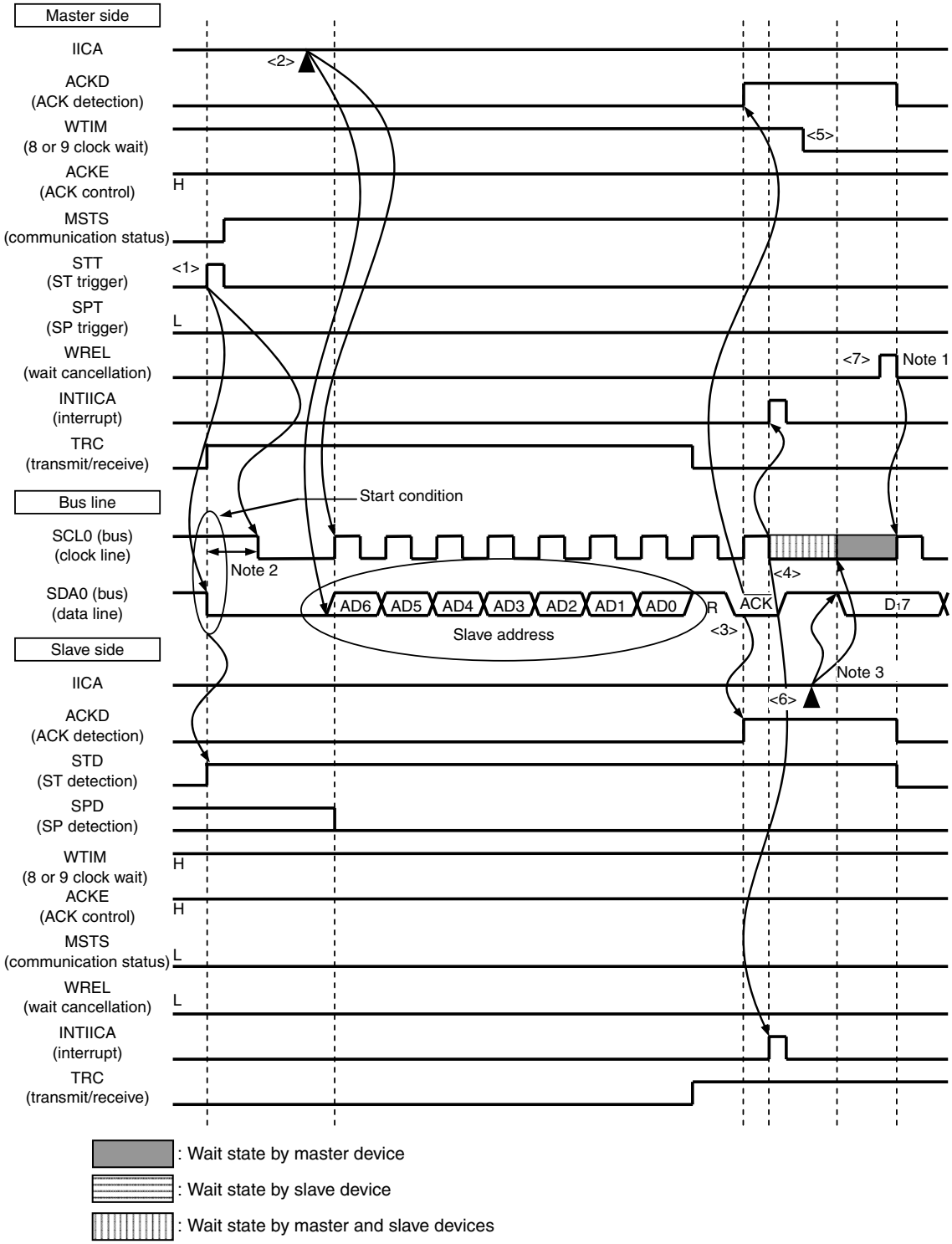
(f) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)
□: Setting is fixed in the CSI master reception mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 15-33. Example of Slave to Master Communication (When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address ~ data



Notes 1. To cancel master wait, write “FFH” to IICA or set the WREL bit.

2. Make sure that the time between the fall of the SDA0 pin signal and the fall of the SCL0 pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

3. Write data to IICA, not setting the WREL bit, in order to cancel a wait state during slave transmission.

Figure 16-23. Three-Time-Slice LCD Drive Waveform Examples (1/2 Bias Method)

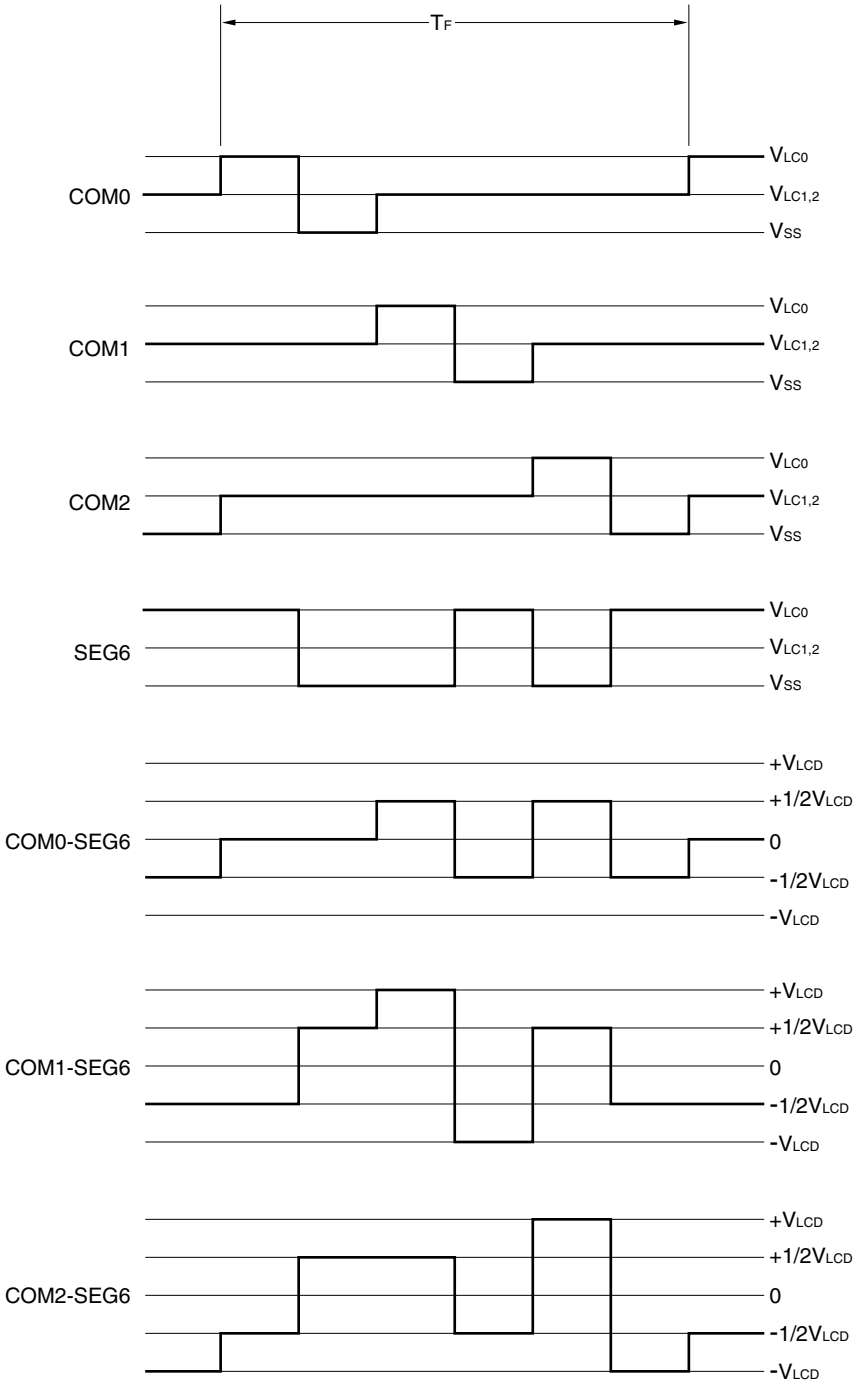


Table 19-1. Interrupt Source List (3/3)

Interrupt Type	Internal/ External	Basic Configuration Type Note 1	Default Priority Note 2	Interrupt Source		Vector Table Address	LF 3	LG 3	LH 3
				Name	Trigger				
Maskable	Internal	(A)	41	INTTM10	End of timer channel 10 count or capture	00056H	√	√	√
			42	INTTM11	End of timer channel 11 count or capture	00058H	√	√	√
			43	INTTM12	End of timer channel 12 count or capture	0005AH	√	√	√
			44	INTTM13	End of timer channel 13 count or capture	0005CH	√	√	√
			45	INTMD	End of multiply/divide operation	0005EH	√	√	√
Software	–	(D)	–	BRK	Execution of BRK instruction	0007EH	√	√	√
Reset	–	–	–	RESET	$\overline{\text{RESET}}$ pin input	00000H	√	√	√
				POC	Power-on-clear		√	√	√
				LVI	Low-voltage detection Note 3		√	√	√
				WDT	Overflow of watchdog timer		√	√	√
				TRAP	Execution of illegal instruction Note 4		√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 45 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 19-1.

3. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

4. When the instruction code in FFH is executed.

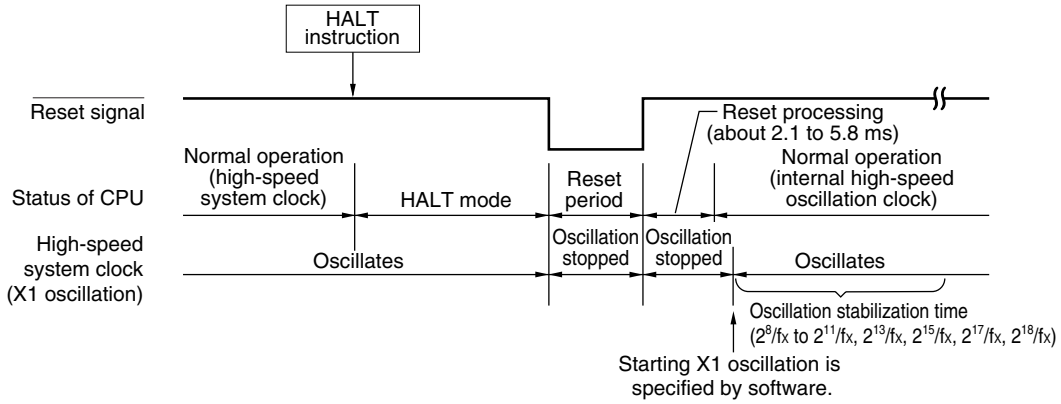
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(b) Release by reset signal generation

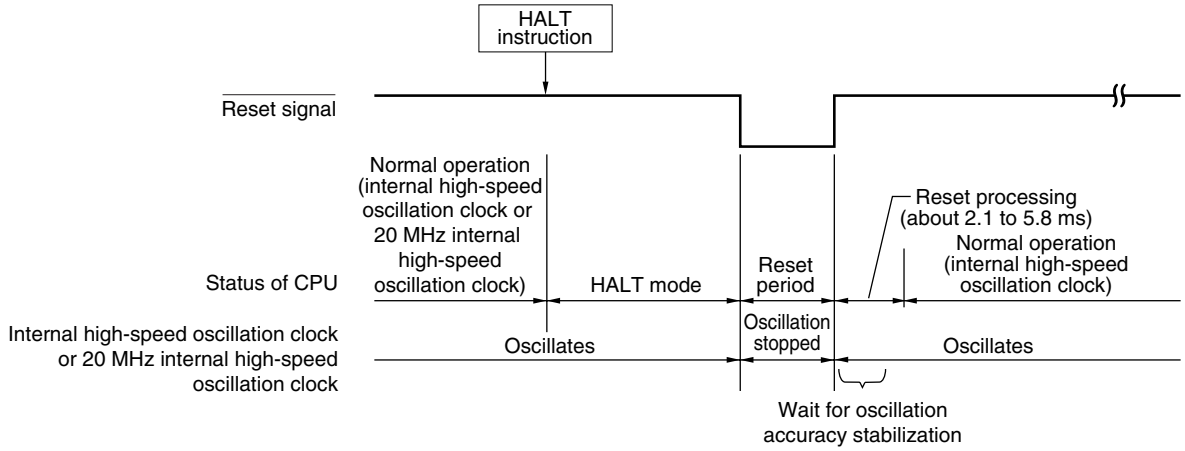
When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 21-4. HALT Mode Release by Reset

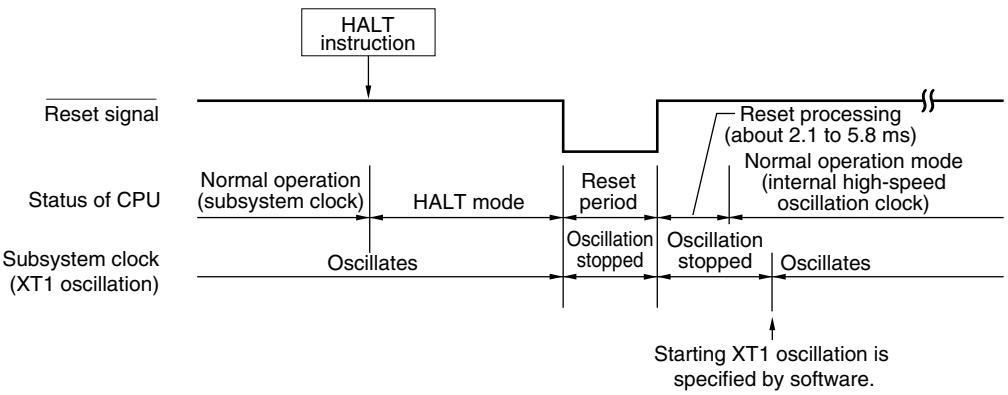
(1) When high-speed system clock is used as CPU clock



(2) When internal high-speed oscillation clock or 20 MHz internal high-speed oscillation clock is used as CPU clock



(3) When subsystem clock is used as CPU clock



Remark fx: X1 clock oscillation frequency

30.1.3 Description of flag operation column

The change of the flag value when the instruction is executed is shown in the “Flag” column using the following symbols.

Table 30-3. Symbols in “Flag” Column

Symbol	Change of Flag Value
(Blank)	Unchanged
0	Cleared to 0
1	Set to 1
×	Set/cleared according to the result
R	Previously saved value is restored

30.1.4 PREFIX instruction

Instructions with “ES:” have a PREFIX operation code as a prefix to extend the accessible data area to the 1 MB space (00000H to FFFFFH), by adding the ES register value to the 64 KB space from F0000H to FFFFFH. When a PREFIX operation code is attached as a prefix to the target instruction, only one instruction immediately after the PREFIX operation code is executed as the addresses with the ES register value added.

Table 30-4. Use Example of PREFIX Operation Code

Instruction	Opcode				
	1	2	3	4	5
MOV !addr16, #byte	CFH	!addr16		#byte	–
MOV ES:!addr16, #byte	11H	CFH	!addr16		#byte
MOV A, [HL]	8BH	–	–	–	–
MOV A, ES:[HL]	11H	8BH	–	–	–

Caution Set the ES register value with MOV ES, A, etc., before executing the PREFIX instruction.

(7/14)

Edition	Description	Chapter
3rd Edition	Addition of description to **6.7.1 Operation as interval timer/square wave output**	CHAPTER 6 TIMER ARRAY UNIT
	Modification of **Figure 6-37 Block Diagram of Operation as Interval Timer/Square Wave Output**	
	Addition of **(2) When the timer input (TIpq pin input, f_{SUB}/4, f_{SUB}/2 or INTRTCI) is selected as count clock** to **Figure 6-39 Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output**	
	Modification of **Figure 6-40 Operation Procedure of Interval Timer/Square Wave Output Function (1/2)**	
	Modification of **Caution** in **Figure 7-3 Format of Real-Time Counter Control Register 0 (RTCC0)**	CHAPTER 7 REAL-TIME COUNTER
	Addition of description to **7.3 (8) Hour count register (HOUR)**	
	Addition of description to **Figure 7-14 Format of Watch Error Correction Register (SUBCUD)**	
	Modification of **Figure 7-26 512 Hz or 16.384 kHz Output Setting Procedure**	
	Addition of **Caution 3** to **Figure 9-2 Format of Clock Output Select Register n (CKSn)**	CHAPTER 9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER
	Modification of **Remark** in **9.4.1 Operation as output pin**	
	Modification of **Figure 9-4 Remote Control Output Application Example**	
	Addition of **Notes 2, 3** to and modification of **Cautions 1, 2** in **Figure 10-4 Format of A/D Converter Mode Register (ADM)**	CHAPTER 10 A/D CONVERTER
	Modification of **Table 10-2 A/D Conversion Time Selection**	
	Modification of description in **10.3 (4) Analog reference voltage control register (ADVRC)**	
	Modification of **Figure 10-8 Format of Analog Reference Voltage Control Register (ADVRC)**	
	Addition of **<3>** to and modification of **<8>** and **Caution 4** in **10.4.1 Basic operations of A/D converter**	
	Modification of **Figure 10-16 Software trigger mode (Continuous conversion mode)**	
	Modification of **Figure 10-17 Software trigger mode (Single conversion mode)**	
	Modification of **<2>** in **10.4.3 (3) Timer trigger mode (Continuous conversion mode)**	
	Modification of **Figure 10-18 Timer trigger mode (Continuous conversion mode)**	
	Modification of **<2>** in and addition of **<5>** to **10.4.3 (4) Timer trigger mode (Single conversion mode)**	
	Modification of **Figure 10-19 Timer trigger mode (Single conversion mode)**	
	Addition of **<3>** to and modification of **<8>, <11>** and **Caution 7** in setting methods of **10.4.3 A/D converter operation modes**	
	Modification of **10.6 (1) Operating current in STOP mode** and **(12) Rewriting DACSWn during A/D conversion**	
	Modification of **Figure 11-1 Block Diagram of D/A Converter**	CHAPTER 11 D/A CONVERTER
	Addition of **Note 1** to and modification of **Note 2** and **Remark** in **Figure 11-3 Format of D/A Converter Mode Register (DAM)**	
	Modification of **Caution** in **Figure 11-4 Format of D/A Conversion Value Setting Registers W0 and W1 (DACSW0, DACSW1)**	
	Modification of **<3>**, **<6>** in and addition of **Cautions 1, 2** to **11.4.1 Operation in normal mode**	
	Modification of **<3>**, **<6>**, **<9>** in and addition of **Cautions 1 to 3** to **11.4.2 Operation in real-time output mode**	
	Modification of **(3)** in **11.5 Cautions for D/A Converter**	