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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1501agc-gad-ax

4.2 Port Configuration

Ports include the following hardware.

Table 4-5. Port Configuration

Item	Configuration
Control registers	• 78K0R/LF3 Port mode registers (PMxx) : PM0 to PM5, PM9 to PM12, PM14, PM15 Port registers (Pxx) : P0 to P5, P9 to P15 Pull-up resistor option registers (PUxx) : PU0, PU1, PU3 to PU5, PU9, PU10, PU12, PU14 Port input mode registers (PIM1) Port output mode registers (POM1) A/D port configuration register (ADPC) Port function register (PFALL) Input switch control register (ISC) • 78K0R/LG3 Port mode registers (PMxx) : PM0 to PM6, PM8 to PM12, PM14, PM15 Port registers (Pxx) : P0 to P6, P8 to P15 Pull-up resistor option registers (PUxx) : PU0, PU1, PU3 to PU5, PU8 to PU10, PU12, PU14 Port input mode registers (PIM1) Port output mode registers (POM1, POM8) A/D port configuration register (ADPC) Port function register (PFALL) Input switch control register (ISC) • 78K0R/LH3 Port mode registers (PMxx) : PM0 to PM12, PM14, PM15 Port registers (Pxx) : P0 to P15 Pull-up resistor option registers (PUxx) : PU0, PU1, PU3 to PU5, PU7 to PU10, PU12, PU14 Port input mode registers (PIM1, PIM7) Port output mode registers (POM1, POM7, POM8) A/D port configuration register (ADPC) Port function register (PFALL) Input switch control register (ISC)
Port	• 78K0R/LF3: Total: 51 (CMOS I/O: 46, CMOS output: 1, CMOS input: 4) • 78K0R/LG3: Total: 67 (CMOS I/O: 60, CMOS output: 1, CMOS input: 4, N-ch open drain I/O: 2) • 78K0R/LH3: Total: 83 (CMOS I/O: 76, CMOS output: 1, CMOS input: 4, N-ch open drain I/O: 2)
Pull-up resistor	• 78K0R/LF3: Total: 36 • 78K0R/LG3: Total: 46 • 78K0R/LH3: Total: 62

4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function

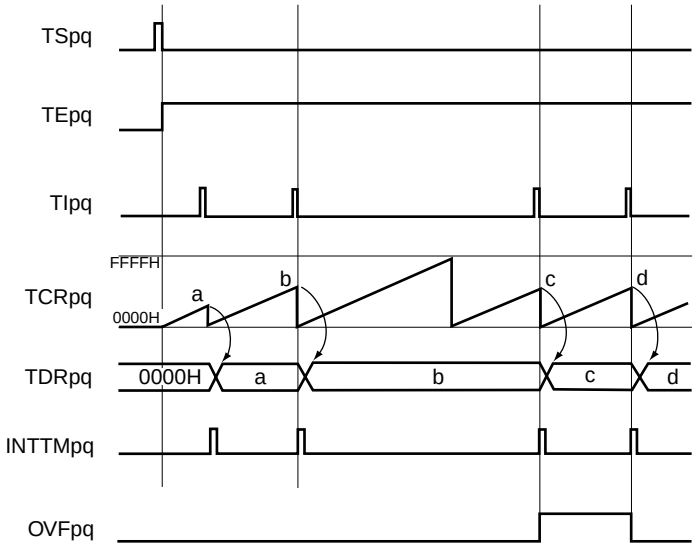
To use the alternate function of a port pin, set the port mode register and output latch as shown in Table 4-11.

Table 4-11. Settings of Port Mode Register and Output Latch When Using Alternate Function (1/5)

LF3	LG3	LH3	Pin Name	Alternate Function		PFALL	ISC	PMxx	Pxx
				Function Name	I/O	(PFxxx)	(ISCx)		
√	√	√	P00	CAPH	Output	–	–	×	×
√	√	√	P01	CAPL	Output	–	–	×	×
√	√	√	P02	V_{LC3}	I/O	–	–	×	×
√	√	√	P10	$\overline{SCK20}$	Input	–	–	1	×
					Output	–	–	0	1
				SCL20	I/O	–	–	0	1
√	√	√	P11	SI20	Input	–	–	1	×
				RxD2	Input	–	–	1	×
				SDA20	I/O	–	–	0	1
				INTP6	Input	–	–	1	×
√	√	√	P12	SO20	Output	–	–	0	1
				TxD2	Output	–	–	0	1
				TO02	Output	–	–	0	0
√	√	√	P13	SO10	Output	–	–	0	1
				TxD1	Output	–	–	0	1
				TO04	Output	–	–	0	0
√	√	√	P14	SI10	Input	–	–	1	×
				RxD1	Input	–	–	1	×
				SDA10	I/O	–	–	0	1
				INTP4	Input	–	–	1	×
√	√	√	P15	$\overline{SCK10}$	Input	–	–	1	×
					Output	–	–	0	1
				SCL10	I/O	–	–	0	1
				INTP7	Input	–	–	1	×
–	√	√	P16	TI05	Input	–	–	1	×
				TO05	Output	–	–	0	0
				INTP10	Input	–	–	1	×

Remark ×: don't care
–: Not applicable
PFALL: Port function register
ISC: Input switch control register
PMxx: Port mode register
Pxx: Port output latch

Figure 6-50. Example of Basic Timing of Operation as Input Pulse Interval Measurement (MDpq0 = 0)



Remark pq: Unit number + Channel number (only for channels provided with timer I/O pins)

78K0R/LF3: pq = 00 to 04, 07

78K0R/LG3: pq = 00 to 07

78K0R/LH3: pq = 00 to 07, 10 to 13

Figure 6-61. Operation Procedure When PWM Function Is Used (2/2)

Operation is resumed.

	Software Operation	Hardware Status
Operation start	Sets TOEmp (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of the TSm register are set to 1 at the same time. → The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	TEmn = 1, TEmp = 1 When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn and TMRmp registers and TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. Set values of the TDRmn and TDRmp registers can be changed after INTTMmn of the master channel is generated. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used. Set values of the TOm and TOEm registers cannot be changed.	The counter of the master channel loads the TDRmn value to TCRmn, and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to TCRmn, and the counter starts counting down again. At the slave channel, the value of TDRmp is loaded to TCRmp, triggered by INTTMmn of the master channel, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. → The TTmn and TTmp bits automatically return to 0 because they are trigger bits.	TEmn, TEmp = 0, and count operation stops. TCRmn and TCRmp hold count value and stops. The TOmp output is not initialized but holds current status.
	TOEmp of slave channel is cleared to 0 and value is set to the TOmp register. →	The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output levels Clears TOmp bit to 0 after the value to be held is set to the port register. →	The TOmp pin output levels is held by port function.
	When holding the TOmp pin output levels is not necessary Switches the port mode register to input mode. →	The TOmp pin output levels go are into Hi-Z output state.
	The TAU0EN or TAU1EN bits of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

Remarks 1. 78K0R/LF3:
- m = 0, n = 0, 2, 6, p = n+1, TO00 to TO04, and TO07 pins

2. 78K0R/LG3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins

3. 78K0R/LH3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins
- m = 1, n = 0, 2, p = n+1, TO10 to TO13 pins

Figure 6-66. Operation Procedure of One-Shot Pulse Output Function (2/2)

	Software Operation	Hardware Status
Operation start	Sets TOEmp (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of the TSm register are set to 1 at the same time. →	TEmn and TEmp are set to 1 and the master channel enters the TImn input edge detection wait status. Counter stops operating.
	Detects the start trigger of master channel. →	Master channel starts counting.
	(The valid edge of the TImn pin input is detected or the TSmn bit is set to 1.)	
During operation	Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed. Set values of the TMRmp, TDRmn, and TDRmp registers and TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used. Set values of the TOm and TOEm registers can be changed.	Master channel loads the value of TDRmn to TCRmn when the start trigger is detected, and the counter starts counting down. When the count value reaches TCRmn = 0000H, the INTTMmn output is generated, and the counter stops until the next valid edge is input to the TImn pin. The slave channel, triggered by INTTMmn of the master channel, loads the value of TDRmp to TCRmp, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. →	TEmn, TEmp = 0, and count operation stops. TCRmn and TCRmp hold count value and stops. The TOmp output is not initialized but holds current status.
	TOEmp of slave channel is cleared to 0 and value is set to the TOm register. →	The TOmp pin outputs the TOmn set level.
TAU stop	To hold the TOmp pin output levels Clears TOmp bit to 0 after the value to be held is set to the port register. →	The TOmp pin output levels is held by port function.
	When holding the TOmp pin output levels is not necessary Switches the port mode register to input mode. →	The TOmp pin output levels go are into Hi-Z output state.
	The TAU0EN or TAU1EN bits of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

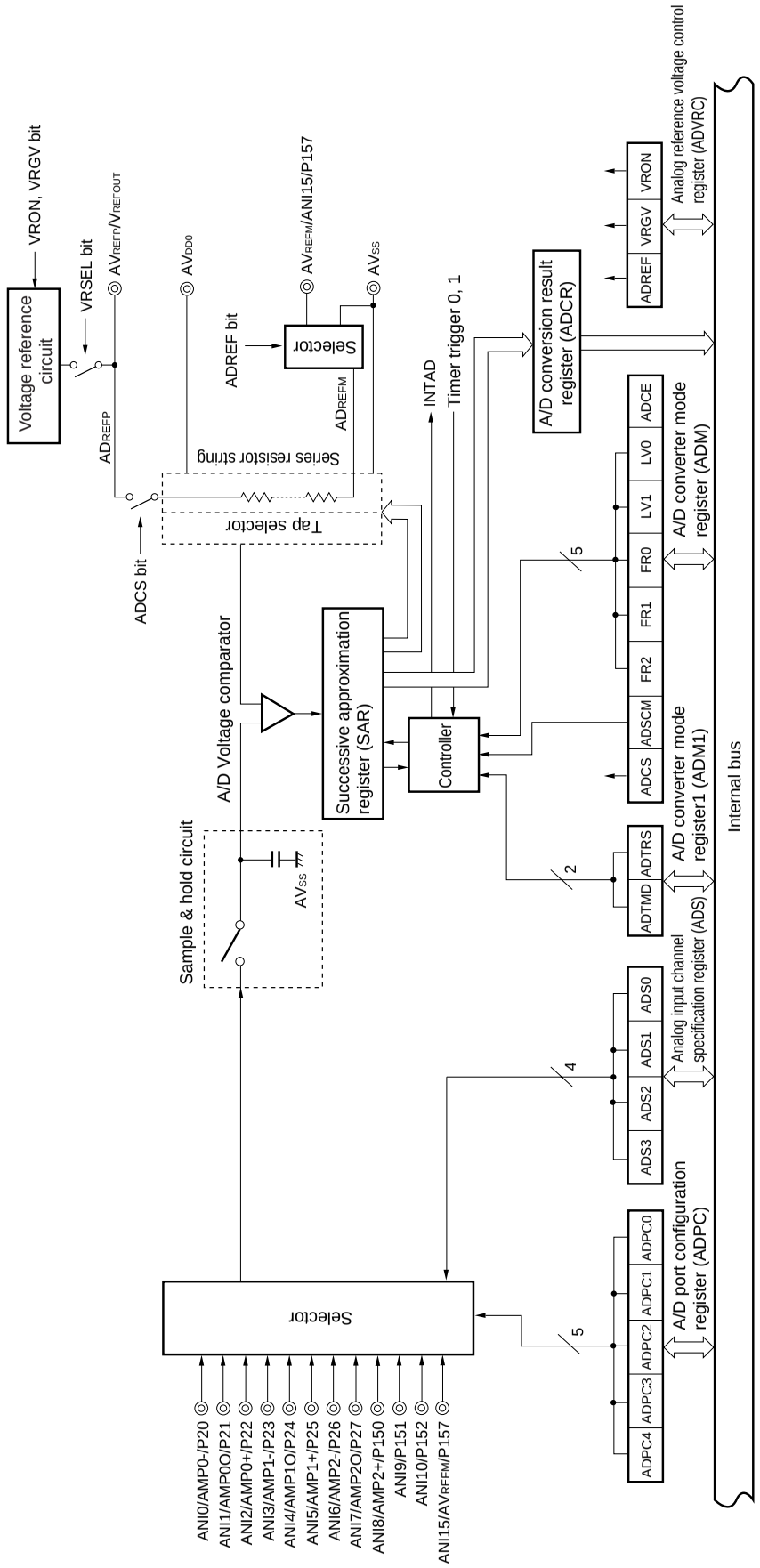
Operation is resumed.

Remarks 1. 78K0R/LF3:
- m = 0, n = 0, 2, 6, p = n+1, TO00 to TO04, and TO07 pins
- Channel 6 of timer array unit 0 can output a one-shot pulse only when software trigger start is selected and it is used as the master channel (because the TI06 pin is not provided).

2. 78K0R/LG3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins

3. 78K0R/LH3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins
- m = 1, n = 0, 2, p = n+1, TO10 to TO13 pins

Figure 10-1. Block Diagram of 12-Bit A/D Converter (μPD78F150xA)



Remark 78K0R/LF3: ANI0-ANI6, ANI15
78K0R/LG3, 78K0R/LH3: ANI0-ANI10, ANI15

Figure 14-7. Format of Serial Communication Operation Setting Register mn (SCRmn) (3/3)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), F0158H, F0159H (SCR10), F015AH, F015BH (SCR11), F015CH, F015DH (SCR12), F015EH, F015FH (SCR13) After reset: 0087H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	0	DLS mn2	DLS mn1	DLS mn0

DLS mn2	DLS mn1	DLS mn0	Setting of data length in CSI and UART modes
1	0	0	5-bit data length (stored in bits 0 to 4 of SDRmn register) (settable in UART mode only)
1	1	0	7-bit data length (stored in bits 0 to 6 of SDRmn register)
1	1	1	8-bit data length (stored in bits 0 to 7 of SDRmn register)
Other than above			Setting prohibited
Be sure to set DLSmn0 = 1 in the simplified I^2C mode.			

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

14.4 Operation stop mode

Each serial interface of serial array unit has the operation stop mode.

In this mode, serial communication cannot be executed, thus reducing the power consumption.

In addition, the P10/SCK20/SCL20, P11/SI20/SDA20/RxD2/INTP6, P12/SO20/TxD2/TO02, P13/SO10/TxD1/TO04, P14/SI10/SDA10/RxD1/INTP4, P15/SCK10/SCL10/INTP7, P50/RxD3/SEGx (78K0R/LF3: x = 30, 78K0R/LG3: x = 39, 78K0R/LH3: x = 53), P51/TxD3/SEGx (78K0R/LF3: x = 29, 78K0R/LG3: x = 38, 78K0R/LH3: x = 52), P75/SCK01/KR5, P76/SI01/KR6, P77/SO01/KR7, P80/SCK00/INTP11, P81/SI00/RxD0/INTP9, and P82/SO00/TxD0 pins can be used as ordinary port pins in this mode.

14.4.1 Stopping the operation by units

The stopping of the operation by units is set by using peripheral enable register 0 (PER0).

PER0 is used to enable or disable use of each peripheral hardware macro. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

To stop the operation of serial array unit 0, set bit 2 (SAU0EN) to 0.

To stop the operation of serial array unit 1, set bit 3 (SAU1EN) to 0.

Figure 14-22. Peripheral Enable Register 0 (PER0) Setting When Stopping the Operation by Units

(a) Peripheral enable register 0 (PER0) … Set only the bit of SAUm to be stopped to 0.

	7	6	5	4	3	2	1	0
PER0	RTCEN	DACEN	ADCEN	IIC0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
	×	×	×	×	0/1	0/1	×	×

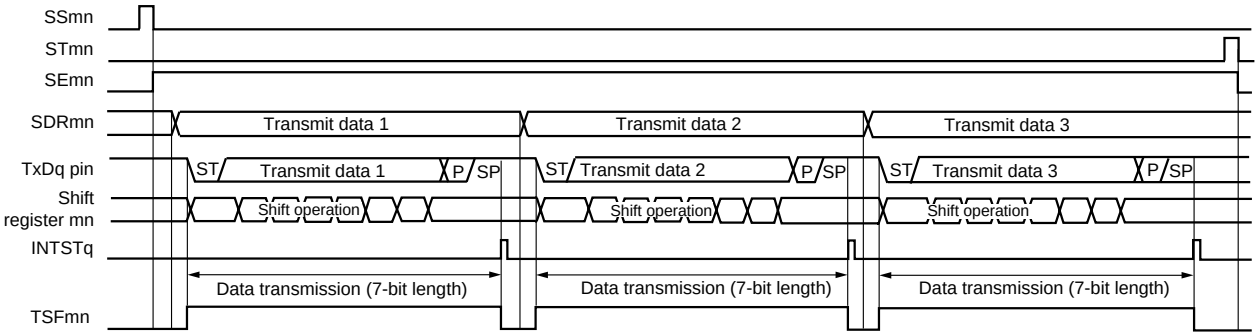
Control of SAUm input clock
0: Stops supply of input clock
1: Supplies input clock

Caution If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for input switch control register (ISC), noise filter enable register (NFEN0), port input mode registers (PIM1, PIM7), port output mode registers (POM1, POM7, POM8), port mode registers (PM1, PM5, PM7, PM8), and port registers (P1, P5, P7, P8)).

Remark m: Unit number (m = 0, 1)
×: Bits not used with serial array units (depending on the settings of other peripheral functions)
0/1: Set to 0 or 1 depending on the usage of the user

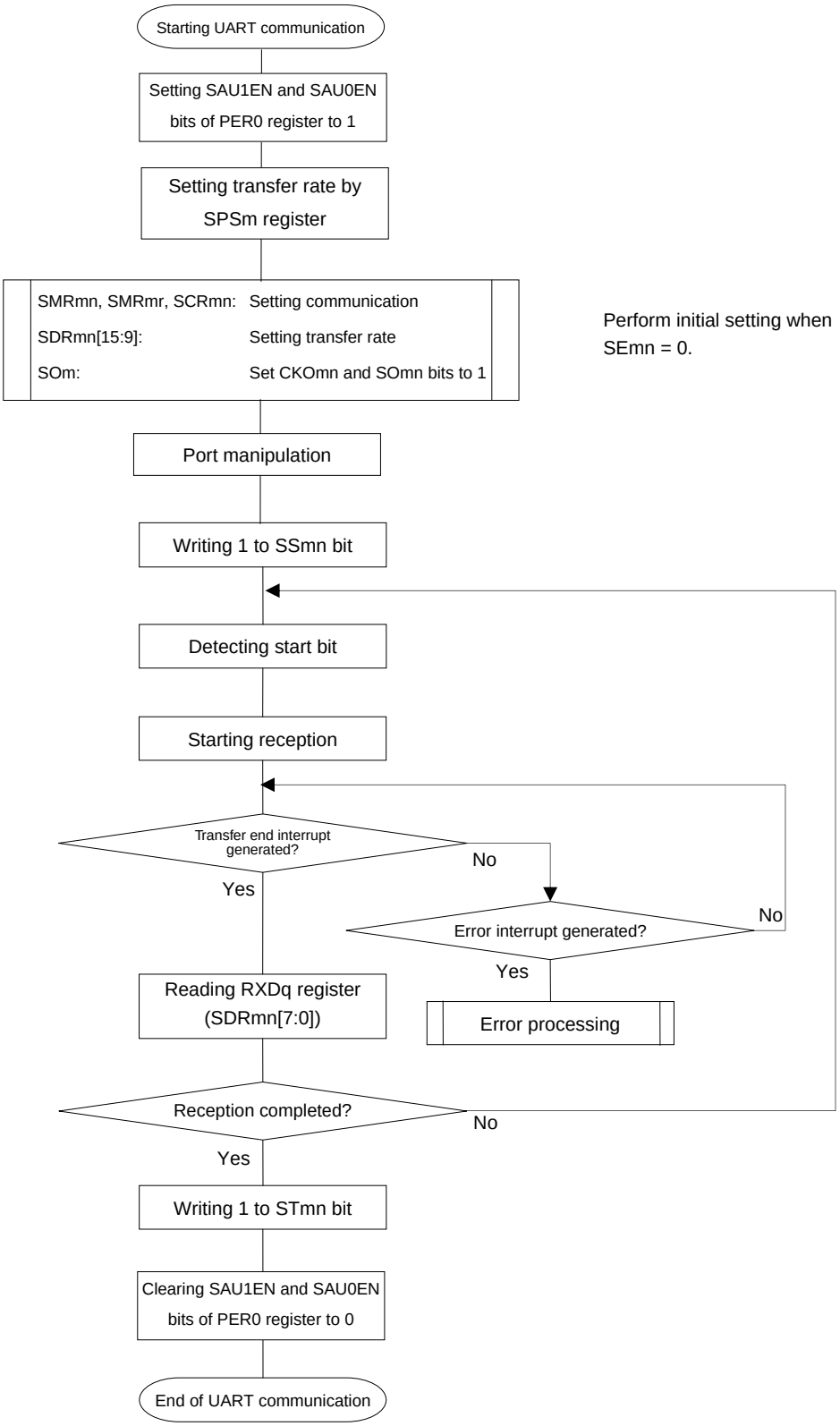
(3) Processing flow (in single-transmission mode)

Figure 14-72. Timing Chart of UART Transmission (in Single-Transmission Mode)



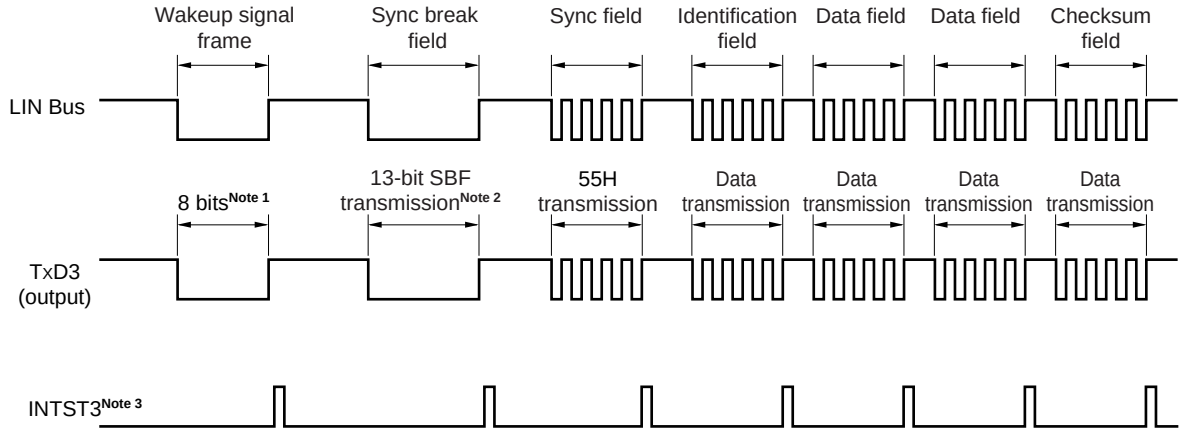
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 3)

Figure 14-81. Flowchart of UART Reception



Caution After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Figure 14-82. Transmission Operation of LIN



Notes 1. The baud rate is set so as to satisfy the standard of the wakeup signal and data of 00H is transmitted.

2. A sync break field is defined to have a width of 13 bits and output a low level. Where the baud rate for main transfer is N [bps], therefore, the baud rate of the sync break field is calculated as follows.

(Baud rate of sync break field) = 9/13 × N

By transmitting data of 00H at this baud rate, a sync break field is generated.

3. INTST3 is output upon completion of transmission. INTST3 is also output when SBF transmission is executed.

Remark The interval between fields is controlled by software.

(5) IICA control register 1 (IICCTL1)

This register is used to set the operation mode of I^2C and detect the statuses of the SCL0 and SDA0 pins.

IICCTL1 can be set by a 1-bit or 8-bit memory manipulation instruction. However, the CLD and DAD bits are read-only.

Set the IICCTL1 register, except the WUP bit, while operation of I^2C is disabled (bit 7 (IICE) of IICA control register 0 (IICCTL0) is 0).

Reset signal generation clears this register to 00H.

Figure 15-9. Format of IICA Control Register 1 (IICCTL1) (1/2)

Address: F0231H After reset: 00H R/W[Note 1]

Symbol	7	6	<5>	<4>	<3>	<2>	1	0
IICCTL1	WUP	0	CLD	DAD	SMC	DFC	0	0

WUP	Control of address match wakeup
0	Stops operation of address match wakeup function in STOP mode.
1	Enables operation of address match wakeup function in STOP mode.

To shift to STOP mode when WUP = 1, execute the STOP instruction at least three clocks after setting (1) the WUP bit (see **Figure 15-22 Flow When Setting WUP = 1**).

Clear (0) the WUP bit after the address has matched or an extension code has been received. The subsequent communication can be entered by the clearing (0) WUP bit. (The wait must be released and transmit data must be written after the WUP bit has been cleared (0).)

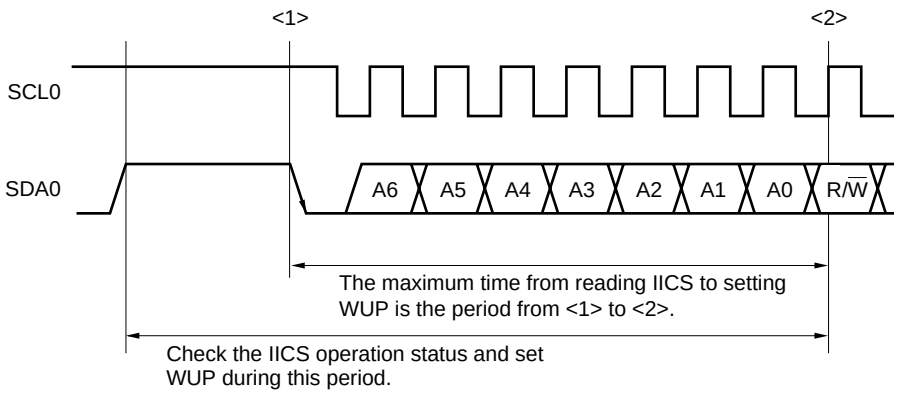
The interrupt timing when the address has matched or when an extension code has been received, while WUP = 1, is identical to the interrupt timing when WUP = 0. (A delay of the difference of sampling by the clock will occur.) Furthermore, when WUP = 1, a stop condition interrupt is not generated even if the SPIE bit is set to 1.

When WUP = 0 is set by a source other than an interrupt from serial interface IICA, operation as the master device cannot be performed until the subsequent start condition or stop condition is detected. Do not output a start condition by setting (1) the STT bit, without waiting for the detection of the subsequent start condition or stop condition.

Condition for clearing (WUP = 0)	Condition for setting (WUP = 1)
• Cleared by instruction (after address match or extension code reception)	• Set by instruction (when the MSTS, EXC, and COI bits are “0”, and the STD bit also “0” (communication not entered))[Note 2]

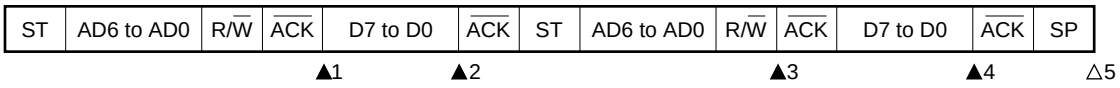
Notes 1. Bits 4 and 5 are read-only.

2. The status of the IICA status register (IICS) must be checked and the WUP bit must be set during the period shown below.



(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

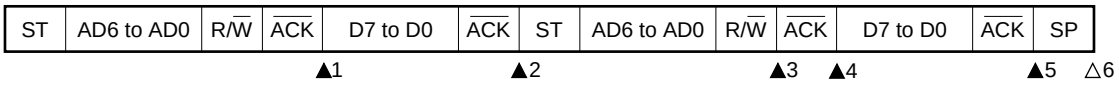
(i) When WTIM = 0 (after restart, does not match address (= extension code))



▲1: IICS = 0001×110B
▲2: IICS = 0001×000B
▲3: IICS = 0010×010B
▲4: IICS = 0010×000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, does not match address (= extension code))



▲1: IICS = 0001×110B
▲2: IICS = 0001××00B
▲3: IICS = 0010×010B
▲4: IICS = 0010×110B
▲5: IICS = 0010××00B
△6: IICS = 00000001B

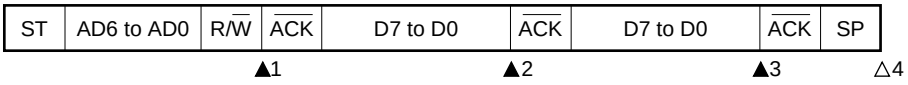
Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(3) Slave device operation (when receiving extension code)

The device is always participating in communication when it receives an extension code.

(a) Start ~ Code ~ Data ~ Data ~ Stop

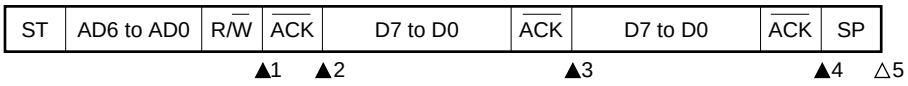
(i) When WTIM = 0



▲1: IICS = 0010×010B
▲2: IICS = 0010×000B
▲3: IICS = 0010×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

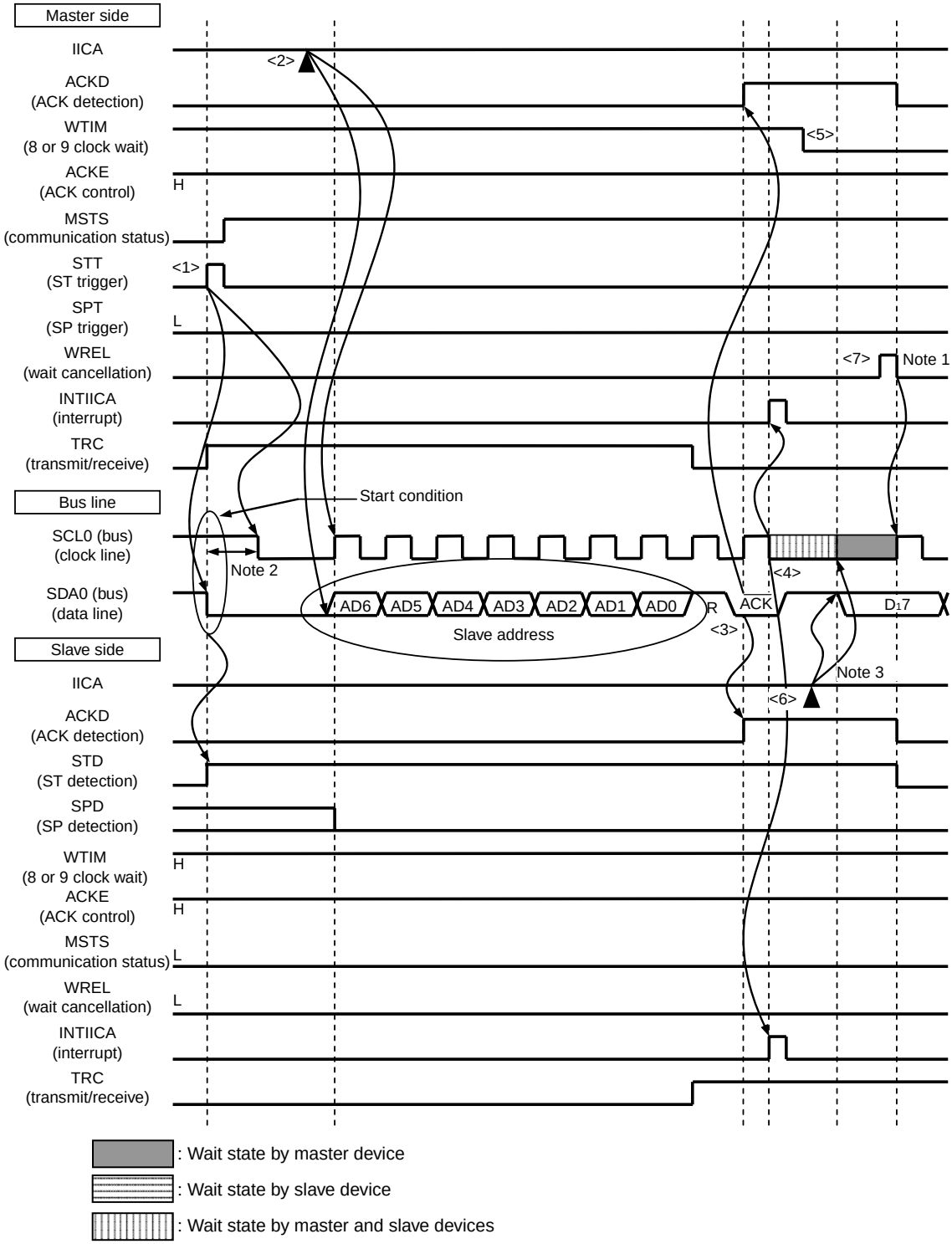


▲1: IICS = 0010×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

Figure 15-33. Example of Slave to Master Communication (When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address ~ data



Notes 1. To cancel master wait, write “FFH” to IICA or set the WREL bit.

2. Make sure that the time between the fall of the SDA0 pin signal and the fall of the SCL0 pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

3. Write data to IICA, not setting the WREL bit, in order to cancel a wait state during slave transmission.

Figure 19-6. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H) (78K0R/LG3)

Address: FFFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	SREMK0	SRMK0	CSIMK00 STMK0	DMAMK1	DMAMK0	SREMK3	SRMK3	STMK3

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	IICAMK	SREMK1	SRMK1	CSIMK10 IICMK10 STMK1

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
MK1H	TMMK04	SREMK2	SRMK2	CSIMK20 IICMK20 STMK2	1	RTCIMK	RTCMK	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK2L	PMK10	PMK9	PMK8	PMK7	PMK6	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
MK2H	1	1	MDMK	TMMK13	TMMK12	TMMK11	TMMK10	PMK11

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution Be sure to set bit 3 of MK1H, bits 6, 7 of MK2H to 1.

Table 22-2. Hardware Statuses After Reset Acknowledgment (1/4)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		06H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Port registers (P0 to P15) (output latches)		00H
Port mode registers (PM0 to PM12, PM14, PM15)		FFH
Port input mode registers 1, 7 (PIM1, PIM7)		00H
Port output mode registers 1, 7, 8 (POM1, POM7, POM8)		00H
Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7 to PU10, PU12, PU14)		00H
Clock operation mode control register (CMC)		00H
Clock operation status control register (CSC)		C0H
Processor mode control register (PMC)		00H
System clock control register (CKC)		09H
20 MHz internal high-speed oscillation control register (DSCCTL)		00H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		07H
Noise filter enable registers 0, 1 (NFEN0, NFEN1)		00H
Peripheral enable registers 0 (PER0)		00H
Operation speed mode control register (OSMC)		00H
Input switch control register (ISC)		00H
Timer array units 0, 1 (TAU0, TAU1)	Timer data registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TDR00, TDR01, TDR02, TDR03, TDR04, TDR05, TDR06, TDR07, TDR10, TDR11, TDR12, TDR13)	0000H
	Timer mode registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TMR00, TMR01, TMR02, TMR03, TMR04, TMR05, TMR06, TMR07, TMR10, TMR11, TMR12, TMR13)	0000H
	Timer status registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TSR00, TSR01, TSR02, TSR03, TSR04, TSR05, TSR06, TSR07, TSR10, TSR11, TSR12, TSR13)	0000H
	Timer input select register 0, 1 (TIS0, TIS1)	00H
	Timer channel counter registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TCR00, TCR01, TCR02, TCR03, TCR04, TCR05, TCR06, TCR07, TCR10, TCR11, TCR12, TCR13)	FFFFH
	Timer channel enable status registers 0, 1 (TE0, TE1)	0000H
	Timer channel start trigger registers 0, 1 (TS0, TS1)	0000H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

Remark The SFR and 2nd SFR provided differ depending on the product. Refer to **3.2.4 Special function registers (SFRs)** and **3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

CHAPTER 29 BCD CORRECTION CIRCUIT

29.1 BCD Correction Circuit Function

The BCD correction circuit is mounted onto all 78K0R/Lx3 microcontroller products.

The result of addition/subtraction of the BCD (binary-coded decimal) code and BCD code can be obtained as BCD code with this circuit.

The decimal correction operation result is obtained by performing addition/subtraction having the A register as the operand and then adding/ subtracting the BCDADJ register.

29.2 Registers Used by BCD Correction Circuit

The BCD correction circuit uses the following registers.

- BCD correction result register (BCDADJ)

(1) BCD correction result register (BCDADJ)

The BCDADJ register stores correction values for obtaining the add/subtract result as BCD code through add/subtract instructions using the A register as the operand.

The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags.

BCDADJ is read by an 8-bit memory manipulation instruction.

Reset input sets this register to undefined.

Figure 29-1. Format of BCD Correction Result Register (BCDADJ)

Address: F00FEH After reset: undefined R

Symbol	7	6	5	4	3	2	1	0
BCDADJ								

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 5	Hard	Clock generator	OSTC: Oscillation stabilization time counter status register	The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).	p.213 ☐
	Soft		OSTS: Oscillation stabilization time select register	To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.	p.214 ☐
				Setting the oscillation stabilization time to 20 μs or less is prohibited.	p.214 ☐
				To change the setting of the OSTS register, be sure to confirm that the counting operation of the OSTC register has been completed.	p.214 ☐
				Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.	p.214 ☐
				The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. In the following cases, set the oscillation stabilization time of OSTS to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts. • If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock. • If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after the STOP mode is released.)	p.214 ☐
	Hard			The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).	p.214 ☐
	Soft		CKC: System clock control register	The clock set by CSS, MCM0, SDIV, and MDIV2 to MDIV0 is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time counter, timer array unit (when f_{SUB}/2, f_{SUB}/4, the valid edge of TI0mn input, or the valid edge of INTRTCI is selected as the count clock), clock output/buzzer output, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral operating hardware clock.	p.216 ☐
	Hard			If the peripheral hardware clock is used as the subsystem clock, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 31 ELECTRICAL SPECIFICATIONS.	p.216 ☐
	Soft		DSCCTL: 20 MHz internal high-speed oscillation control register	20 MHz internal oscillation can only be used if $V_{DD} \geq 2.7$ V.	p.218 ☐
				Set SELDSC when 100 μs have elapsed after having set DSCON with $V_{DD} \geq 2.7$ V.	p.218 ☐
				The internal high-speed oscillator must be operated (HIOSTOP = 0) when DSCON = 1.	p.218 ☐
			OSMC: Operation speed mode control register	Write “1” to FSEL before the following two operations. • Changing the clock prior to dividing f_{CLK} to a clock other than f_{IH}. • Operating the DMA controller.	p.221 ☐
				The CPU waits (140.5 clock (f_{CLK})) when “1” is written to the FSEL bit. Interrupt requests issued during a wait will be suspended. However, counting the oscillation stabilization time of f_X can continue even while the CPU is waiting.	p.221 ☐
				To increase f_{CLK} to 10 MHz or higher, set FSEL to “1”, then change f_{CLK} after two or more clocks have elapsed.	p.221 ☐
				Confirm that the clock is operating at 10 MHz or less before setting FSEL = 0.	p.221 ☐