Renesas Electronics America Inc - UPD78F1501AGK-GAK-AX Datasheet

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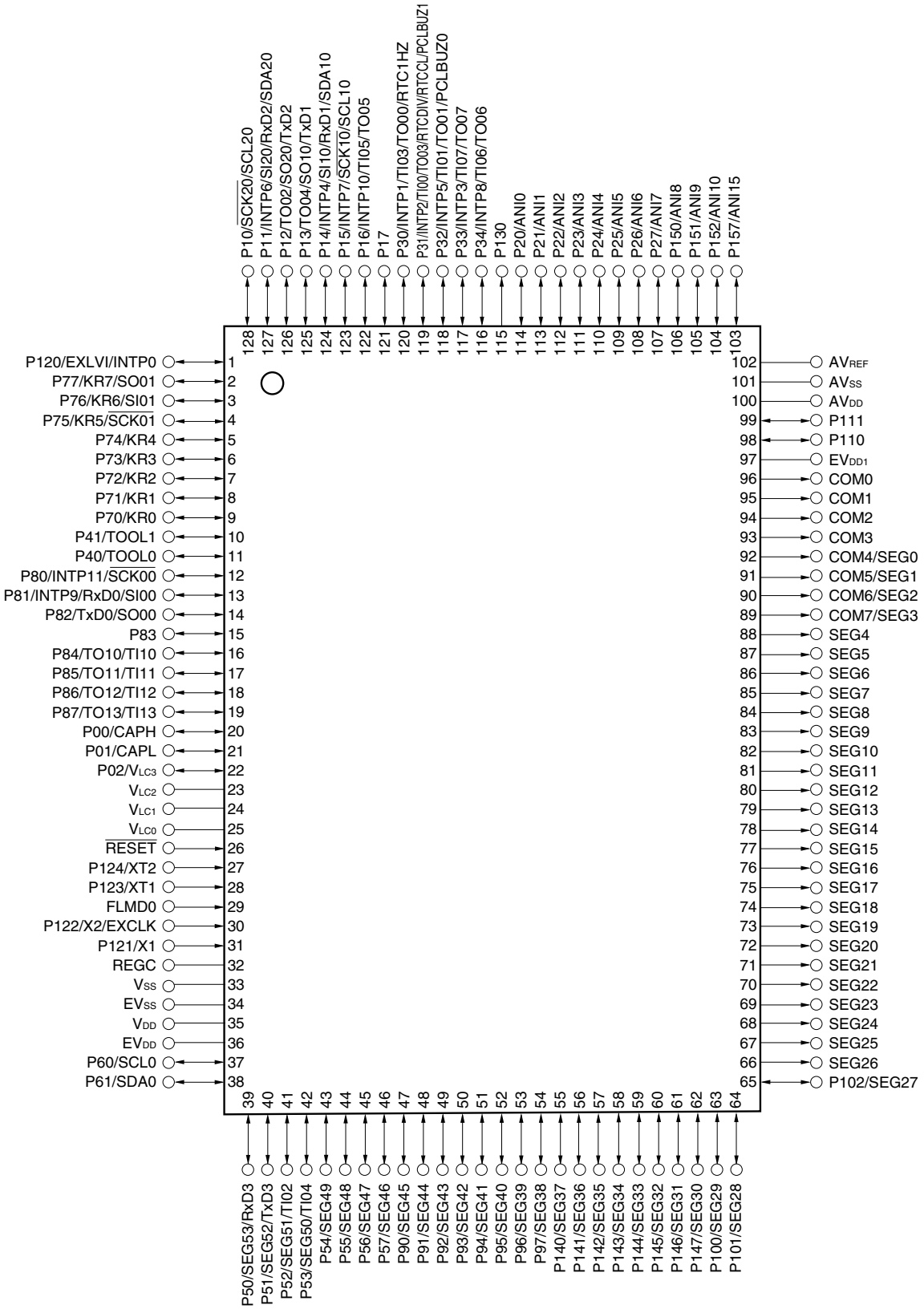
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1501agk-gak-ax

<R> (2) μPD78F151xA



Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Table 2-2. Connection of Unused Pins (78K0R/LF3) (2/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P90/SEG22 to P92/SEG20	17-P	I/O	<When setting to port I/O> Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P100/SEG11			
<R> P110/ANO0 Note 3, P111/ANO1 Note 3	12-A Note 4		Input: Independently connect to AV_{DD1} or AV_{SS} via a resistor. Output: Leave open.
P120/INTP0/EXLVI	8-R	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P121/X1 Note 1	37-C	Input	Independently connect to EV_{DD} or EV_{SS} via a resistor.
P122/X2/EXCLK Note 1			
P123/XT1 Note 1	37-A		
P124/XT2 Note 1			
P130	3-C	Output	Leave open.
P140/SEG19 to P147/SEG12	17-P	I/O	<When setting to port I/O> Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
<R> P157/ANI15/AV_{REFM} Note 2, 3	11-T Note 5	I/O	Input: Independently connect to AV_{DD0} or AV_{SS} via a resistor. Output: Leave open.
SEG0/COM4 to SEG3/COM7	18-F	Output	Leave open.
SEG4 to SEG10	17-T		
COM0 to COM3	18-E		
V_{LC0} to V_{LC2}	–	–	

Notes 1. Use recommended connection above in input port mode (see **Figure 5-2 Format of Clock Operation Mode Control Register (CMC)**) when these pins are not used.

2. P157/ANI15/AV_{REFM} is set in the digital input port mode after release of reset.

<R> **3.** ANOx and AV_{REFM} apply to μPD78F150xA only.

4. μPD78F151xA corresponds to type 5.

5. μPD78F151xA corresponds to type 11-G.

Table 3-5. SFR List (3/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
				1-bit	8-bit	16-bit				
FFF5CH	D/A converter mode register	DAM	R/W	√	√	–	00H	√	√	√
FFF64H	Timer data register 02	TDR02	R/W	–	–	√	0000H	√	√	√
FFF65H										
FFF66H	Timer data register 03	TDR03	R/W	–	–	√	0000H	√	√	√
FFF67H										
FFF68H	Timer data register 04	TDR04	R/W	–	–	√	0000H	√	√	√
FFF69H										
FFF6AH	Timer data register 05	TDR05	R/W	–	–	√	0000H	√	√	√
FFF6BH										
FFF6CH	Timer data register 06	TDR06	R/W	–	–	√	0000H	√	√	√
FFF6DH										
FFF6EH	Timer data register 07	TDR07	R/W	–	–	√	0000H	√	√	√
FFF6FH										
FFF70H	Timer data register 10	TDR10	R/W	–	–	√	0000H	√	√	√
FFF71H										
FFF72H	Timer data register 11	TDR11	R/W	–	–	√	0000H	√	√	√
FFF73H										
FFF74H	Timer data register 12	TDR12	R/W	–	–	√	0000H	√	√	√
FFF75H										
FFF76H	Timer data register 13	TDR13	R/W	–	–	√	0000H	√	√	√
FFF77H										
FFF90H	Sub-count register	RSUBC	R	–	–	√	0000H	√	√	√
FFF91H										
FFF92H	Second count register	SEC	R/W	–	√	–	00H	√	√	√
FFF93H	Minute count register	MIN	R/W	–	√	–	00H	√	√	√
FFF94H	Hour count register	HOUR	R/W	–	√	–	12H[Note]	√	√	√
FFF95H	Week count register	WEEK	R/W	–	√	–	00H	√	√	√
FFF96H	Day count register	DAY	R/W	–	√	–	01H	√	√	√
FFF97H	Month count register	MONTH	R/W	–	√	–	01H	√	√	√
FFF98H	Year count register	YEAR	R/W	–	√	–	00H	√	√	√
FFF99H	Watch error correction register	SUBCUD	R/W	–	√	–	00H	√	√	√
FFF9AH	Alarm minute register	ALARMWM	R/W	–	√	–	00H	√	√	√
FFF9BH	Alarm hour register	ALARMWH	R/W	–	√	–	12H	√	√	√
FFF9CH	Alarm week register	ALARMWW	R/W	–	√	–	00H	√	√	√

Note The value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

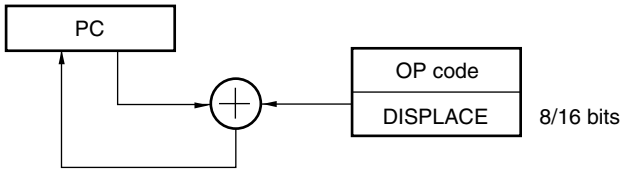
3.3 Instruction Address Addressing

3.3.1 Relative addressing

[Function]

Relative addressing stores in the program counter (PC) the result of adding a displacement value included in the instruction word (signed complement data: −128 to +127 or −32768 to +32767) to the program counter (PC)'s value (the start address of the next instruction), and specifies the program address to be used as the branch destination. Relative addressing is applied only to branch instructions.

Figure 3-14. Outline of Relative Addressing



3.3.2 Immediate addressing

[Function]

Immediate addressing stores immediate data of the instruction word in the program counter, and specifies the program address to be used as the branch destination.

For immediate addressing, CALL !!addr20 or BR !!addr20 is used to specify 20-bit addresses and CALL !addr16 or BR !addr16 is used to specify 16-bit addresses. 0000 is set to the higher 4 bits when specifying 16-bit addresses.

Figure 3-15. Example of CALL !!addr20/BR !!addr20

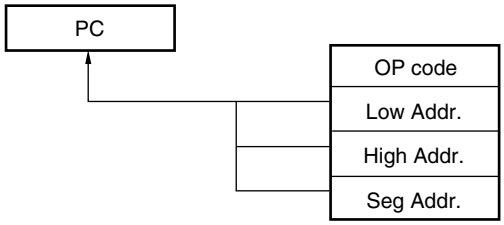


Figure 3-16. Example of CALL !addr16/BR !addr16

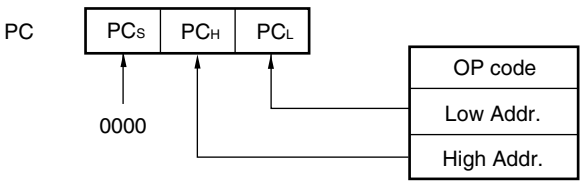


Table 4-6. Setting Functions of ANI0/AMP0-/P20, ANI2/AMP0+/P22, ANI3/AMP1-/P23, ANI5/AMP1+/P25, and ANI6/AMP2-/P26 Pins

ADPC register	PM2 registers	OAENn bit	ADS register	ANI0/AMP0-/P20, ANI2/AMP0+/P22, ANI3/AMP1-/P23, ANI5/AMP1+/P25, and ANI6/AMP2-/P26 Pins
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	Selects ANI.	Setting prohibited
			Does not select ANI.	Operational amplifier input
	Output mode	–	–	Setting prohibited

Table 4-7. Setting Functions of ANI1/AMP0O/P21, ANI4/AMP1O/P24, and ANI7/AMP2O/P27 Pins

ADPC register	PM2 register	OAENn bit	ADS register	ANI1/AMP0O/P21, ANI4/AMP1O/P24, and ANI7/AMP2O/P27 Pins
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	Selects ANI.	Operational amplifier output (to be converted)
			Does not select ANI.	Operational amplifier output (not to be converted)
	Output mode	–	–	Setting prohibited

Remark 78K0R/LF3: n = 0, 1
78K0R/LG3, 78K0R/LH3: n = 0 to 2

Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{IH1}: 1 MHz internal high-speed oscillation clock frequency
f_{IH8}: 8 MHz internal high-speed oscillation clock frequency
f_{IH20}: 20 MHz internal high-speed oscillation clock frequency
f_{EX}: External main system clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency
f_{MAINC}: Main system selection clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{SUB}: Subsystem clock frequency
f_{SUBC}: Subsystem selection clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency
f_{IL}: Internal low-speed oscillation clock frequency

5.3 Registers Controlling Clock Generator

The following eight registers are used to control the clock generator.

- Clock operation mode control register (CMC)
- Clock operation status control register (CSC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- System clock control register (CKC)
- 20 MHz internal high-speed oscillation control register (DSCCTL)
- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)

(1) Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/P121, X2/EXCLK/P122, XT1/P123, and XT2/P124 pins, and to select a gain of the oscillator.

CMC can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Table 5-9. Maximum Number of Clocks Required in f_{MAINC} ↔f_{SUBC}

Set Value Before Switchover		Set Value After Switchover	
CSS		CSS	
		0 (f_{CLK} = f_{MAINC})	1 (f_{CLK} = f_{SUBC})
0 (f_{CLK} = f_{MAINC})	f_{MAINC}>f_{SUBC}		1 + 2f_{MAINC}/f_{SUBC} clock
1 (f_{CLK} = f_{SUBC})	f_{MAINC}>f_{SUBC}	2 + f_{SUBC}/f_{MAINC} clock	

Remarks 1. The number of clocks listed in Table 5-7 to Table 5-9 is the number of CPU clocks before switchover.

2. Calculate the number of clocks in Table 5-7 to Table 5-9 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{IH} = 8 MHz, f_{MX} = 10 MHz)

1 + f_{IH}/f_{MX} = 1 + 8/10 = 1 + 0.8 = 1.8 → 2 clocks

5.6.8 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5-10. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the internal high-speed oscillation clock)	HIOSTOP = 1
X1 clock External main system clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock)	MSTOP = 1
Subsystem clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock)	XTSTOP = 1
20 MHz internal high-speed oscillation clock	SELDSC = 0 (The main system clock is operating on a clock other than the 20 MHz internal high-speed oscillation clock.)	DSCON = 0

Figure 6-56. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN or TAU1EN bits of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSp register. Determines clock frequencies of CKp0 and CKp1.	
Channel default setting	Sets the TMRpq register (determines operation mode of channel). Clears TOEpq to 0 and stops operation of TOpq.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSpq bit to 1. → The TSpq bit automatically returns to 0 because it is a trigger bit.	TEpq = 1, and the TIpq pin start edge detection wait status is set.
	Detects TIpq pin input count start valid edge. →	Clears TCRpq to 0000H and starts counting up.
During operation	Set value of the TDRpq register can be changed. The TCRpq register can always be read. The TSRpq register is not used. Set values of TMRpq, TOMp, TOLp, TOp, and TOEp registers cannot be changed.	When the TIpq pin start edge is detected, the counter (TCRpq) counts up from 0000H. If a capture edge of the TIpq pin is detected, the count value is transferred to TDRpq and INTTMpq is generated. If an overflow occurs at this time, the OVFpq bit of the TSRpq register is set; if an overflow does not occur, the OVFpq bit is cleared. TCRpq stops the count operation until the next TIpq pin start edge is detected.
Operation stop	The TTpq bit is set to 1. → TTpq bit automatically returns to 0 because it is a trigger bit.	TEpq = 0, and count operation stops. TCRpq holds count value and stops. The OVFpq bit of the TSRpq register is also held.
TAU stop	The TAU0EN or TAU1EN bits of PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: p = 0, pq = 00 to 04, 07
78K0R/LG3: p = 0, pq = 00 to 07
78K0R/LH3: p = 0, 1, pq = 00 to 07, 10 to 13

(2) A/D converter mode register (ADM)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

ADM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-5. Format of A/D Converter Mode Register (ADM)

Address: FFF30H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	ADSCM	FR2 Note 1	FR1 Note 1	FR0 Note 1	LV1 Note 1	LV0 Note 1	ADCE

ADCS	A/D conversion operation control Notes 2, 3, 4
0	Stops conversion operation
1	Enables conversion operation

ADSCM	A/D conversion operation mode specification
0	Continuous conversion mode
1	Single conversion mode

ADCE	A/D voltage comparator operation control Note 4
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Notes 1. For details of FR2 to FR0, LV1, LV0, and A/D conversion, see **Table 10-2 A/D Conversion Time Selection**.

2. When using the A/D converter in timer trigger mode, do not set ADCS to 1. (ADCS automatically switches to 1 when a timer trigger signal is generated.) However, ADCS may be set to 0 to stop A/D conversion.

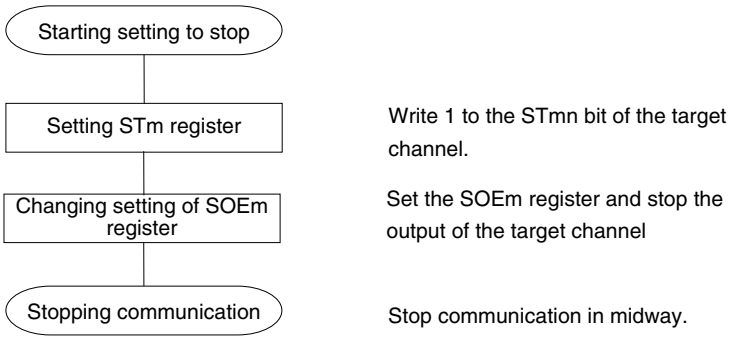
3. Read ADCS to determine whether A/D conversion is under execution.

4. The operation of the A/D voltage comparator is controlled by ADCS and ADCE, and it takes 1 μs from operation start to operation stabilization. Therefore, when ADCS is set to 1 after 1 μs or more has elapsed from the time ADCE is set to 1, the conversion result at that time has priority over the first conversion result. Otherwise, ignore data of the first conversion.

Table 10-1. Settings of ADCS and ADCE

ADCS	ADCE	A/D Conversion Operation
0	0	Stop status (DC power consumption path does not exist)
0	1	Conversion waiting mode (A/D voltage comparator operation, only comparator consumes power)
1	0	Setting prohibited
1	1	Conversion mode (A/D voltage comparator operation)

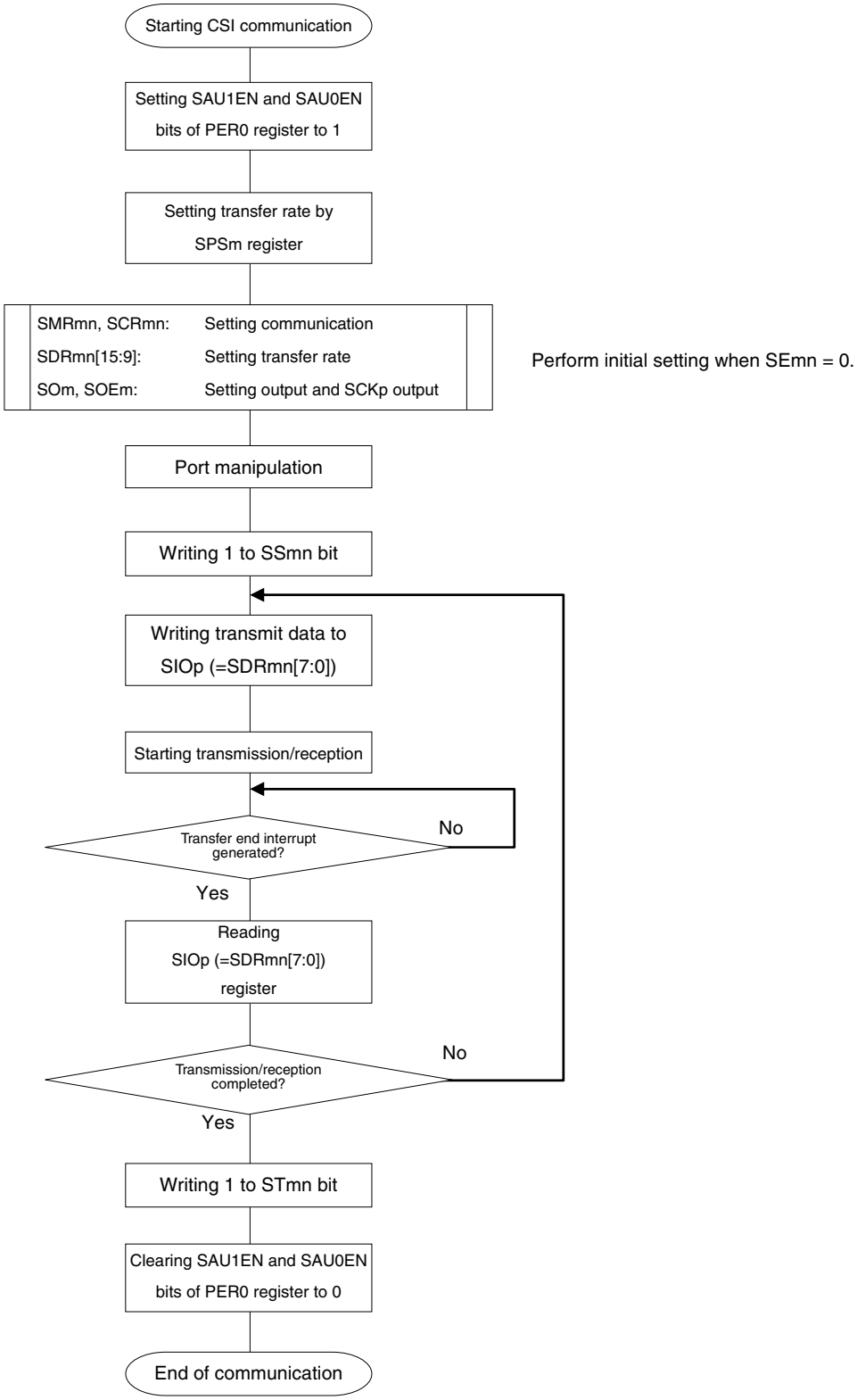
Figure 14-26. Procedure for Stopping Master Transmission



Remarks 1. Even after communication is stopped, the pin level is retained. To resume the operation, re-set the SOm register (see **Figure 14-27 Procedure for Resuming Master Transmission**).

2. p: CSI number (p = 00, 01, 10, 20)

Figure 14-43. Flowchart of Master Transmission/Reception (in Single- Transmission/Reception Mode)

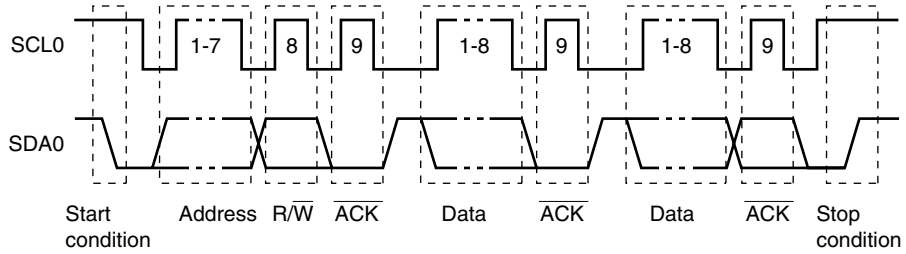


Caution After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

15.5 I^2C Bus Definitions and Control Methods

The following section describes the I^2C bus's serial data communication format and the signals used by the I^2C bus. Figure 15-14 shows the transfer timing for the "start condition", "address", "data", and "stop condition" output via the I^2C bus's serial data bus.

Figure 15-14. I^2C Bus Serial Data Transfer Timing



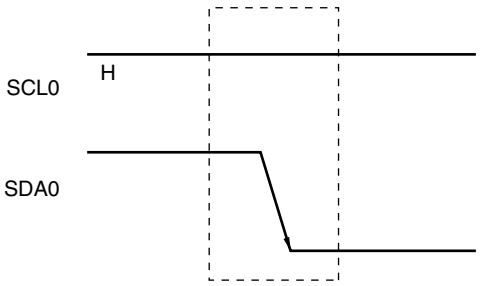
The master device generates the start condition, slave address, and stop condition.
The acknowledge ($\overline{ACK}$) can be generated by either the master or slave device (normally, it is output by the device that receives 8-bit data).

The serial clock (SCL0) is continuously output by the master device. However, in the slave device, the SCL0's low level period can be extended and a wait can be inserted.

15.5.1 Start conditions

A start condition is met when the SCL0 pin is at high level and the SDA0 pin changes from high level to low level. The start conditions for the SCL0 pin and SDA0 pin are signals that the master device generates to the slave device when starting a serial transfer. When the device is used as a slave, start conditions can be detected.

Figure 15-15. Start Conditions



A start condition is output when bit 1 (STT) of IICA control register 0 (IICCTL0) is set (1) after a stop condition has been detected (SPD: Bit 0 of the IICA status register (IICS) = 1). When a start condition is detected, bit 1 (STD) of IICS is set (1).

15.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the 78K0R/Lx3 microcontrollers as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the 78K0R/Lx3 microcontrollers take part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the 78K0R/Lx3 microcontrollers loose in arbitration and are specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

An example of when the 78K0R/Lx3 microcontrollers are used as the I^2C bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICA interrupt occurrence (communication waiting). When an INTIICA interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

16.2 Configuration of LCD Controller/Driver

The LCD controller/driver consists of the following hardware.

Table 16-2. Configuration of LCD Controller/Driver

Item	Configuration
Display outputs	78K0R/LF3: 31 segment signals[Note] (SEG0 to SEG30), 8 common signals[Note] (COM0 to COM7) 78K0R/LG3: 40 segment signals[Note] (SEG0 to SEG39), 8 common signals[Note] (COM0 to COM7) 78K0R/LH3: 54 segment signals[Note] (SEG0 to SEG53), 8 common signals[Note] (COM0 to COM7)
Control registers	LCD mode register (LCDMD) LCD display mode register (LCDM) LCD clock control register 0 (LCDC0) LCD boost level control register (VLCD) Port function register (PFALL) Segment enable register (SEGEN) Input switch control register (ISC)

Note The four segment signal outputs (SEG0 to SEG3) and four common signal outputs (COM4 to COM7) are alternate-function pins. COM4 to COM7 can be used only when eight-time-slice mode is selected by the setting of the LCD display mode register (LCDM).

Figure 16-7. Format of Segment Enable Register (SEGEN)

• 78K0R/LF3

Address: F0081H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SEGEN	0	0	0	0	0	0	0	SEGEN0

• 78K0R/LG3

Address: F0081H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SEGEN	0	0	0	0	0	0	SEGEN1	SEGEN0

• 78K0R/LH3

Address: F0081H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SEGEN	0	0	0	SEGEN4	SEGEN3	SEGEN2	SEGEN1	SEGEN0

SEGENn	Output enable/disable to segment output only pins (n = 0 to 4)
0	Disables segment output
1	Enables segment output

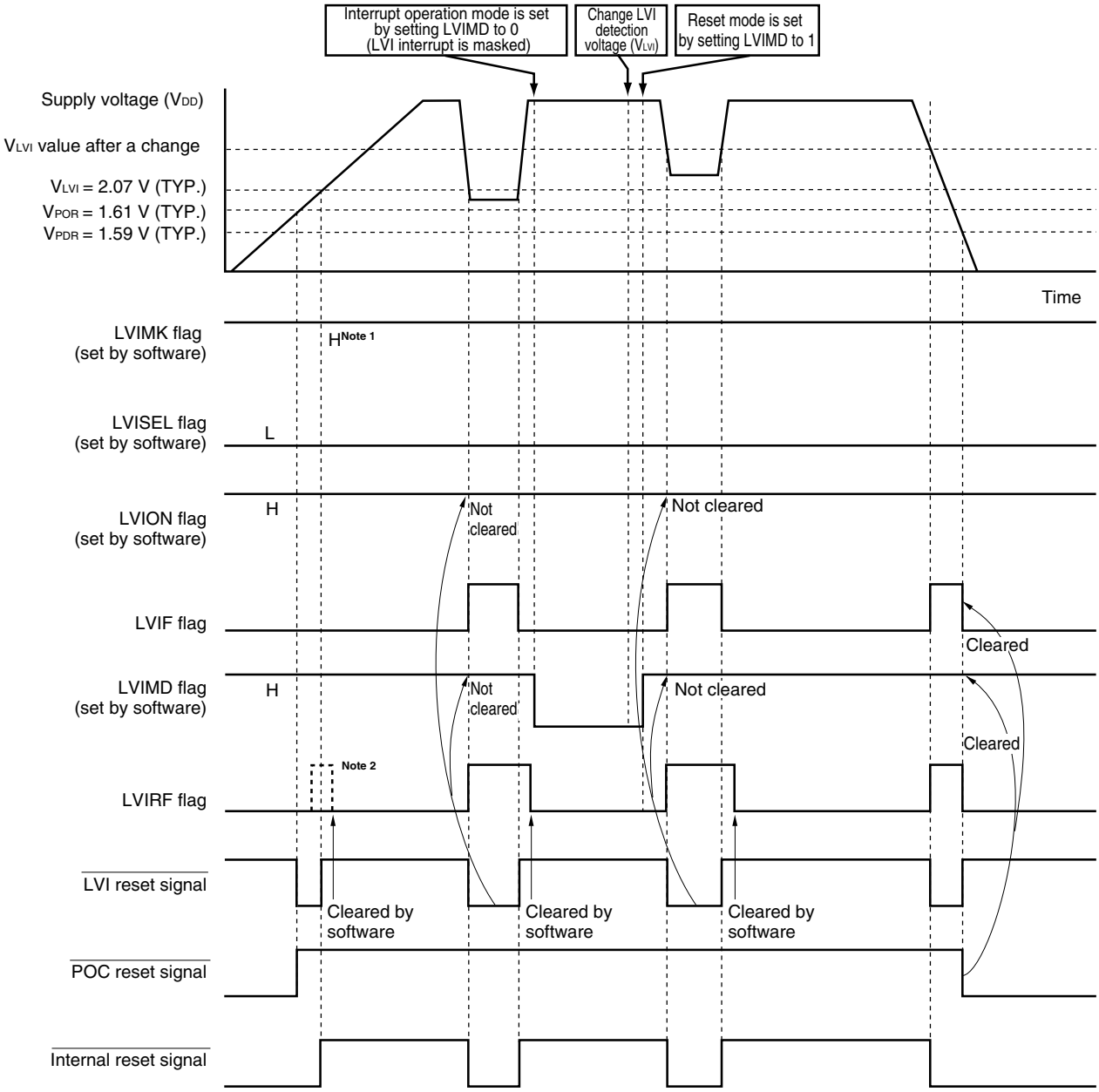
Cautions 1. SEGEN can be written only once after reset release.

2. For 78K0R/LF3, bits 1 to 7 must be set to 0. For 78K0R/LG3, bits 2 to 7 must be set to 0. For 78K0R/LH3, bits 5 to 7 must be set to 0.

The segment output only pins operated by SEGEN4 to SEGEN0 are as follows.

SEGEN register	Segment output only pins		
	78K0R/LF3	78K0R/LG3	78K0R/LH3
SEGE4	–	–	SEG24 to SEG26 pins
SEGE3	–	–	SEG20 to SEG23 pins
SEGE2	–	–	SEG16 to SEG19 pins
SEGE1	–	SEG12 to SEG14 pins	SEG12 to SEG15 pins
SEGE0	SEG8 to SEG10 pins	SEG8 to SEG11 pins	SEG8 to SEG11 pins

Figure 24-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 0)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. LVIRF is bit 0 of the reset control flag register (RESF).
When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, the LVIRF flag may become 1 from the beginning due to the power-on waveform.
For details of RESF, see **CHAPTER 22 RESET FUNCTION**.

Remark V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 31	Hard	Electrical specifications	–	The 78K0R/Lx3 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.	p.877 ☐
				The pins mounted depend on the product. Refer to 1.3 Pin Configuration (Top View) and CHAPTER 2 PIN FUNCTIONS.	p.877 ☐
			Absolute maximum ratings	Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.	pp.878 to 880 ☐
				The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.	pp.879 ☐
			X1 oscillator characteristics	When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance. • Keep the wiring length as short as possible. • Do not cross the wiring with the other signal lines. • Do not route the wiring near a signal line through which a high fluctuating current flows. • Always make the ground point of the oscillator capacitor the same potential as V_{SS}. • Do not ground the capacitor to a ground pattern through which a high current flows. • Do not fetch signals from the oscillator.	p.880 ☐
				Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.	p.880 ☐
			XT1 oscillator characteristics	When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance. • Keep the wiring length as short as possible. • Do not cross the wiring with the other signal lines. • Do not route the wiring near a signal line through which a high fluctuating current flows. • Always make the ground point of the oscillator capacitor the same potential as V_{SS}. • Do not ground the capacitor to a ground pattern through which a high current flows. • Do not fetch signals from the oscillator.	p.881 ☐
				The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.	p.881 ☐
			Recommended oscillator circuit constants	The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/Lx3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.	pp.882 , 883 ☐

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Edition	Description	Chapter
4th Edition	Addition of example of calculation of LCD frame frequency to (c) and (d) of **Figure 16-13. Common Signal Waveforms (2/2)**	**CHAPTER 16 LCD CONTROLLER/ DRIVER**
	Change of **Caution** of **Figure 16-31. Examples of LCD Drive Power Connections (External Resistance Division Method)**	
	Change the capacitance value of external capacitors to 0.47 μF±30% in **16.8.2 Internal voltage boosting method** and **16.8.3 Capacitor split method**	
	Addition of **Note** to **Figure 18-4. Format of DMA Mode Control Register n (DMCn) (1/2)**	**CHAPTER 18 DMA CONTROLLER**
	Change of description of **Figure 18-7. Example of Setting for CSI Consecutive Transmission**	
	Addition of **18.5.2 CSI master reception** and **18.5.3 CSI transmission/reception**	
	Change of **18.5.6 Holding DMA transfer pending by DWAITn** and addition of **Caution**	
	Change of **18.5.7 Forced termination by software**	
	Change of **18.6 Cautions on Using DMA Controller**	
	Change value of maskable interrupts of 78K0R/LF3	**CHAPTER 19 INTERRUPT FUNCTIONS**
	Change of **Figure 26-1. Format of User Option Byte (000C0H/010C0H) (1/2)**	**CHAPTER 26 OPTION BYTE**
	Change of **26.4 Setting of Option Byte**	
	Addition of **Figure 27-3. Example of Wiring Adapter for Flash Memory Writing (μPD78F1508A)**	**CHAPTER 27 FLASH MEMORY**
	Addition of **27.9 Creating ROM Code to Place Order for Previously Written Product**	
	Change of Examples 2 in **29.3 BCD Correction Circuit Operation**	**CHAPTER 29 BCD CORRECTION CIRCUIT**
	Change of **Table 30-5. Operation List**	**CHAPTER 30 INSTRUCTION SET**
	Deletion of (TARGET)	**CHAPTER 31 ELECTRICAL SPECIFICATIONS**
	Change of analog output voltage, output current, high, and output current, low in **Absolute Maximum Ratings (T_A = 25°C)**	
	Change of **Internal Oscillator Characteristics**	
	Addition of **Recommended oscillator circuit constants**	
	Change of output voltage, low (V_{OL2}), supply current, and operating current of **DC Characteristics**	
	Change of **Caution** of **(1) Basic operation (3/6)** in **AC Characteristics**	
	Change of **(b) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)** of **(2) Serial interface: Serial array unit (2/18)** and addition of **Note 1**	
	Change of **(c) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)** of **(2) Serial interface: Serial array unit (3/18)**	
	Change of **(d) During communication at same potential (simplified I^2C mode)** of **(2) Serial interface: Serial array unit (5/18)**	
	Change of **(f) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)** of **(2) Serial interface: Serial array unit (11/18)** and addition of **Note 1**	