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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1502agk-gak-ax

(2) Non-port functions (3/4) : 78K0R/LF3

Function Name	I/O	Function	After Reset	Alternate Function
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P14/SI10/RxD1/ INTP4
SDA20				P11/SI20/RxD2/ INTP6
SI10		Serial data input to CSI10		P14/RxD1/SDA10/ INTP4
SI20		Serial data input to CSI20		P11/RxD2/SDA20/ INTP6
SO10	Output	Serial data output from CSI10	Input port	P13/TxD1/TO04
SO20		Serial data output from CSI20		P12/TxD2/TO02
TI00	Input	External count clock input to 16-bit timer 00	Input port	P31/TO03/RTCDIV/ RTCCL/PCLBUZ1/ INTP2
TI01		External count clock input to 16-bit timer 01		P32/TO01/INTP5/ PCLBUZ0
TI02		External count clock input to 16-bit timer 02		P52/SEG28
TI03		External count clock input to 16-bit timer 03		P30/TO00/RTC1HZ/ INTP1
TI04		External count clock input to 16-bit timer 04		P53/SEG27
TI07		External count clock input to 16-bit timer 07		P33/TO07/INTP3
TO00	Output	16-bit timer 00 output	Input port	P30/TI03/RTC1HZ/ INTP1
TO01		16-bit timer 01 output		P32/TI01/INTP5/ PCLBUZ0
TO02		16-bit timer 02 output		P12/SO20/TxD2
TO03		16-bit timer 03 output		P31/TI00/RTCDIV/ RTCCL/PCLBUZ1/ INTP2
TO04		16-bit timer 04 output		P13/SO10/TxD1
TO07		16-bit timer 07 output		P33/TI07/INTP3
TxD1	Output	Serial data output from UART1	Input port	P13/SO10/TO04
TxD2		Serial data output from UART2		P12/SO20/TO02
TxD3		Serial data output from UART3		P51/SEG29
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
V_{DD}	–	Positive power supply (Pins other than port and $\overline{RESET}$, FLMD0 pins)	–	–
EV_{DD}	–	Positive power supply for $\overline{RESET}$, FLMD0 pins, and port pins other than P20 to P26, P110, P111, P157	–	–

2.2 Description of Pin Functions

Remark The pins mounted depend on the product. Refer to **1.3 Pin Configuration (Top View)** and **2.1 Pin Function List**.

2.2.1 P00 to P02

P00 to P02 function as an I/O port. This port can also be used for connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P00/CAPH	√		
P01/CAPL	√		
P02/V_{LC3}	√		

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 to P02 function as an I/O port. P00 to P02 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P02 function as connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

(a) CAPH, CAPL

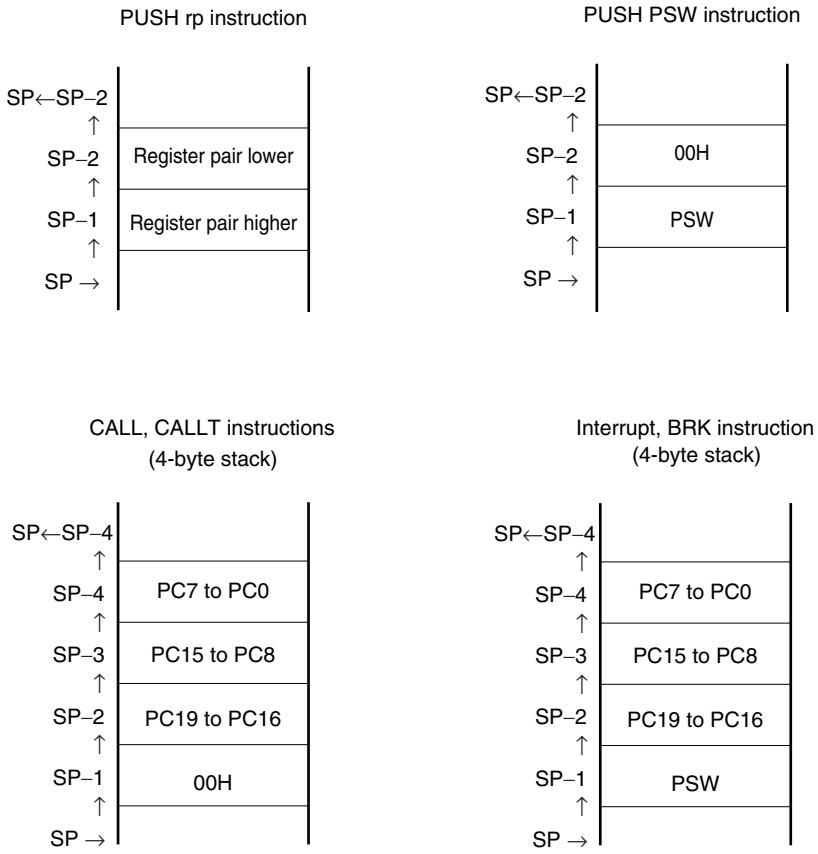
These are the pins for connecting a capacitor for LCD controller/driver.

(b) V_{LC3}

This is the pin for inputting a power supply voltage pin for driving the LCD.

Caution To use P00/CAPH, P01/CAPL, and P02/V_{LC3} as a general-purpose port, set bit 5 (MDSET1) and bit 4 (MDSET0) of LCD mode register (LCDMD) to "0", which is the same as their default status setting.

Figure 3-11. Data to Be Saved to Stack Memory



3.2.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FFEE0H to FFEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

These registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupts for each bank.

Caution It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

Table 3-6. Extended SFR (2nd SFR) List (4/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
					1-bit	8-bit	16-bit				
F0174H	Serial output level register 1	SOL1L	SOL1	R/W	–	√	√	0000H	√	√	√
F0175H		–			–	–			√	√	√
F0180H	Timer counter register 00	TCR00		R	–	–	√	FFFFH	√	√	√
F0181H											
F0182H	Timer counter register 01	TCR01		R	–	–	√	FFFFH	√	√	√
F0183H											
F0184H	Timer counter register 02	TCR02		R	–	–	√	FFFFH	√	√	√
F0185H											
F0186H	Timer counter register 03	TCR03		R	–	–	√	FFFFH	√	√	√
F0187H											
F0188H	Timer counter register 04	TCR04		R	–	–	√	FFFFH	√	√	√
F0189H											
F018AH	Timer counter register 05	TCR05		R	–	–	√	FFFFH	√	√	√
F018BH											
F018CH	Timer counter register 06	TCR06		R	–	–	√	FFFFH	√	√	√
F018DH											
F018EH	Timer counter register 07	TCR07		R	–	–	√	FFFFH	√	√	√
F018FH											
F0190H	Timer mode register 00	TMR00		R/W	–	–	√	0000H	√	√	√
F0191H											
F0192H	Timer mode register 01	TMR01		R/W	–	–	√	0000H	√	√	√
F0193H											
F0194H	Timer mode register 02	TMR02		R/W	–	–	√	0000H	√	√	√
F0195H											
F0196H	Timer mode register 03	TMR03		R/W	–	–	√	0000H	√	√	√
F0197H											
F0198H	Timer mode register 04	TMR04		R/W	–	–	√	0000H	√	√	√
F0199H											
F019AH	Timer mode register 05	TMR05		R/W	–	–	√	0000H	√	√	√
F019BH											
F019CH	Timer mode register 06	TMR06		R/W	–	–	√	0000H	√	√	√
F019DH											
F019EH	Timer mode register 07	TMR07		R/W	–	–	√	0000H	√	√	√
F019FH											
F01A0H	Timer status register 00	TSR00L	TSR00	R	–	√	√	0000H	√	√	√
F01A1H		–			–	–			√	√	√
F01A2H	Timer status register 01	TSR01L	TSR01	R	–	√	√	0000H	√	√	√
F01A3H		–			–	–			√	√	√
F01A4H	Timer status register 02	TSR02L	TSR02	R	–	√	√	0000H	√	√	√
F01A5H		–			–	–			√	√	√

3.4 Addressing for Processing Data Addresses

3.4.1 Implied addressing

[Function]

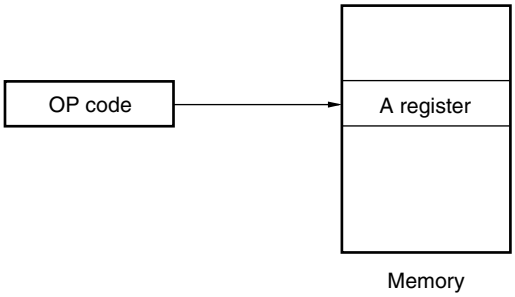
Instructions for accessing registers (such as accumulators) that have special functions are directly specified with the instruction word, without using any register specification field in the instruction word.

[Operand format]

Because implied addressing can be automatically employed with an instruction, no particular operand format is necessary.

Implied addressing can be applied only to MULU X.

Figure 3-19. Outline of Implied Addressing



3.4.2 Register addressing

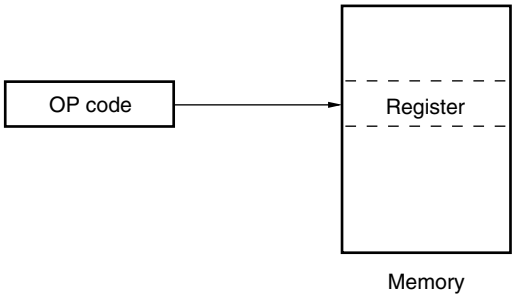
[Function]

Register addressing accesses a general-purpose register as an operand. The instruction word of 3-bit long is used to select an 8-bit register and the instruction word of 2-bit long is used to select a 16-bit register.

[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

Figure 3-20. Outline of Register Addressing



3.4.7 Based addressing

[Function]

Based addressing uses the contents of a register pair specified with the instruction word as a base address, and 8-bit immediate data or 16-bit immediate data as offset data. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL + byte], [DE + byte], [SP + byte] (only the space from F0000H to FFFFFH is specifiable)
–	word[B], word[C] (only the space from F0000H to FFFFFH is specifiable)
–	word[BC] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL + byte], ES:[DE + byte] (higher 4-bit addresses are specified by the ES register)
–	ES:word[B], ES:word[C] (higher 4-bit addresses are specified by the ES register)
–	ES:word[BC] (higher 4-bit addresses are specified by the ES register)

Figure 3-27. Example of [SP+byte]

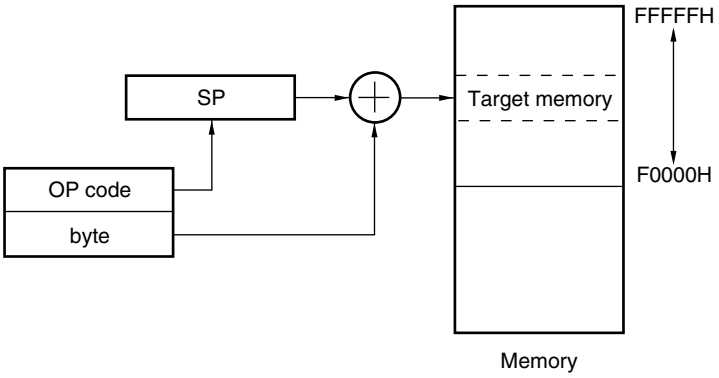


Table 4-4. Port functions (78K0R/LH3) (2/3)

Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG53/RxD3
P51				SEG52/TxD3
P52				SEG51/TI02
P53				SEG50/TI04
P54 to P57				SEG49 to SEG46
P60	I/O	Port 6. 2-bit I/O port. Output is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P70 to P74	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Input of P75 and P76 can be set to TTL buffer. Output of P75 and P77 can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR4
P75				KR5/$\overline{SCK01}$
P76				KR6/SI01
P77				KR7/SO01
P80	I/O	Port 8. 8-bit I/O port. Inputs/output can be specified in 1-bit units. Output of P80 and P82 can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$/INTP11
P81				RxD0/SI00/INTP9
P82				TxD0/SO00
P83				–
P84				TI10/TO10
P85				TI11/TO11
P86				TI12/TO12
P87				TI13/TO13
P90 to P97	I/O	Port 9. 8-bit I/O port. Inputs/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG45 to SEG38
P100 to P102	I/O	Port 10. 3-bit I/O port. Inputs/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG29 to SEG27
<R> P110	I/O	Port 11. 2-bit I/O port. Inputs/output can be specified in 1-bit units.	Input port	ANO0 Note
P111				ANO1 Note
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2

<R> **Note** ANOx applies to μPD78F150xA only.

(7) Peripheral enable register 0 (PER0)

This register is used to enable or disable use of each peripheral hardware macro. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

PER0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears theses registers to 00H.

Figure 5-8. Format of Peripheral Enable Register 0 (PER0) (1/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	DACEN	ADCEN	IICAEN[Note 1]	SAU1EN	SAU0EN	TAU1EN	TAU0EN

RTCEN	Control of real-time counter (RTC) input clock[Note 2]
0	Stops input clock supply. • SFR used by the real-time counter (RTC) cannot be written. • The real-time counter (RTC) is in the reset status.
1	Supplies input clock. • SFR used by the real-time counter (RTC) can be read and written.

DACEN	Control of D/A converter input clock
0	Stops input clock supply. • SFR used by the D/A converter cannot be written. • The D/A converter is in the reset status.
1	Supplies input clock. • SFR used by the D/A converter can be read and written.

ADCEN	Control of A/D converter, operational amplifier, and voltage reference input clock
0	Stops input clock supply. • SFR used by the A/D converter, operational amplifier, and voltage reference cannot be written. • The A/D converter, operational amplifier, and voltage reference is in the reset status.
1	Supplies input clock. • SFR used by the A/D converter, operational amplifier, and voltage reference can be read and written.

IICAEN	Control of serial interface IICA input clock
0	Stops input clock supply. • SFR used by the serial interface IICA cannot be written. • The serial interface IICA is in the reset status.
1	Supplies input clock. • SFR used by the serial interface IICA can be read and written.

Notes 1. 78K0R/LG3, 78K0R/LH3 only

2. By using RTCEN, can supply and stop the clock that is used when accessing the real-time counter (RTC) from the CPU. RTCEN cannot control supply of the operating clock (f_{SUB}) to RTC.

(17) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P30/RTC1HZ/TO00/TI03/INTP1 pin for real-time counter correction clock output, the P31/RTCDIV/RTCCL/TI00/TO03/PCLBUZ1/INTP2 pin for real-time counter clock output, set PM30, PM31 and the output latches of P30, P31 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM3 to FFH.

Figure 7-18. Format of Port Mode Register 3 (PM3)

- 78K0R/LF3

Address: FFF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	PM33	PM32	PM31	PM30

- 78K0R/LG3, 78K0R/LH3

Address: FFF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

8.4 Operation of Watchdog Timer

8.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (000C0H).

   - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (000C0H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 26**).

WDTON	Watchdog Timer Counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

   - Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H) (for details, see **8.4.2** and **CHAPTER 26**).
   - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (000C0H) (for details, see **8.4.3** and **CHAPTER 26**).

2. After a reset release, the watchdog timer starts counting.
3. By writing “ACH” to WDTE after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
4. After that, write WDTE the second time or later after a reset release during the window open period. If WDTE is written during a window close period, an internal reset signal is generated.
5. If the overflow time expires without “ACH” written to WDTE, an internal reset signal is generated.
   An internal reset signal is generated in the following cases.

   - If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
   - If data other than “ACH” is written to WDTE

Cautions 1. When data is written to WDTE for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

2. If the watchdog timer is cleared by writing “ACH” to WDTE, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f_{IL} seconds.

3. The watchdog timer can be cleared immediately before the count value overflows.

<Example> When the overflow time is set to $2^{10}/f_{IL}$, writing “ACH” is valid up to count value 3FH.

15.5.4 Acknowledge ($\overline{ACK}$)

$\overline{ACK}$ is used to check the status of serial data at the transmission and reception sides.

The reception side returns $\overline{ACK}$ each time it has received 8-bit data.

The transmission side usually receives $\overline{ACK}$ after transmitting 8-bit data. When $\overline{ACK}$ is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether $\overline{ACK}$ has been detected can be checked by using bit 2 (ACKD) of the IICA status register (IICS).

When the master receives the last data item, it does not return $\overline{ACK}$ and instead generates a stop condition. If a slave does not return $\overline{ACK}$ after receiving data, the master outputs a stop condition or restart condition and stops transmission. If $\overline{ACK}$ is not returned, the possible causes are as follows.

<1> Reception was not performed normally.
<2> The final data item was received.
<3> The reception side specified by the address does not exist.

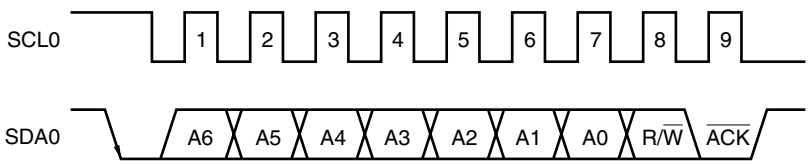
To generate $\overline{ACK}$, the reception side makes the SDA0 line low at the ninth clock (indicating normal reception).

Automatic generation of $\overline{ACK}$ is enabled by setting bit 2 (ACKE) of IICA control register 0 (IICCTL0) to 1. Bit 3 (TRC) of the IICS register is set by the data of the eighth bit that follows 7-bit address information. Usually, set ACKE to 1 for reception (TRC = 0).

If a slave can receive no more data during reception (TRC = 0) or does not require the next data item, then the slave must inform the master, by clearing ACKE to 0, that it will not receive any more data.

When the master does not require the next data item during reception (TRC = 0), it must clear ACKE to 0 so that $\overline{ACK}$ is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

Figure 15-18. $\overline{ACK}$



When the local address is received, $\overline{ACK}$ is automatically generated, regardless of the value of ACKE. When an address other than that of the local address is received, $\overline{ACK}$ is not generated (NACK).

When an extension code is received, $\overline{ACK}$ is generated if ACKE is set to 1 in advance.

How $\overline{ACK}$ is generated when data is received differs as follows depending on the setting of the wait timing.

- When 8-clock wait state is selected (bit 3 (WTIM) of IICCTL0 register = 0):
  By setting ACKE to 1 before releasing the wait state, $\overline{ACK}$ is generated at the falling edge of the eighth clock of the SCL0 pin.
- When 9-clock wait state is selected (bit 3 (WTIM) of IICCTL0 register = 1):
  $\overline{ACK}$ is generated by setting ACKE to 1 in advance.

The meanings of <1> to <6> in (1) Start condition ~ address ~ data in Figure 15-32 are explained below.

<1> The start condition trigger is set by the master device (STT = 1) and a start condition (SDA0 = 0 and SCL0 = 1) is generated once the bus data line goes low (SDA0 = 0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS = 1). The master device is ready to communicate once the bus clock line goes low (SCL0 = 0) after the hold time has elapsed.

<2> The master device writes the address + W (transmission) to the IICA shift register (IICA) and transmits the slave address.

<3> If the address received matches the address of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock, and the slave device whose address matched the transmitted slave address also issues an interrupt (INTIICA: address match). The master device and slave device also set a wait status (SCL0 = 0)[Note] when the addresses match.

<5> The master device writes the data to transmit to the IICA register and releases the wait status that it set by the master device.

<6> If the slave device releases the wait status (WREL = 1), the master device starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

18.5.2 CSI master reception

A flowchart showing an example of setting for CSI master reception is shown below.

- Master reception (256 bytes) of CSI00
- DMA channel 0 is used to read received data and DMA channel 1 is used to write dummy data.
- DMA start source: INTCSI00
  (If the same start source is specified for DMA channels 0 and 1, the data of channel 0 is transferred, and then that of channel 1.)
- Interrupt of CSI00 is specified by IFC03 to IFC00 = IFC13 to IFC10 (bits 3 to 0 of the DMCn register) = 0110B.
- Data is transferred (received) from FFF10H of the CSI data register (SIO00) to FF100H to FF1FFH of RAM (256 bytes). (In successive reception mode, the data that is to be received when the first buffer empty interrupt occurs is invalid because the data has not been received.)
- Transfers dummy data FF101H to FF1FFH (255 bytes) of RAM to FFF10H of the data register (SIO00) of CSI.
  (Dummy data is written to the first byte by using software (an instruction).)

CHAPTER 21 STANDBY FUNCTION

21.1 Standby Function and Configuration

21.1.1 Standby function

The standby function is mounted onto all 78K0R/Lx3 microcontroller products.

The standby function reduces the operating current of the system, and the following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, 20 MHz internal high-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The STOP mode cannot be set while the CPU operates with the subsystem clock. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

4. It can be selected by the option byte whether the internal low-speed oscillator continues oscillating or stops in the HALT or STOP mode. For details, see CHAPTER 26 OPTION BYTE.

5. The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.

21.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATOR**.

Table 22-2. Hardware Statuses After Reset Acknowledgment (4/4)

Hardware		Status After Reset Acknowledgment[Note 1]
Reset function	Reset control flag register (RESF)	Undefined[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 3]
	Low-voltage detection level select register (LVIS)	0EH[Note 2]
DMA controller	SFR address registers 0, 1 (DSA0, DSA1)	00H
	RAM address registers 0L, 0H, 1L, 1H (DRA0L, DRA0H, DRA1L, DRA1H)	00H
	Byte count registers 0L, 0H, 1L, 1H (DBC0L, DBC0H, DBC1L, DBC1H)	00H
	Mode control registers 0, 1 (DMC0, DMC1)	00H
	Operation control registers 0, 1 (DRC0, DRC1)	00H
Interrupt	Request flag registers 0L, 0H, 1L, 1H, 2L, 2H (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)	00H
	Mask flag registers 0L, 0H, 1L, 1H, 2L, 2H (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)	FFH
	Priority specification flag registers 00L, 00H, 01L, 01H, 02L, 02H, 10L, 10H, 11L, 11H, 12L, 12H (PR00L, PR00H, PR01L, PR01H, PR10L, PR10H, PR11L, PR11H, PR02L, PR02H, PR12L, PR12H)	FFH
	External interrupt rising edge enable registers 0, 1 (EGP0, EGP1)	00H
	External interrupt falling edge enable registers 0, 1 (EGN0, EGN1)	00H
Regulator	Regulator mode control register (RMC)	00H
BCD correction circuit (BCD)	BCD correction result register (BCDADJ)	Undefined

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by LVI
RESF	TRAP bit	Cleared (0)	Cleared (0)	Set (1)	Held	Held
	WDRF bit			Held	Set (1)	Held
	LVIRF bit			Held	Held	Set (1)
LVIS		Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Held

3. This value varies depending on the reset source and the option byte.

Remark The SFR and 2nd SFR mounted depend on the product. Refer to **3.2.4 Special function registers (SFRs)** and **3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

DC Characteristics (2/11)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{DD0} ≤ V_{DD}, 1.8 V ≤ AV_{DD1} ≤ V_{DD}, 1.8 V ≤ AV_{DD} ≤ V_{DD}, 1.8 V ≤ EV_{DD1} = V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P02, P12, P13, P16, P17, P30 to P34, P40, P41, P70 to P77, P80 to P87, P120, P130	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.5	mA
		Per pin for P10, P11, P14, P15	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6	mA
		Per pin for P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Per pin for P50 to P57, P90 to P97, P100 to P102, P140 to P147	4.0 V ≤ V_{DD} ≤ 5.5 V			1.8	mA
			2.7 V ≤ V_{DD} < 4.0 V			0.8	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.35	mA
		Total of P00 to P02, P10 to P17, P30 to P34, P40, P41, P70 to P77, P80 to P87, P120, P130 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P60, P61 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			6.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			4.0	mA
		Total of P50 to P57, P90 to P97, P100 to P102, P140 to P147 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			14.4	mA
			2.7 V ≤ V_{DD} < 4.0 V			6.4	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.8	mA
		Total of all pins (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			64.4	mA
			2.7 V ≤ V_{DD} < 4.0 V			27.4	mA
			1.8 V ≤ V_{DD} < 2.7 V			15.8	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P152, P157				0.4	mA
		Per pin for P110, P111				0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to V_{SS} and AV_{SS} pin.

2. Specification under conditions where the duty factor is 60% or 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

•Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OL} = 20.0 mA

Total output current of pins = (20.0 × 0.7)/(50 × 0.01) = 28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (11/11)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{DD0} ≤ V_{DD}, 1.8 V ≤ AV_{DD1} ≤ V_{DD}, 1.8 V ≤ AV_{DD} ≤ V_{DD}, 1.8 V ≤ EV_{DD1} = V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Operational amplifier operating current	I_{AMP} Note 1, 6	AV_{DD0} = 5.0 V		OAIMI = 0		250	335	μA
		AV_{DD0} = 3.0 V		OAIMI = 0		230	320	μA
		AV_{DD0} = 2.3 V		OAIMI = 0		220	310	μA
Voltage reference operating current 1	I_{VR1} Note 2, 6	AV_{DD0} = 5.0 V				19	38	μA
		AV_{DD0} = 3.0 V		VR output = 2.5 V		9.5	25	μA
		AV_{DD0} = 3.0 V		VR output = 2.0 V		9.5	25	μA
Voltage reference operating current 2	I_{VR2} Note 3, 6	V_{DD} = 5.0 V				10	40	μA
		V_{DD} = 3.0 V		VR output = 2.5 V		10	40	μA
		V_{DD} = 3.0 V		VR output = 2.0 V		10	40	μA
LCD operating current	I_{LCD1} Notes 4, 5	External resistance division method	f_{LCD} = f_{SUB}, LCD panel not connected, LCD clock = 512 Hz	V_{DD} = 5.0 V		0.28	1.2	μA
				V_{DD} = 3.0 V		0.2	1.2	μA
	I_{LCD2} Note4	Internal voltage boosting method	f_{LCD} = f_{SUB}, LCD panel not connected, LCD clock = 512 Hz	1/3 bias V_{LCD} = 01H		1.39	4.7	μA
				1/3 bias V_{LCD} = 0FH		0.94	3.1	μA
				1/4 bias V_{LCD} = 0AH		1.53	5.0	μA
	I_{LCD3} Note4	Capacitor split method	f_{LCD} = f_{SUB}, LCD panel not connected, LCD clock = 512 Hz	V_{DD} = 5.0 V		0.56	2.0	μA
				V_{DD} = 3.0 V		0.36	1.7	μA

Notes 1. Current flowing only to the operational amplifier (AV_{DD0} pin). The current value of the 78K0R/Lx3 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{AMP} when the operational amplifier operates in an operation mode, HALT mode or STOP mode.

2. Current flowing only to the voltage reference (AV_{DD0} pin). The current value of the 78K0R/Lx3 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{VR1} when the voltage reference circuit operates in an operation mode, HALT mode or STOP mode.

3. Current flowing only to the voltage reference or input gate voltage boost circuit for the A/D converter (V_{DD} pin). The current value of the 78K0R/Lx3 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{VR2} when the voltage reference or boost circuit operates in an operation mode, HALT mode or STOP mode.

4. Current flowing only to the LCD controller/driver (V_{DD} pin). The current value of the 78K0R/Lx3 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1}, or I_{DD2}) when the LCD controller/driver operates in an operation mode or HALT mode.

5. Not including the current that flows through the LCD divider resistor.

<R> **6.** Dedicated to μPD78F150xA

(21/39)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 13	Soft	Voltage reference	ADVRC: A/D reference voltage control register	During voltage reference operation, be sure to connect a tantalum capacitor (capacitance: 10 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) and a ceramic capacitor (capacitance: 0.1 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) to the VREFOUT/AVREFP pin for stabilizing the reference voltage. Furthermore, do not apply a voltage from the VREFOUT/AVREFP pin during voltage reference operation.	p.436 ☐
				To use voltage reference output (VREFOUT) to the positive reference voltage of the A/D converter (ADREFP) and the positive reference voltage of the the D/A converter (DAREFP), be sure to set VRON to 1 after setting VRSEL to 1.	p.436 ☐
				Rewriting DACSWn (n = 0, 1) during A/D conversion is prohibited when both the positive reference voltage of the A/D converter (ADREFP) and the positive reference voltage fo the D/A converter (DAREFP) are the voltage reference output (VREFOUT) (VRSEL = 1 and DAREF = 1). Rewrite it when conversion operation is stopped (ADCS = 0).	p.437 ☐
				Do not change the output voltage of the reference voltage by using VRGV during the voltage reference operation (VRON = 1).	p.437 ☐
	Hard		VREFOUT pin	The VREFOUT output voltage can be used only as the positive reference voltage of the internal A/D and D/A converters of the microcontroller. Do not connect an external circuit other than a tantalum capacitor (capacitance: 10 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) and a ceramic capacitor (capacitance: 0.1 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) to the VREFOUT pin for stabilizing the reference voltage.	p.437 ☐
Chapter 14	Soft	Configuration of serial array unit	SDRmn: Lower 8 bits of the serial data register mn	Be sure to clear bit 8 to "0".	p.445 ☐
			PER0: Peripheral enable register 0	When setting serial array unit m, be sure to set SAUmEN to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for input switch control register (ISC), noise filter enable register (NFEN0), port input mode register (PIM1, PIM7), port output mode register (POM1, POM7, POM8), port mode registers (PM1, PM5, PM7, PM8), and port registers (P1, P5, P7, P8)).	p.447 ☐
				After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	p.447 ☐
			SPSm: Serial clock select register m	Be sure to clear bits 15 to 8 to "0".	p.448 ☐
				After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	p.448 ☐
			SMRmn: Serial mode register mn	Be sure to clear bits 13 to 9, 7, 4, and 3 to "0". Be sure to set bit 5 to "1".	p.449 ☐
			SCRmn: Serial communication operation setting register mn	Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".	pp.451 to 453 ☐
			SDRmn: Serial data register mn	Be sure to clear bit 8 to "0".	p.454 ☐
				Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.	p.454 ☐
				Setting SDRmn[15:9] = 0000000B is prohibited when the simplified I^2C is used. Set SDRmn[15:9] to 0000001B or greater.	p.454 ☐