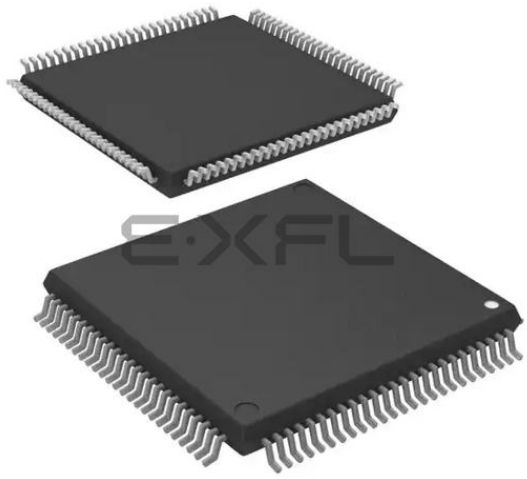
Renesas Electronics America Inc - UPD78F1503AGC-UEU-AX Datasheet



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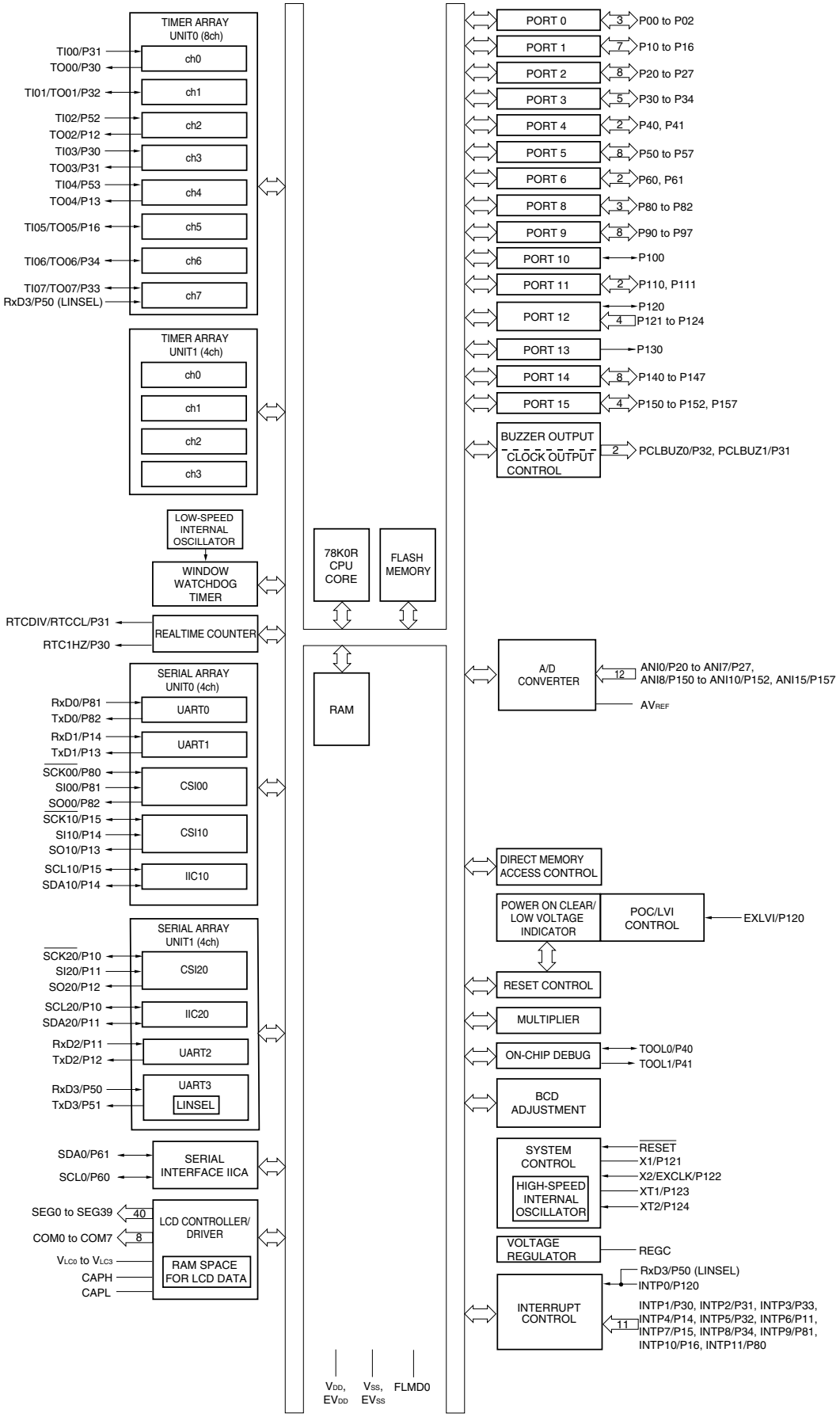
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1503agc-ueu-ax

<R> (2) μPD78F1513A, 78F1515A



(h) INTP9, INTP11

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

Caution To use P80/$\overline{\text{SCK00}}$/INTP11, P81/RxD0/SI00/INTP9, and P82/SO00/TxD0, as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 14-5 Relationship Between Register Settings and Pins (Channel 0 of unit 0: CSI00, UART0 Reception).

2.2.10 P90 to P97

P90 to P97 function as an I/O port. This port can also be used for segment output of LCD controller/driver.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P90/SEGxx	√ (xx = 22)	√ (xx = 31)	√ (xx = 45)
P91/SEGxx	√ (xx = 21)	√ (xx = 30)	√ (xx = 44)
P92/SEGxx	√ (xx = 20)	√ (xx = 29)	√ (xx = 43)
P93/SEGxx	–	√ (xx = 28)	√ (xx = 42)
P94/SEGxx	–	√ (xx = 27)	√ (xx = 41)
P95/SEGxx	–	√ (xx = 26)	√ (xx = 40)
P96/SEGxx	–	√ (xx = 25)	√ (xx = 39)
P97/SEGxx	–	√ (xx = 24)	√ (xx = 38)

The following operation modes can be specified in 1-bit units.

(1) Port mode

P90 to P97 function as an I/O port. P90 to P97 can be set to input or output port in 1-bit units using port mode register 9 (PM9). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 9 (PU9).

(2) Control mode

P90 to P97 function as segment output of LCD controller/driver (SEGxx).

Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3-1. Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number	Address Value	Block Number	Address Value	Block Number	Address Value	Block Number
00000H to 003FFH	00H	08000H to 083FFH	20H	10000H to 103FFH	40H	18000H to 183FFH	60H
00400H to 007FFH	01H	08400H to 087FFH	21H	10400H to 107FFH	41H	18400H to 187FFH	61H
00800H to 00BFFH	02H	08800H to 08BFFH	22H	10800H to 10BFFH	42H	18800H to 18BFFH	62H
00C00H to 00FFFH	03H	08C00H to 08FFFH	23H	10C00H to 10FFFH	43H	18C00H to 18FFFH	63H
01000H to 013FFH	04H	09000H to 093FFH	24H	11000H to 113FFH	44H	19000H to 193FFH	64H
01400H to 017FFH	05H	09400H to 097FFH	25H	11400H to 117FFH	45H	19400H to 197FFH	65H
01800H to 01BFFH	06H	09800H to 09BFFH	26H	11800H to 11BFFH	46H	19800H to 19BFFH	66H
01C00H to 01FFFH	07H	09C00H to 09FFFH	27H	11C00H to 11FFFH	47H	19C00H to 19FFFH	67H
02000H to 023FFH	08H	0A000H to 0A3FFH	28H	12000H to 123FFH	48H	1A000H to 1A3FFH	68H
02400H to 027FFH	09H	0A400H to 0A7FFH	29H	12400H to 127FFH	49H	1A400H to 1A7FFH	69H
02800H to 02BFFH	0AH	0A800H to 0ABFFH	2AH	12800H to 12BFFH	4AH	1A800H to 1ABFFH	6AH
02C00H to 02FFFH	0BH	0AC00H to 0AFFFH	2BH	12C00H to 12FFFH	4BH	1AC00H to 1AFFFH	6BH
03000H to 033FFH	0CH	0B000H to 0B3FFH	2CH	13000H to 133FFH	4CH	1B000H to 1B3FFH	6CH
03400H to 037FFH	0DH	0B400H to 0B7FFH	2DH	13400H to 137FFH	4DH	1B400H to 1B7FFH	6DH
03800H to 03BFFH	0EH	0B800H to 0BBFFH	2EH	13800H to 13BFFH	4EH	1B800H to 1BBFFH	6EH
03C00H to 03FFFH	0FH	0BC00H to 0BFFFH	2FH	13C00H to 13FFFH	4FH	1BC00H to 1BFFFH	6FH
04000H to 043FFH	10H	0C000H to 0C3FFH	30H	14000H to 143FFH	50H	1C000H to 1C3FFH	70H
04400H to 047FFH	11H	0C400H to 0C7FFH	31H	14400H to 147FFH	51H	1C400H to 1C7FFH	71H
04800H to 04BFFH	12H	0C800H to 0CBFFH	32H	14800H to 14BFFH	52H	1C800H to 1CBFFH	72H
04C00H to 04FFFH	13H	0CC00H to 0CFFFH	33H	14C00H to 14FFFH	53H	1CC00H to 1CFFFH	73H
05000H to 053FFH	14H	0D000H to 0D3FFH	34H	15000H to 153FFH	54H	1D000H to 1D3FFH	74H
05400H to 057FFH	15H	0D400H to 0D7FFH	35H	15400H to 157FFH	55H	1D400H to 1D7FFH	75H
05800H to 05BFFH	16H	0D800H to 0DBFFH	36H	15800H to 15BFFH	56H	1D800H to 1DBFFH	76H
05C00H to 05FFFH	17H	0DC00H to 0DFFFH	37H	15C00H to 15FFFH	57H	1DC00H to 1DFFFH	77H
06000H to 063FFH	18H	0E000H to 0E3FFH	38H	16000H to 163FFH	58H	1E000H to 1E3FFH	78H
06400H to 067FFH	19H	0E400H to 0E7FFH	39H	16400H to 167FFH	59H	1E400H to 1E7FFH	79H
06800H to 06BFFH	1AH	0E800H to 0EBFFH	3AH	16800H to 16BFFH	5AH	1E800H to 1EBFFH	7AH
06C00H to 06FFFH	1BH	0EC00H to 0EFFFH	3BH	16C00H to 16FFFH	5BH	1EC00H to 1EFFFH	7BH
07000H to 073FFH	1CH	0F000H to 0F3FFH	3CH	17000H to 173FFH	5CH	1F000H to 1F3FFH	7CH
07400H to 077FFH	1DH	0F400H to 0F7FFH	3DH	17400H to 177FFH	5DH	1F400H to 1F7FFH	7DH
07800H to 07BFFH	1EH	0F800H to 0FBFFH	3EH	17800H to 17BFFH	5EH	1F800H to 1FBFFH	7EH
07C00H to 07FFFH	1FH	0FC00H to 0FFFFH	3FH	17C00H to 17FFFH	5FH	1FC00H to 1FFFFH	7FH

<R> **Remark** μPD78F1500A, 78F1503A, 78F1506A, 78F1510A, 78F1513A, 78F1516A: Block numbers 00H to 3FH

μPD78F1501A, 78F1504A, 78F1507A: Block numbers 00H to 5FH

<R> μPD78F1502A, 78F1505A, 78F1508A, 78F1512A, 78F1515A, 78F1518A: Block numbers 00H to 7FH

3.1.1 Internal program memory space

The internal program memory space stores the program and table data. Normally, it is addressed with the program counter (PC).

78K0R/Lx3 microcontrollers products incorporate internal ROM (flash memory), as shown below.

Table 3-2. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
<R> μPD78F1500A, 78F1503A, 78F1506A, 78F1510A, 78F1513A, 78F1516A	Flash memory	65536 × 8 bits (00000H to 0FFFFH)
μPD78F1501A, 78F1504A, 78F1507A		98303 × 8 bits (00000H to 17FFFH)
<R> μPD78F1502A, 78F1505A, 78F1508A, 78F1512A, 78F1515A, 78F1518A		131071 × 8 bits (00000H to 1FFFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 128-byte area 00000H to 0007FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area. Furthermore, the interrupt jump address is a 64 K address of 00000H to 0FFFFH, because the vector code is assumed to be 2 bytes.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

4.2.10 Port 9

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P90/SEGxx	√ (xx = 22)	√ (xx = 31)	√ (xx = 45)
P91/SEGxx	√ (xx = 21)	√ (xx = 30)	√ (xx = 44)
P92/SEGxx	√ (xx = 20)	√ (xx = 29)	√ (xx = 43)
P93/SEGxx	–	√ (xx = 28)	√ (xx = 42)
P94/SEGxx	–	√ (xx = 27)	√ (xx = 41)
P95/SEGxx	–	√ (xx = 26)	√ (xx = 40)
P96/SEGxx	–	√ (xx = 25)	√ (xx = 39)
P97/SEGxx	–	√ (xx = 24)	√ (xx = 38)

Port 9 is an I/O port with an output latch. Port 9 can be set to the input mode or output mode in 1-bit units using port mode register 9 (PM9). When the P90 to P97 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 9 (PU9).

This port can also be used for segment output.

Reset signal generation sets port 9 to input mode.

Figures 4-25 and 4-26 show block diagrams of port 9.

Figure 4-46. Format of Pull-up Resistor Option Register (78K0R/LH3)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	0	PU02	PU01	PU00	F0030H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	PU34	PU33	PU32	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	0	0	0	PU41	PU40	F0034H	00H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU8	PU87	PU86	PU85	PU84	PU83	PU82	PU81	PU80	F0038H	00H	R/W
PU9	PU97	PU96	PU95	PU94	PU93	PU92	PU91	PU90	F0039H	00H	R/W
PU10	0	0	0	0	0	PU102	PU101	PU100	F003AH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W
PU14	PU147	PU146	PU145	PU144	PU143	PU142	PU141	PU140	F003EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 5, 7 to 10, 12, 14 ; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

(5) Port output mode registers (POMx)

These registers set the output mode of P10 to P15, P75, P77, P80, or P82 in 1-bit units.

N-ch open drain output (V_{DD} tolerance) mode can be selected during serial communication with an external device of the different potential, and for the SDA10, SDA20 pin during simplified I^2C communication with an external device of the same potential.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4-48. Format of Port Output Mode Register

- 78K0R/LF3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W

- 78K0R/LG3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM8	0	0	0	0	0	POM82	0	POM80	F0058H	00H	R/W

- 78K0R/LH3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM7	POM77	0	POM75	0	0	0	0	0	F0057H	00H	R/W
POM8	0	0	0	0	0	POM82	0	POM80	F0058H	00H	R/W

POMmn	Pmn pin output mode selection (m = 1, 7, and 8; n = 0 to 5 and 7)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

Figure 6-17. Format of Timer Input Select Registers 0, 1 (TIS0, TIS1) (2/2)

• 78K0R/LG3

Address: FFF3EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	TIS07	TIS06	TIS05	TIS04	TIS03	TIS02	TIS01	TIS00

Address: FFF4EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS1	0	0	RTCIS04	RTCIS00	0	0	0	0

• 78K0R/LH3

Address: FFF3EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	TIS07	TIS06	TIS05	TIS04	TIS03	TIS02	TIS01	TIS00

Address: FFF4EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS1	0	0	RTCIS04	RTCIS00	TIS13	TIS12	TIS11	TIS10

• Channels 1 to 3 and 5 to 7 of timer array unit 0 and channels 0 to 3 of timer array unit 1

TISpq	SDIV	Selection of Timer input used with channel (pq = 01, 02, 03, 05, 06, 07, 10, 11, 12, 13)
0	×	Input signal of timer input pin (TIpq)
1	0	$f_{SUB}/2$
	1	$f_{SUB}/4$

• Channels 0 and 4 of timer array unit 0

TISpq	RTCISpq	SDIV	Selection of Timer input used with channel (pq = 00, 04)
0	×	×	Input signal of timer input pin (TIpq)
1	0	0	$f_{SUB}/2$
		1	$f_{SUB}/4$
	1	0	RTC Interval interrupt (INTRTCI)
		1	Setting prohibited

Caution When the LIN-bus communication function is used, select the input signal of the RxD3 pin by setting ISC1 to 1 and TIS07 = 0.

Remarks 1. pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: pq = 00 to 04, 07
78K0R/LG3: pq = 00 to 07
78K0R/LH3: pq = 00 to 07, 10 to 13

2. ×: don't care

3. f_{SUB}: Subsystem select clock

4. SDIV: Bit 3 of the system clock control register (CKC)

6.7.2 Operation as external event counter

The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TIpq pin. When a specified count value is reached, the event counter generates an interrupt. The specified number of counts can be calculated by the following expression.

Specified number of counts = Set value of TDRpq + 1

TCRpq operates as a down counter in the event counter mode.

When the channel start trigger bit (TSpq) is set to 1, TCRpq loads the value of TDRpq.

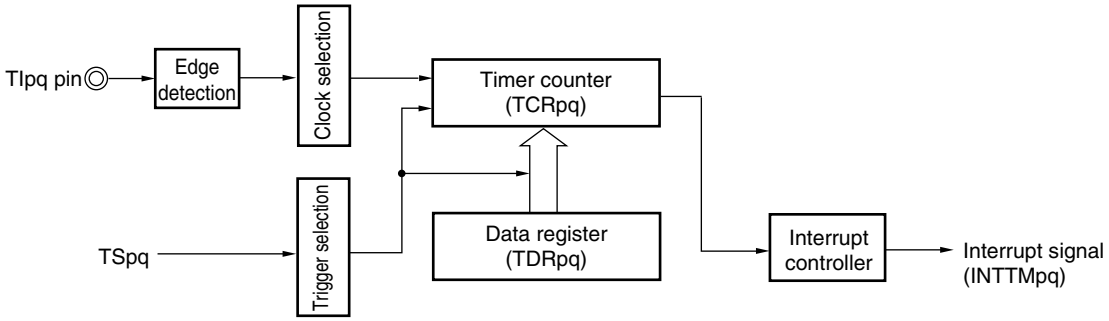
TCRpq counts down each time the valid input edge of the TIpq pin has been detected. When TCRpq = 0000H, TCRpq loads the value of TDRpq again, and outputs INTTMpq.

After that, the above operation is repeated.

TOpq must not be used because its waveform depends on the external event and irregular.

TDRpq can be rewritten at any time. The new value of TDRpq becomes valid during the next count period.

Figure 6-41. Block Diagram of Operation as External Event Counter



Remark pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: pq = 00 to 04, 07
78K0R/LG3: pq = 00 to 07
78K0R/LH3: pq = 00 to 07, 10 to 13

Figure 6-56. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN or TAU1EN bits of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSp register. Determines clock frequencies of CKp0 and CKp1.	
Channel default setting	Sets the TMRpq register (determines operation mode of channel). Clears TOEpq to 0 and stops operation of TOpq.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSpq bit to 1. → The TSpq bit automatically returns to 0 because it is a trigger bit.	TEpq = 1, and the TIpq pin start edge detection wait status is set.
	Detects TIpq pin input count start valid edge. →	Clears TCRpq to 0000H and starts counting up.
During operation	Set value of the TDRpq register can be changed. The TCRpq register can always be read. The TSRpq register is not used. Set values of TMRpq, TOMp, TOLp, TOp, and TOEp registers cannot be changed.	When the TIpq pin start edge is detected, the counter (TCRpq) counts up from 0000H. If a capture edge of the TIpq pin is detected, the count value is transferred to TDRpq and INTTMpq is generated. If an overflow occurs at this time, the OVFpq bit of the TSRpq register is set; if an overflow does not occur, the OVFpq bit is cleared. TCRpq stops the count operation until the next TIpq pin start edge is detected.
Operation stop	The TTpq bit is set to 1. → TTpq bit automatically returns to 0 because it is a trigger bit.	TEpq = 0, and count operation stops. TCRpq holds count value and stops. The OVFpq bit of the TSRpq register is also held.
TAU stop	The TAU0EN or TAU1EN bits of PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: p = 0, pq = 00 to 04, 07
78K0R/LG3: p = 0, pq = 00 to 07
78K0R/LH3: p = 0, 1, pq = 00 to 07, 10 to 13

(8) Serial channel enable status register m (SEm)

SEm indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register 0 (SSm), the corresponding bit of this register is set to 1.

When 1 is written a bit of serial channel stop register 0 (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of CKOmn of the serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of CKOmn of the SOm register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

SEm can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of SEm can be set with an 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears this register to 0000H.

Figure 14-11. Format of Serial Channel Enable Status Register m (SEm)

Address: F0120H, F0121H (SE0), F0160H, F0161H (SE1) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEm	0	0	0	0	0	0	0	0	0	0	0	0	SEm3	SEm2	SEm1	SEm0

SEmn	Indication of operation enable/stop status of channel n
0	Operation stops (stops with the values of the control register and shift register, and the statuses of the serial clock I/O pin, serial data output pin, and the FEF, PEF, and OVF error flags retained[Note]).
1	Operation is enabled.

Note Bits 6 and 5 (TSFmn, BFFmn) of the SSRmn register are cleared.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Figure 14-57. Procedure for Resuming Slave Reception

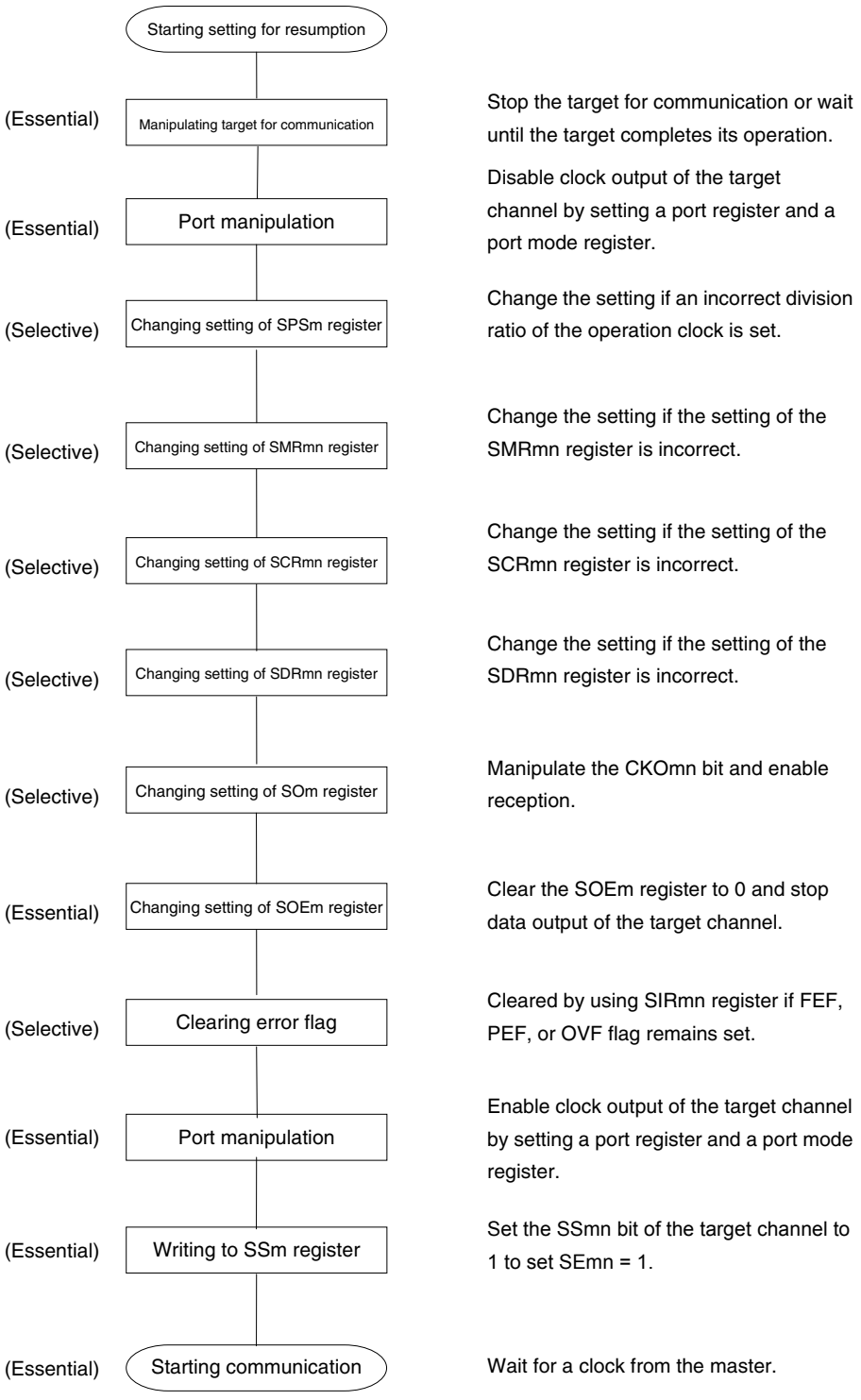
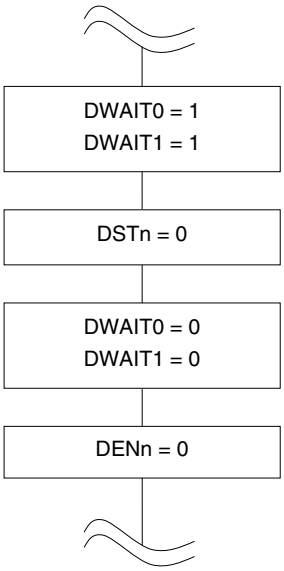


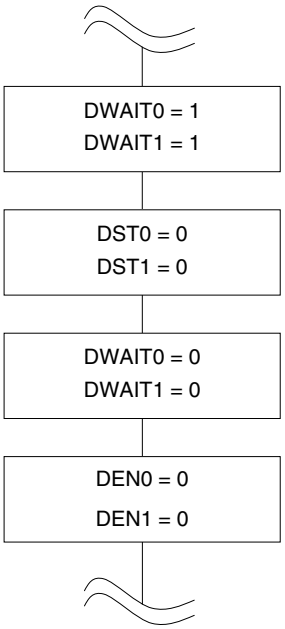
Figure 18-13. Forced Termination of DMA Transfer (2/2)

Example 3

- Procedure for forcibly terminating the DMA transfer for one channel if both channels are used



- Procedure for forcibly terminating the DMA transfer for both channels if both channels are used



Caution In example 3, the system is not required to wait two clock cycles after the DWAITn bit is set to 1. In addition, the system does not have to wait two clock cycles after clearing the DSTn bit to 0, because more than two clock cycles elapse from when the DSTn bit is cleared to 0 to when the DENn bit is cleared to 0.

Remarks 1. n: DMA channel number (n = 0, 1)

2. 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

CHAPTER 19 INTERRUPT FUNCTIONS

<R>

		78K0R/LF3	78K0R/FG3	78K0R/LH3
		80 pins	100 pins	128 pins
Maskable interrupts	External	30	33	33
	internal	8	12	13

19.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. For the priority order, see **Table 19-1**.

A standby release signal is generated and STOP and HALT modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

Table 22-2. Hardware Statuses After Reset Acknowledgment (1/4)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		06H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Port registers (P0 to P15) (output latches)		00H
Port mode registers (PM0 to PM12, PM14, PM15)		FFH
Port input mode registers 1, 7 (PIM1, PIM7)		00H
Port output mode registers 1, 7, 8 (POM1, POM7, POM8)		00H
Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7 to PU10, PU12, PU14)		00H
Clock operation mode control register (CMC)		00H
Clock operation status control register (CSC)		C0H
Processor mode control register (PMC)		00H
System clock control register (CKC)		09H
20 MHz internal high-speed oscillation control register (DSCCTL)		00H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		07H
Noise filter enable registers 0, 1 (NFEN0, NFEN1)		00H
Peripheral enable registers 0 (PER0)		00H
Operation speed mode control register (OSMC)		00H
Input switch control register (ISC)		00H
Timer array units 0, 1 (TAU0, TAU1)	Timer data registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TDR00, TDR01, TDR02, TDR03, TDR04, TDR05, TDR06, TDR07, TDR10, TDR11, TDR12, TDR13)	0000H
	Timer mode registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TMR00, TMR01, TMR02, TMR03, TMR04, TMR05, TMR06, TMR07, TMR10, TMR11, TMR12, TMR13)	0000H
	Timer status registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TSR00, TSR01, TSR02, TSR03, TSR04, TSR05, TSR06, TSR07, TSR10, TSR11, TSR12, TSR13)	0000H
	Timer input select register 0, 1 (TIS0, TIS1)	00H
	Timer channel counter registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TCR00, TCR01, TCR02, TCR03, TCR04, TCR05, TCR06, TCR07, TCR10, TCR11, TCR12, TCR13)	FFFFH
	Timer channel enable status registers 0, 1 (TE0, TE1)	0000H
	Timer channel start trigger registers 0, 1 (TS0, TS1)	0000H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

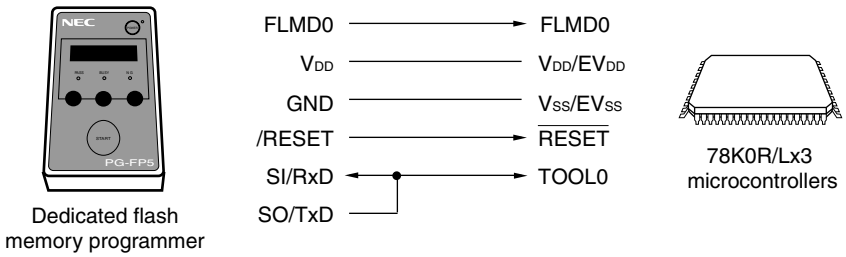
Remark The SFR and 2nd SFR provided differ depending on the product. Refer to **3.2.4 Special function registers (SFRs)** and **3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

27.3 Communication Mode

Communication between the dedicated flash memory programmer and the 78K0R/Lx3 microcontrollers is established by serial communication using the TOOL0 pin via a dedicated single-line UART of the 78K0R/Lx3 microcontrollers.

Transfer rate: 115,200 bps to 1,000,000 bps

Figure 27-2. Communication with Dedicated Flash Memory Programmer



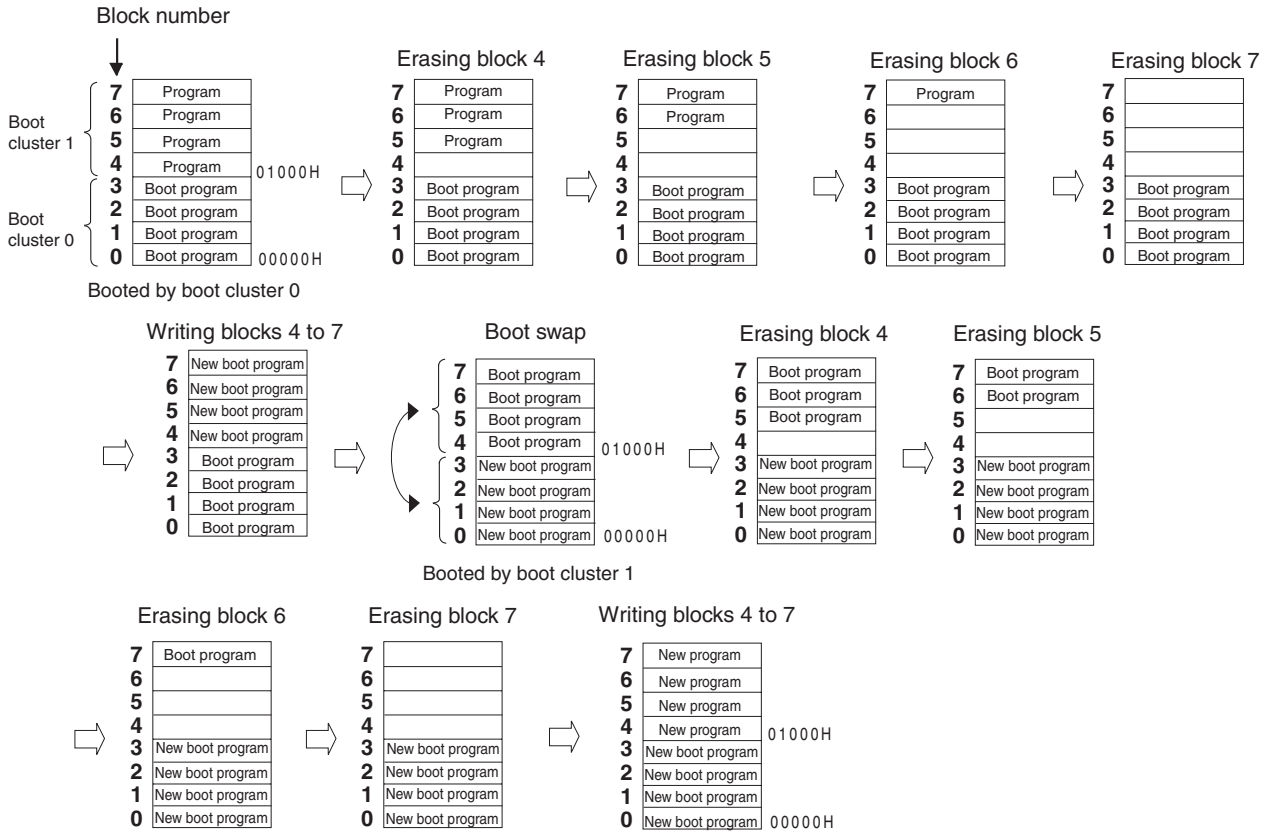
When using the FlashPro5 as the dedicated flash memory programmer, the FlashPro5 generates the following signals for the 78K0R/Lx3 microcontrollers. For details, refer to the user's manual for the FlashPro5.

Table 27-1. Pin Connection

FlashPro5			78K0R/Lx3 microcontrollers	Connection
Signal Name	I/O	Pin Function	Pin Name	
FLMD0	Output	Mode signal	FLMD0	◎
V_{DD}	I/O	V_{DD} voltage generation/power monitoring	V_{DD}, EV_{DD}, AV_{DD0}, AV_{DD1}	◎
GND	–	Ground	V_{SS}, EV_{SS}, AV_{SS}	◎
CLK	Output	Clock output	–	×
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎
SI/RxD	Input	Receive signal	TOOL0	◎
SO/TxD	Output	Transmit signal		
SCK	Output	Transfer clock	–	×

Remark ◎: Be sure to connect the pin.
×: The pin does not have to be connected.

Figure 27-12. Example of Executing Boot Swapping



(26/39)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 16	Soft	LCD controller/driver	LCDM: LCD display mode register	To manipulate VLCON when using the internal voltage boosting method or capacitor split method, follow the procedure below. A. To stop the operation of the voltage boosting/capacitor split circuit after switching display status from on to off: 1) Set to display off status by setting LCDON = 0. 2) Disable outputs of all the segment buffers and common buffers by setting SCOC = 0. 3) Stop the operation of the voltage boosting/capacitor split circuit by setting V LCON = 0. B. To stop the operation of the voltage boosting/capacitor split circuit during display on status: Setting prohibited. Be sure to stop the operation of the voltage boosting/capacitor split circuit after setting display off. C. To set display on from stop status of the voltage boosting/capacitor split circuit: 1) Start the operation of the voltage boosting/capacitor split circuit by setting VLCON = 1, then wait for the voltage boosting/capacitor split wait time (see CHAPTER 31 ELECTRICAL SPECIFICATIONS). 2) Set all the segment buffers and common buffers to non-display output status by setting SCOC = 1. 3) Set display on by setting LCDON = 1.	p.669 ☐
			LCDC0: LCD clock control register 0	Bits 3, 6, and 7 must be set to 0.	p.670 ☐
				Set the LCD clock (LCDCL) to no more than 512 Hz when the internal voltage boost method has been set.	p.670 ☐
			VLCD: LCD boost level control register	The VLCD setting is valid only when the voltage boost circuit is operating.	p.671 ☐
				Bits 5 to 7 must be set to 0.	p.671 ☐
				Be sure to change the VLCD value after having stopped the operation of the voltage boost circuit (VLCON = 0).	p.671 ☐
				These values above may change after device evaluation.	p.671 ☐
				To use the internal voltage boosting method, specify the reference voltage by using the VLCD register (or perform a reset to use the default value of the reference voltage), wait for the reference voltage setup time (2 ms (min.)), and then set VLCON to 1.	p.671 ☐
			PFALL: Port function register	For 78K0R/LF3, bits 3 and 7 must be set to 0. For 78K0R/LG3 and 78K0R/LH3, bit 7 must be set to 0.	p.672 ☐
			SEGEN: Segment enable register	SEGEN can be written only once after reset release.	p.673 ☐
				For 78K0R/LF3, bits 1 to 7 must be set to 0. For 78K0R/LG3, bits 2 to 7 must be set to 0. For 78K0R/LH3, bits 5 to 7 must be set to 0.	p.673 ☐

(31/39)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 21	Hard	Standby function	OSTS: Oscillation stabilization time select register	The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).	p.775 ☐
	Soft		STOP mode	Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.	p.782 ☐
				The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.	pp.782 ☐ , 784
				To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.	p.784 ☐
				To stop the internal low-speed oscillation clock in the STOP mode, use an option byte to stop the watchdog timer operation in the HALT/STOP mode (bit 0 (WDSTBYON) of 000C0H = 0), and then execute the STOP instruction.	p.784 ☐
				To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), temporarily switch the CPU clock to the internal high-speed oscillation clock before the next execution of the STOP instruction. Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).	p.784 ☐
Chapter 22	Hard	Reset function	–	For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin (To perform an external reset upon power application, a low level of at least 10 μs must be continued during the period in which the supply voltage is within the operating range ($V_{DD} \geq 1.8$ V)).	p.788 ☐
				During reset input, the X1 clock, XT1 clock, internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.	p.788 ☐
				When the STOP mode is released by a reset, the RAM contents in the STOP mode are held during reset input.	p.788 ☐
				When reset is effected, port pin P140 is set to low-level output and other port pins become high-impedance, because each SFR and 2nd SFR are initialized.	p.788 ☐
	Soft		Block diagram of reset function	An LVI circuit internal reset does not reset the LVI circuit.	p.790 ☐
			Watchdog timer overflow	A watchdog timer internal reset resets the watchdog timer.	p.790 ☐
			RESF: Reset control flag register	Do not read data by a 1-bit memory manipulation instruction.	p.797 ☐
				Do not make a judgment based on only the read value of the RESF register 8-bit data, because bits other than TRAP, WDRF, and LVIRF become undefined.	p.797 ☐
				When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, LVIRF flag may become 1 from the beginning depending on the power-on waveform.	p.797 ☐

(13/14)

Edition	Description	Chapter
4th Edition	Addition of example of calculation of LCD frame frequency to (c) and (d) of **Figure 16-13. Common Signal Waveforms (2/2)**	**CHAPTER 16 LCD CONTROLLER/ DRIVER**
	Change of **Caution** of **Figure 16-31. Examples of LCD Drive Power Connections (External Resistance Division Method)**	
	Change the capacitance value of external capacitors to 0.47 μF±30% in **16.8.2 Internal voltage boosting method** and **16.8.3 Capacitor split method**	
	Addition of **Note** to **Figure 18-4. Format of DMA Mode Control Register n (DMCn) (1/2)**	**CHAPTER 18 DMA CONTROLLER**
	Change of description of **Figure 18-7. Example of Setting for CSI Consecutive Transmission**	
	Addition of **18.5.2 CSI master reception** and **18.5.3 CSI transmission/reception**	
	Change of **18.5.6 Holding DMA transfer pending by DWAITn** and addition of **Caution**	
	Change of **18.5.7 Forced termination by software**	
	Change of **18.6 Cautions on Using DMA Controller**	
	Change value of maskable interrupts of 78K0R/LF3	**CHAPTER 19 INTERRUPT FUNCTIONS**
	Change of **Figure 26-1. Format of User Option Byte (000C0H/010C0H) (1/2)**	**CHAPTER 26 OPTION BYTE**
	Change of **26.4 Setting of Option Byte**	
	Addition of **Figure 27-3. Example of Wiring Adapter for Flash Memory Writing (μPD78F1508A)**	**CHAPTER 27 FLASH MEMORY**
	Addition of **27.9 Creating ROM Code to Place Order for Previously Written Product**	
	Change of Examples 2 in **29.3 BCD Correction Circuit Operation**	**CHAPTER 29 BCD CORRECTION CIRCUIT**
	Change of **Table 30-5. Operation List**	**CHAPTER 30 INSTRUCTION SET**
	Deletion of (TARGET)	**CHAPTER 31 ELECTRICAL SPECIFICATIONS**
	Change of analog output voltage, output current, high, and output current, low in **Absolute Maximum Ratings (T_A = 25°C)**	
	Change of **Internal Oscillator Characteristics**	
	Addition of **Recommended oscillator circuit constants**	
	Change of output voltage, low (V_{OL2}), supply current, and operating current of **DC Characteristics**	
	Change of **Caution** of **(1) Basic operation (3/6)** in **AC Characteristics**	
	Change of **(b) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)** of **(2) Serial interface: Serial array unit (2/18)** and addition of **Note 1**	
	Change of **(c) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)** of **(2) Serial interface: Serial array unit (3/18)**	
	Change of **(d) During communication at same potential (simplified I^2C mode)** of **(2) Serial interface: Serial array unit (5/18)**	
	Change of **(f) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)** of **(2) Serial interface: Serial array unit (11/18)** and addition of **Note 1**	