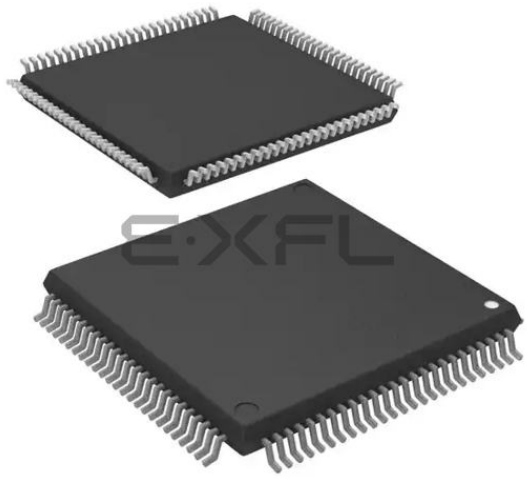
Renesas Electronics America Inc - UPD78F1505AGC(R)-UEU-AX Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1505agc-r-ueu-ax

(2) Non-port functions (5/5) : 78K0R/LH3

Function Name	I/O	Function	After Reset	Alternate Function
TO10	Output	16-bit timer 10 output	Input port	P84/TI10
TO11		16-bit timer 11 output		P85/TI11
TO12		16-bit timer 12 output		P86/TI12
TO13		16-bit timer 13 output		P87/TI13
TxD0	Output	Serial data output from UART0	Input port	P82/SO00
TxD1		Serial data output from UART1		P13/SO10/TO04
TxD2		Serial data output from UART2		P12/SO20/TO02
TxD3		Serial data output from UART3		P51/SEG52
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
V_{DD}	–	Positive power supply (Pins other than port and $\overline{RESET}$, FLMD0 pins)	–	–
EV_{DD}	–	Positive power supply for $\overline{RESET}$, FLMD0 pins, and port pins other than P20 to P27, P110, P111, P150 to P152, P157	–	–
<R> AV_{DD}, Note 1 AV_{DD} Note 2	–	Positive power supply for P20 to P27, P150 to P152, P157	–	–
AV_{DD1} Note 1 EV_{DD1} Note 2	–	Positive power supply for P110, P111	–	–
V_{SS}	–	Ground potential (Pins other than port and $\overline{RESET}$, FLMD0 pins)	–	–
EV_{SS}	–	Ground potential for $\overline{RESET}$, FLMD0 pins, and port pins other than P20 to P27, P110, P111, P150 to P152, P157	–	–
AV_{SS}	–	Ground potential for P20 to P27, P110, P111, P150 to P152, P157	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

<R> **Notes 1.** AV_{DD0} and AV_{DD1} apply to μPD78F150xA only.

2. AV_{DD} and EV_{DD1} apply to μPD78F151xA only.

Cautions 1. To use P30/TO00/TI03/RTC1HZ/INTP1 as a general-purpose port, set bit 5 (RCLOE1) of real-time counter control register 0 (RTCC0), bit 0 (TO00) of timer output register 0 (TO0) and bit 0 (TOE00) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

2. To use P31/TO03/TI00/RTCDIV/RTCCL/PCLBUZ1/INTP2 as a general-purpose port, set bit 4 (RCLOE0) of real-time counter control register 0 (RTCC0), bit 6 (RCLOE2) of real-time counter control register 2 (RTCC2), bit 3 (TO03) of timer output register 0 (TO0), bit 3 (TOE03) of timer output enable register 0 (TOE0) and bit 7 of clock output select register 1 (CKS1) to "0", which is the same as their default status setting.

3. To use P32/TO01/TI01/INTP5/PCLBUZ0 as a general-purpose port, set bit 1 (TO01) of timer output register 0 (TO0), bit 1 (TOE01) of timer output enable register 0 (TOE0) and bit 7 of clock output select register 0 (CKS0) to "0", which is the same as their default status setting.

4. To use P33/TO07/TI07/INTP3 and P34/TO06/TI06/INTP8 as a general-purpose port, set bit 7, 6 (TO07, TO06) of timer output register 0 (TO0), and bit 7, 6 (TOE07, TOE06) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

2.2.5 P40, P41

P40 and P41 function as an I/O port. These pins also function as data I/O for a flash memory programmer/debugger and clock output for a debugger.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P40/TOOL0	√		
P41/TOOL1	√		

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 and P41 function as an I/O port. P40 and P41 can be set to input or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

Be sure to connect an external pull-up resistor to P40 when on-chip debugging is enabled (by using an option byte).

(2) Control mode

P40 and P41 function as data I/O for a flash memory programmer/debugger and clock output for a debugger.

(a) TOOL0

This is a data I/O pin for a flash memory programmer/debugger.

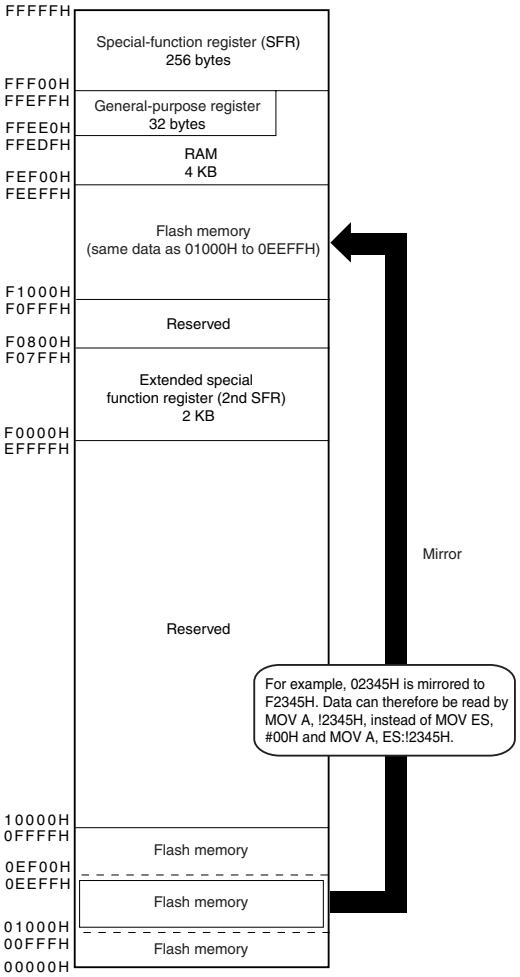
Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

The following show examples.

<R>

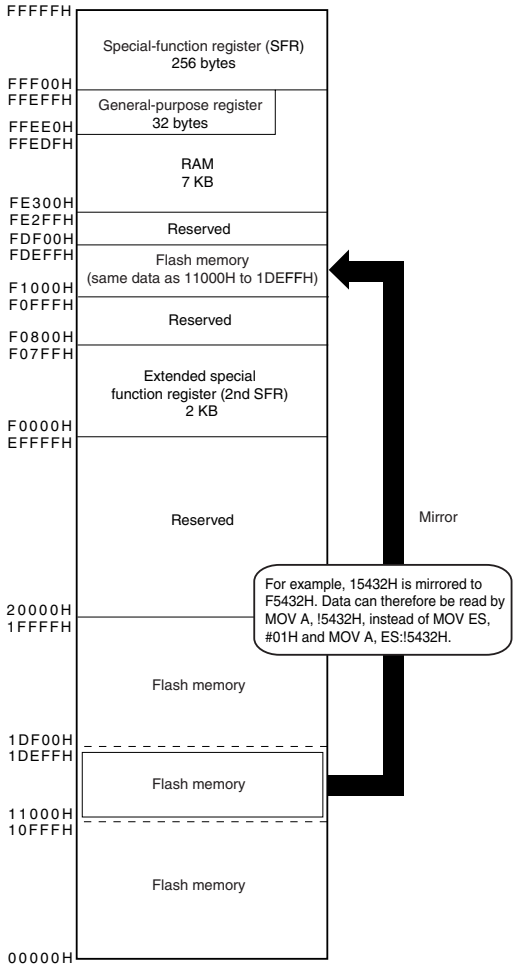
Example 1 μPD78F1500A, 78F1503A, 78F1506A, 78F1510A, 78F1513A, 78F1516A (Flash memory: 64 KB, RAM: 4 KB)

Setting MAA = 0



Example 2 μPD78F1502A, 78F1505A, 78F1508A, 78F1512A, 78F1515A, 78F1518A (Flash memory: 128 KB, RAM: 7 KB)

Setting MAA = 1



Remark MAA: Bit 0 of the processor mode control register (PMC).

4.2.3 Port 2

<R>

	μPD78F150xA			μPD78F151xA		
	78K0R/LF3 (80 pins)	78K0R/LG3 (100 pins)	78K0R/LH3 (128 pins)	78K0R/LF3 (80 pins)	78K0R/LG3 (100 pins)	78K0R/LH3 (128 pins)
P20/ANI0/AMP0-	√			P20/ANI0		
P21/ANI1/AMP0O	√			P20/ANI1		
P22/ANI2/AMP0+	√			P20/ANI2		
P23/ANI3/AMP1-	√			P20/ANI3		
P24/ANI4/AMP1O	√			P20/ANI4		
P25/ANI5/AMP1+	√			P20/ANI5		
P26/ANI6/AMP2-	P26/ANI6	√		P26/ANI6		
P27/ANI7/AMP2O	–	√		–	P27/ANI7	

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for A/D converter analog input, and operational amplifier I/O.

To use P20/ANI0/AMP0- to P27/ANI7/AMP2O as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using PM2. Use these pins starting from the lower bit.

To use P20/ANI0/AMP0- to P27/ANI7/AMP2O as digital output pins, set them in the digital I/O mode by using ADPC and in the output mode by using PM2.

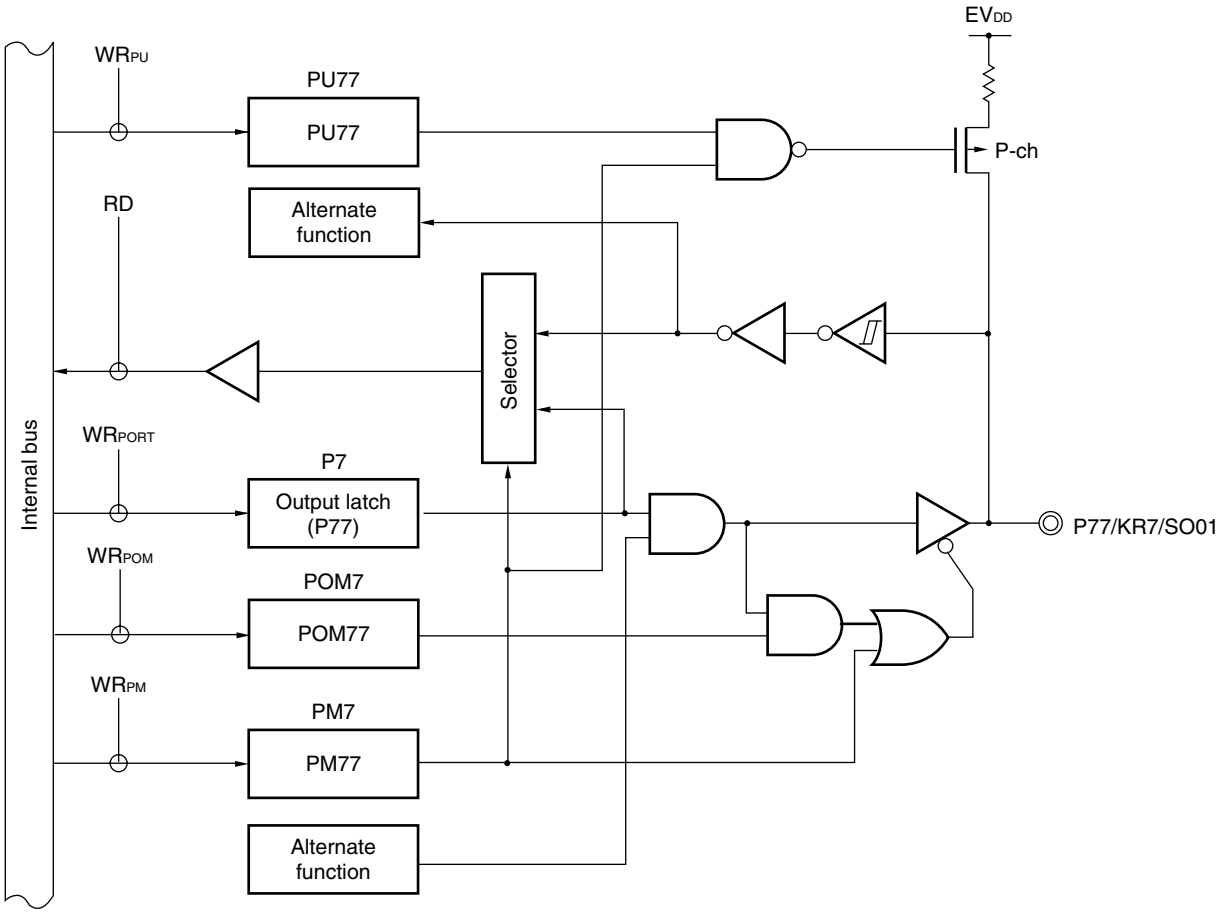
To use P20/ANI0/AMP0- to P27/ANI7/AMP2O as analog input pins, set them in the analog input mode by using the A/D port configuration register (ADPC) and in the input mode by using PM2. Use these pins starting from the upper bit.

All P20/ANI0/AMP0- to P27/ANI7/AMP2O are set in the digital input mode when the reset signal is generated.

Figures 4-7 to 4-9 show block diagrams of port 2.

Caution Make the AV_{DD0} pin the same potential as the EV_{DD} or V_{DD} pin when port 2 is used as a digital port.

Figure 4-19. Block Diagram of P77



P7: Port register 7
PU7: Pull-up resistor option register 7
POM7: Port output mode register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

Figure 4-45. Format of Pull-up Resistor Option Register (78K0R/LG3)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	0	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	PU34	PU33	PU32	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	0	0	0	PU41	PU40	F0034H	00H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU8	0	0	0	0	0	PU82	PU81	PU80	F0038H	00H	R/W
PU9	PU97	PU96	PU95	PU94	PU93	PU92	PU91	PU90	F0039H	00H	R/W
PU10	0	0	0	0	0	0	0	PU100	F003AH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W
PU14	PU147	PU146	PU145	PU144	PU143	PU142	PU141	PU140	F003EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 5, 8 to 10, 12, 14 ; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Table 5-4. CPU Clock Transition and SFR Register Setting Examples (6/6)

(13) • HALT mode (E) set while CPU is operating with internal high-speed oscillation clock (B)
• HALT mode (F) set while CPU is operating with high-speed system clock (C)
• HALT mode (G) set while CPU is operating with subsystem clock (D)
• HALT mode (K) set while CPU is operating with 20 MHz internal high-speed oscillation clock (J)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G) (J) → (K)	Executing HALT instruction

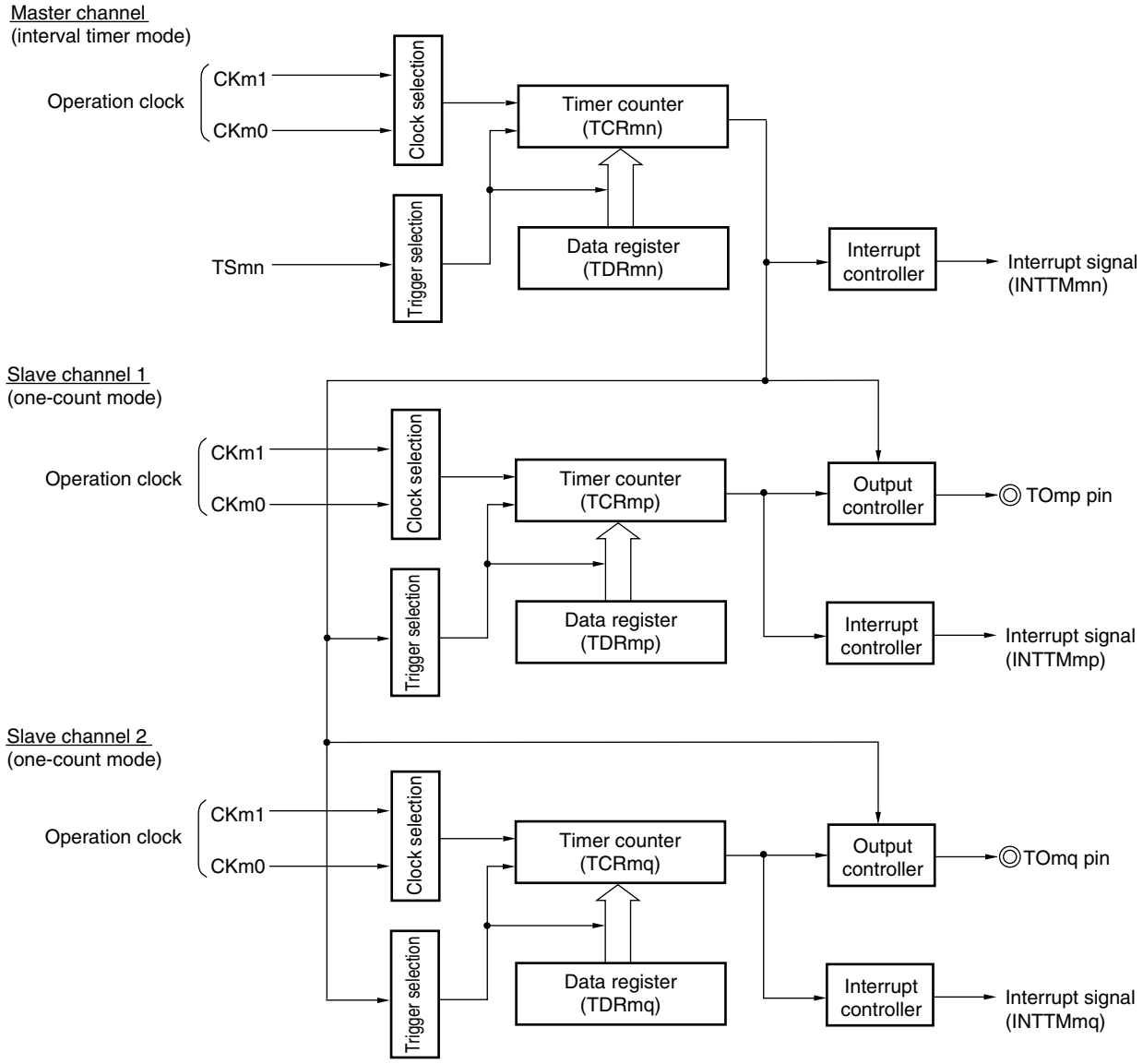
(14) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B)
• STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) ——————————————————————▶

Status Transition		Setting		
(B) → (H)		Stopping peripheral functions that cannot operate in STOP mode	–	Executing STOP instruction
(C) → (I)	In X1 oscillation		Sets the OSTS register	
	External main system clock		–	

Remark (A) to (K) in Table 5-4 correspond to (A) to (K) in Figure 5-15.

Figure 6-67. Block Diagram of Operation as Multiple PWM Output Function (output two types of PWMs)



Remarks 1. 78K0R/LF3:

- m = 0, n = 0, 2, p = n+1, q = n+2, TO00 to TO04, and TO07 pins

2. 78K0R/LG3:

- m = 0, n = 0, 2, 4, p = n+1, q = n+2, TO00 to TO07 pins

3. 78K0R/LH3:

- m = 0, n = 0, 2, 4, p = n+1, q = n+2, TO00 to TO07 pins
- m = 1, n = 0, p = 1, q = 2, TO10 to TO13 pins

(8) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-13. Format of Analog Input Channel Specification Register (ADS)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	ADS3	ADS2	ADS1	ADS0

	ADS3	ADS2	ADS1	ADS0	Analog input channel
	0	0	0	0	ANI0
	0	0	0	1	ANI1
	0	0	1	0	ANI2
	0	0	1	1	ANI3
	0	1	0	0	ANI4
	0	1	0	1	ANI5
	0	1	1	0	ANI6
Note →	0	1	1	1	ANI7
Note →	1	0	0	0	ANI8
Note →	1	0	0	1	ANI9
Note →	1	0	1	0	ANI10
	1	1	1	1	ANI15
	Other than the above				Setting prohibited

Note This setting is prohibited for 78K0R/LF3.

Cautions 1. Be sure to clear bits 4 to 7 to "0".

2 Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 and 15 (PM2, PM15).

3. Do not set the pin that is set by ADPC as digital I/O by ADS.

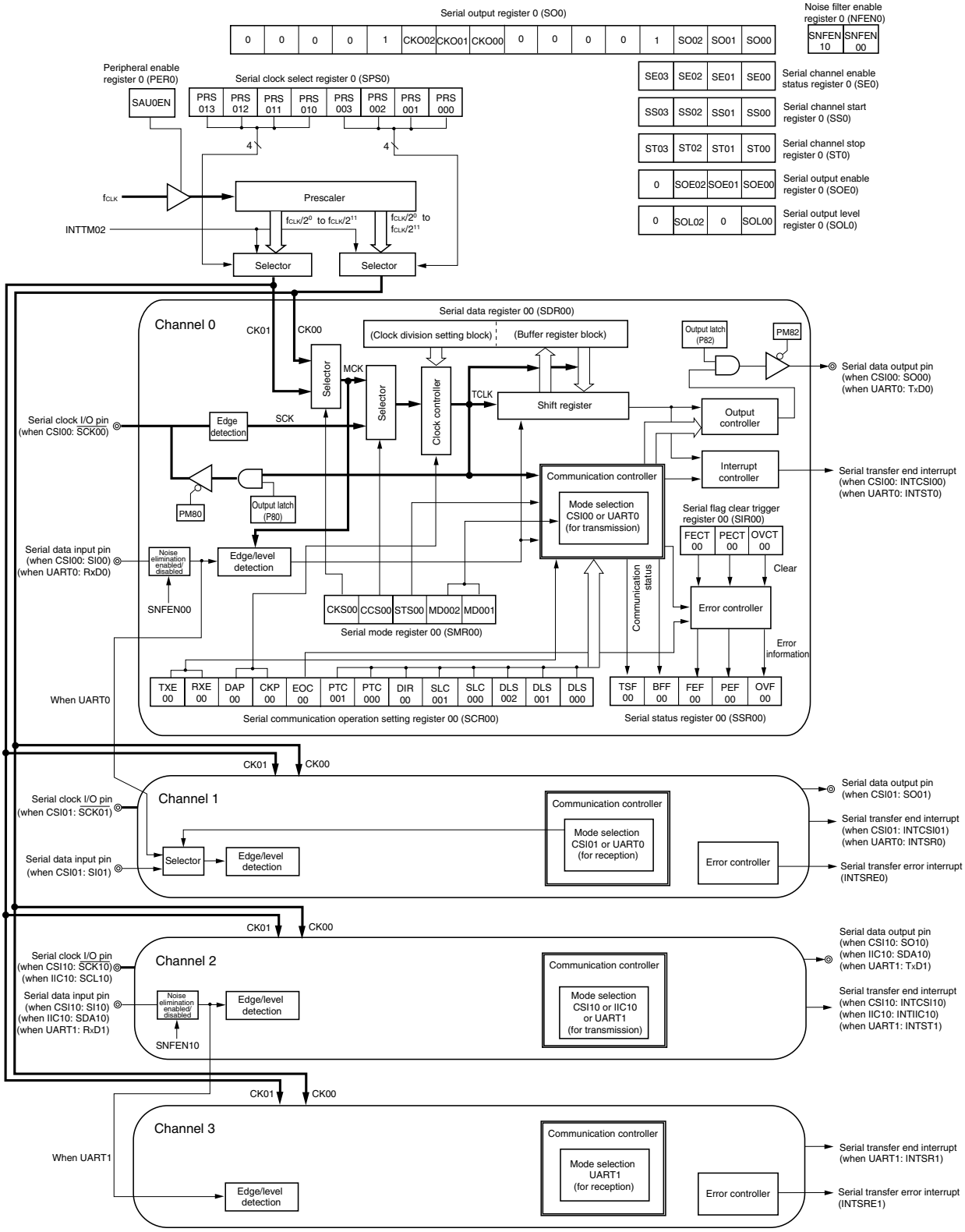
4. When using an operational amplifier n, the output signal of an operational amplifier n can be used as an analog input.

Remark 78K0R/LF3: n = 0, 1

78K0R/LG3, 78K0R/LH3: n = 0 to 2

Figure 14-1 shows the block diagram of serial array unit 0.

Figure 14-1. Block Diagram of Serial Array Unit 0

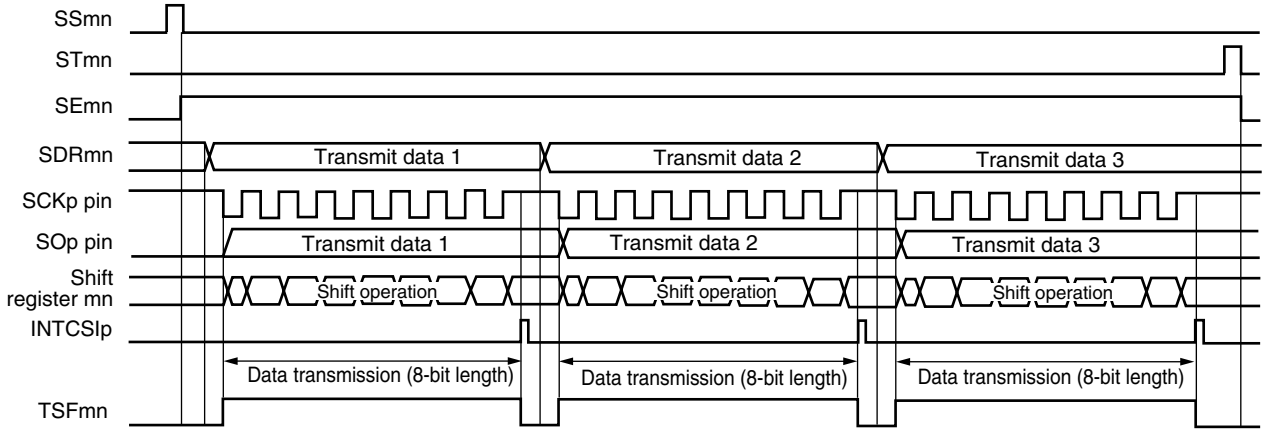


Remarks 1. For 78K0R/LF3, the channels 0 and 1 are not mounted.

2. For 78K0R/LG3, CSI01 is not mounted.

(3) Processing flow (in single-transmission mode)

Figure 14-28. Timing Chart of Master Transmission (in Single-Transmission Mode)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)

CHAPTER 16 LCD CONTROLLER/DRIVER

<R>

Item	78K0R/LF3	78K0R/LG3	78K0R/LH3
	80 pins	100 pins	128 pins
LCD Controller/driver	Segment signal outputs: 31 Common signal outputs: 8	Segment signal outputs: 40 Common signal outputs: 8	Segment signal outputs: 54 Common signal outputs: 8

16.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the 78K0R/Lx3 microcontrollers are as follows.

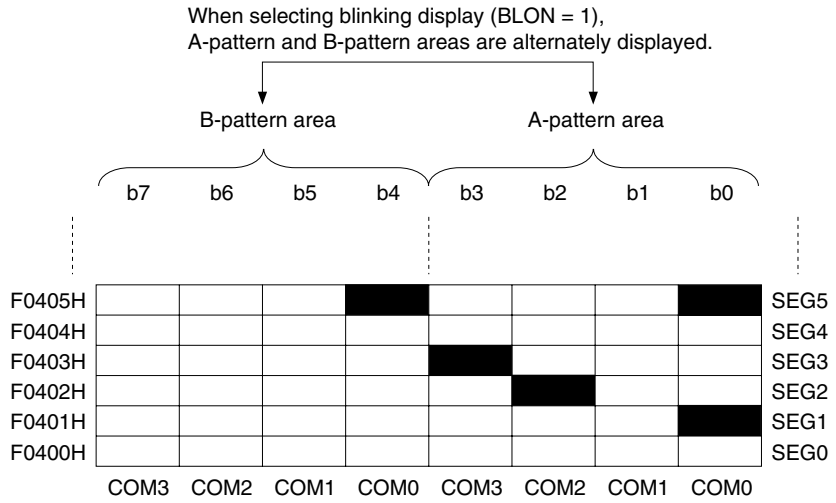
(1) The LCD driver voltage generator can switch internal voltage boosting method, capacitor split method, and external resistance division method.
(2) Automatic output of segment and common signals based on automatic display data memory read
(3) Six different display modes:
- Static
- 1/2 duty (1/2 bias)
- 1/3 duty (1/2 bias)
- 1/3 duty (1/3 bias)
- 1/4 duty (1/3 bias)
- 1/8 duty (1/4 bias)

(4) Six different frame frequencies, selectable in each display mode
(5) The reference voltage to be generated when operating the voltage boost circuit can be selected from 20 stages (contrast adjustment).
(6) The data display of the LCD display data memory can be selected from three types.
- Displaying an A-pattern area (lower four bits)
- Displaying a B-pattern area (higher four bits)
- Alternately displaying A-pattern and B-pattern areas (blinking display corresponding to the constant-period interrupt (INTRTC) timing of the real-time counter (RTC))

(7) 78K0R/LF3: Segment signal outputs: 31Note (SEG0 to SEG30),
Common signal outputs: 8Note (COM0 to COM7)
78K0R/LG3: Segment signal outputs: 40Note (SEG0 to SEG39),
Common signal outputs: 8Note (COM0 to COM7)
78K0R/LH3: Segment signal outputs: 54Note (SEG0 to SEG53),
Common signal outputs: 8Note (COM0 to COM7)

Note The four segment signal outputs (SEG0 to SEG3) and four common signal outputs (COM4 to COM7) are alternate-function pins. COM4 to COM7 can be used only when eight-time-slice mode is selected by the setting of the LCD display mode register (LCDM).

Figure 16-12. Example of Display Data When Blinking Display Has Been Selected



16.5 Setting LCD Controller/Driver

Set the LCD controller/driver using the following procedure.

(1) External resistance division method

<1> Set the external resistance division method via the MDSET0 and MDSET1 bits (bits 4 and 5 of the LCDMD register) (MDSET0 = MDSET1 = 0).

<2> To use segment output only pins, use the SEGEN register to enable segment output to them.
To use segment output pins, which are alternatively used with port pins, use the PFALL register to set them to segment output. In addition, to use the segment output pins, which are alternatively used with the TI04, TI02, and RxD3 pins, use the ISC register to disable input to the Schmitt trigger buffer.

<3> Set the display data in LCD display RAM.

<4> Set the number of time slices and the bias mode via the LCDM0 to LCDM2 bits (bits 0 to 2 of the LCDM register).
- When setting Static, 2-time-slice, 3-time-slice, or 4-time-slice → Go to step <5>
- When setting 8-time-slice → Go to step <6>

<5> Select the display data area via the LCDSEL and BLON bits (bits 3 and 4 of the LCDM register).

<6> Set the LCD source clock and LCD clock via the LCDC0 register.

<7> Set (SCOC = 1) the SCOC bit (bit 6 of the LCDM register).
Non-selected waveforms are output from all the segment and common pins, and the non-display status is entered.

<8> Start output corresponding to each data memory by setting (LCDON = 1) the LCDON bit (bit 7 of the LCDM register).

27.4.2 TOOL0 pin

In the flash memory programming mode, connect this pin directly to the dedicated flash memory programmer or pull it up by connecting it to EV_{DD} via an external resistor.

When on-chip debugging is enabled in the normal operation mode, pull this pin up by connecting it to V_{DD} via an external resistor, and be sure to keep inputting the V_{DD} level to the TOOL0 pin before reset is released (pulling down this pin is prohibited).

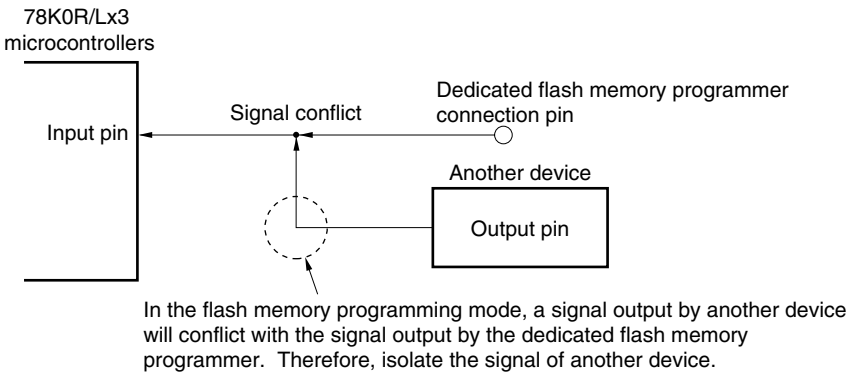
Remark The SAU and IICA pins are not used for communication between the 78K0R/Lx3 microcontrollers and dedicated flash memory programmer, because single-line UART is used.

27.4.3 $\overline{\text{RESET}}$ pin

Signal conflict will occur if the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board. To prevent this conflict, isolate the connection with the reset signal generator.

The flash memory will not be correctly programmed if the reset signal is input from the user system while the flash memory programming mode is set . Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 27-5. Signal Conflict ($\overline{\text{RESET}}$ Pin)



27.4.4 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to V_{DD} or V_{SS} via a resistor.

27.4.5 REGC pin

Connect the REGC pin to GND via a capacitor (0.47 to 1 μF) in the same manner as during normal operation.

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

27.4.6 X1 and X2 pins

Connect X1 and X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the internal high-speed oscillation clock (f_{IH}) is used.

Table 30-5. Operation List (13/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Rotate	ROR	A, 1	2	1	–	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			×
	ROL	A, 1	2	1	–	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			×
	RORC	A, 1	2	1	–	(CY $\leftarrow A_0$, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1			×
	ROLC	A, 1	2	1	–	(CY $\leftarrow A_7$, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1			×
	ROLWC	AX,1	2	1	–	(CY $\leftarrow AX_{15}$, $AX_0 \leftarrow$ CY, $AX_{m+1} \leftarrow AX_m$) × 1			×
		BC,1	2	1	–	(CY $\leftarrow BC_{15}$, $BC_0 \leftarrow$ CY, $BC_{m+1} \leftarrow BC_m$) × 1			×
Bit manipulate	MOV1	CY, saddr.bit	3	1	–	CY ← (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← sfr.bit			×
		CY, A.bit	2	1	–	CY ← A.bit			×
		CY, PSW.bit	3	1	–	CY ← PSW.bit			×
		CY,[HL].bit	2	1	4	CY ← (HL).bit			×
		saddr.bit, CY	3	2	–	(saddr).bit ← CY			
		sfr.bit, CY	3	2	–	sfr.bit ← CY			
		A.bit, CY	2	1	–	A.bit ← CY			
		PSW.bit, CY	3	4	–	PSW.bit ← CY	×	×	
		[HL].bit, CY	2	2	–	(HL).bit ← CY			
		CY, ES:[HL].bit	3	2	5	CY ← (ES, HL).bit			×
		ES:[HL].bit, CY	3	3	–	(ES, HL).bit ← CY			
	AND1	CY, saddr.bit	3	1	–	CY ← CY ∧ (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← CY ∧ sfr.bit			×
		CY, A.bit	2	1	–	CY ← CY ∧ A.bit			×
		CY, PSW.bit	3	1	–	CY ← CY ∧ PSW.bit			×
		CY,[HL].bit	2	1	4	CY ← CY ∧ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∧ (ES, HL).bit			×
	OR1	CY, saddr.bit	3	1	–	CY ← CY ∨ (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← CY ∨ sfr.bit			×
		CY, A.bit	2	1	–	CY ← CY ∨ A.bit			×
		CY, PSW.bit	3	1	–	CY ← CY ∨ PSW.bit			×
		CY, [HL].bit	2	1	4	CY ← CY ∨ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∨ (ES, HL).bit			×

Notes 1. When the internal RAM area or SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area.

(2) Serial interface: Serial array unit (7/18)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AVss = 0 V)

(e) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps
			2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps

Caution Select the TTL input buffer for RxDq and the N-ch open drain output (V_{DD} tolerance) mode for TxDq by using the PIMg and POMx registers.

Remarks 1. q: UART number (q = 0 to 3), g: PIM number (g = 1, 7), x: POM number (x = 1, 7, 8)

2. V_b[V]: Communication line voltage

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of the SMRmn register. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

K

L

M

N

O

(7/39)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 5	Hard	Clock generator	OSTC: Oscillation stabilization time counter status register	The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).	p.213 ☐
	Soft		OSTS: Oscillation stabilization time select register	To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.	p.214 ☐
				Setting the oscillation stabilization time to 20 μs or less is prohibited.	p.214 ☐
				To change the setting of the OSTS register, be sure to confirm that the counting operation of the OSTC register has been completed.	p.214 ☐
				Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.	p.214 ☐
				The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. In the following cases, set the oscillation stabilization time of OSTS to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts. • If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock. • If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after the STOP mode is released.)	p.214 ☐
	Hard			The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).	p.214 ☐
	Soft		CKC: System clock control register	The clock set by CSS, MCM0, SDIV, and MDIV2 to MDIV0 is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time counter, timer array unit (when f_{SUB}/2, f_{SUB}/4, the valid edge of TI0mn input, or the valid edge of INTRTCI is selected as the count clock), clock output/buzzer output, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral operating hardware clock.	p.216 ☐
	Hard			If the peripheral hardware clock is used as the subsystem clock, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 31 ELECTRICAL SPECIFICATIONS.	p.216 ☐
	Soft		DSCCTL: 20 MHz internal high-speed oscillation control register	20 MHz internal oscillation can only be used if $V_{DD} \geq 2.7$ V.	p.218 ☐
				Set SELDSC when 100 μs have elapsed after having set DSCON with $V_{DD} \geq 2.7$ V.	p.218 ☐
				The internal high-speed oscillator must be operated (HIOSTOP = 0) when DSCON = 1.	p.218 ☐
			OSMC: Operation speed mode control register	Write “1” to FSEL before the following two operations. • Changing the clock prior to dividing f_{CLK} to a clock other than f_{IH}. • Operating the DMA controller.	p.221 ☐
				The CPU waits (140.5 clock (f_{CLK})) when “1” is written to the FSEL bit. Interrupt requests issued during a wait will be suspended. However, counting the oscillation stabilization time of f_X can continue even while the CPU is waiting.	p.221 ☐
				To increase f_{CLK} to 10 MHz or higher, set FSEL to “1”, then change f_{CLK} after two or more clocks have elapsed.	p.221 ☐
				Confirm that the clock is operating at 10 MHz or less before setting FSEL = 0.	p.221 ☐

(21/39)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 13	Soft	Voltage reference	ADVRC: A/D reference voltage control register	During voltage reference operation, be sure to connect a tantalum capacitor (capacitance: 10 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) and a ceramic capacitor (capacitance: 0.1 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) to the VREFOUT/AVREFP pin for stabilizing the reference voltage. Furthermore, do not apply a voltage from the VREFOUT/AVREFP pin during voltage reference operation.	p.436 ☐
				To use voltage reference output (VREFOUT) to the positive reference voltage of the A/D converter (ADREFP) and the positive reference voltage of the the D/A converter (DAREFP), be sure to set VRON to 1 after setting VRSEL to 1.	p.436 ☐
				Rewriting DACSWn (n = 0, 1) during A/D conversion is prohibited when both the positive reference voltage of the A/D converter (ADREFP) and the positive reference voltage fo the D/A converter (DAREFP) are the voltage reference output (VREFOUT) (VRSEL = 1 and DAREF = 1). Rewrite it when conversion operation is stopped (ADCS = 0).	p.437 ☐
				Do not change the output voltage of the reference voltage by using VRGV during the voltage reference operation (VRON = 1).	p.437 ☐
	Hard		VREFOUT pin	The VREFOUT output voltage can be used only as the positive reference voltage of the internal A/D and D/A converters of the microcontroller. Do not connect an external circuit other than a tantalum capacitor (capacitance: 10 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) and a ceramic capacitor (capacitance: 0.1 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) to the VREFOUT pin for stabilizing the reference voltage.	p.437 ☐
Chapter 14	Soft	Configuration of serial array unit	SDRmn: Lower 8 bits of the serial data register mn	Be sure to clear bit 8 to "0".	p.445 ☐
			PER0: Peripheral enable register 0	When setting serial array unit m, be sure to set SAUmEN to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for input switch control register (ISC), noise filter enable register (NFEN0), port input mode register (PIM1, PIM7), port output mode register (POM1, POM7, POM8), port mode registers (PM1, PM5, PM7, PM8), and port registers (P1, P5, P7, P8)).	p.447 ☐
				After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	p.447 ☐
			SPSm: Serial clock select register m	Be sure to clear bits 15 to 8 to "0".	p.448 ☐
				After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	p.448 ☐
			SMRmn: Serial mode register mn	Be sure to clear bits 13 to 9, 7, 4, and 3 to "0". Be sure to set bit 5 to "1".	p.449 ☐
			SCRmn: Serial communication operation setting register mn	Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".	pp.451 to 453 ☐
			SDRmn: Serial data register mn	Be sure to clear bit 8 to "0".	p.454 ☐
				Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.	p.454 ☐
				Setting SDRmn[15:9] = 0000000B is prohibited when the simplified I^2C is used. Set SDRmn[15:9] to 0000001B or greater.	p.454 ☐

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.0