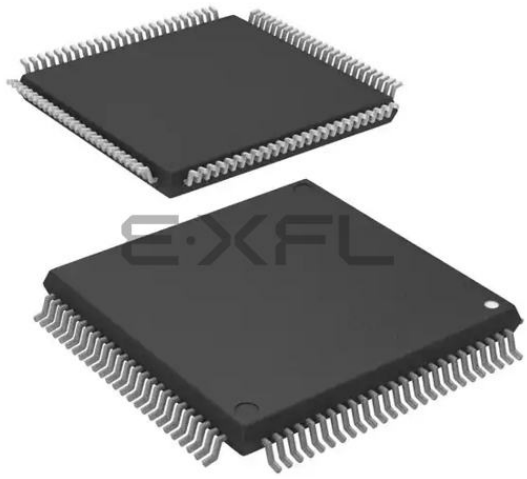
Renesas Electronics America Inc - UPD78F1505AGC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1505agc-ueu-ax

Table 2-4. Connection of Unused Pins (78K0R/LH3) (3/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
<R> P150/ANI8/AMP2+ Note 1	11-N	I/O	Input: Independently connect to AV_{DD0} or AV_{SS} via a resistor. Output: Leave open.
P151/ANI9 Note 1	11-G Note 3		
P152/ANI10 Note 1			
P157/ANI15/AV_{REFM} Note 1, 2	11-T		
SEG0/COM4 to SEG3/COM7	18-F	Output	Leave open.
SEG4 to SEG26	17-T		
COM0 to COM3	18-E		
V_{LC0} to V_{LC2}	–	–	
AV_{DD0}	–	–	<When one or more of P20 to P27, P150 to P152, or P157 are set as a digital port> Make this pin the same potential as EV_{DD} or V_{DD}. <When all of P20 to P27, P150 to P152, and P157 are set as analog ports> Make this pin to have a potential where 2.3 V ≤ AV_{DD0} ≤ V_{DD}.
AV_{DD1}	–	–	<When one or more of P110 or P111 are set as a digital port> Make this pin the same potential as EV_{DD} or V_{DD}. <When all of P110 and P111 are set as analog ports> Make this pin to have a potential where 2.3 V ≤ AV_{DD1} ≤ V_{DD}.
AV_{SS}	–	–	Make this pin the same potential as the EV_{SS} or V_{SS}.
V_{REFOUT}/AV_{REFP}	–	–	Make this pin the same potential as the AV_{DD0}, EV_{DD} or V_{DD}.
FLMD0	2-W	–	Leave open or connect to V_{SS} via a resistor of 100 kΩ or more.
$\overline{\text{RESET}}$	2	Input	Connect directly to EV_{DD} or via a resistor.
REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF).

Notes 1. P150/ANI8/AMP2+ to P152/ANI10 and P157/ANI15/AV_{REFM} are set in the digital input port mode after release of reset.

<R> **2.** AV_{REFM} applies to μPD78F150xA only.

3. μPD78F151xA corresponds to type 11-G.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flags (ISP1, ISP0)

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 by a priority specification flag register (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H) (see **19.3 (3)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

Remark n = 0, 1

(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

Figure 3-10. Format of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves data as shown in Figure 3-11.

Cautions 1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

2. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as a stack area.

3. While using the self-programming function, the area of FFE20H to FFEFFH cannot be used as a stack memory.

Table 5-4. CPU Clock Transition and SFR Register Setting Examples (2/6)

(4) CPU operating with 20 MHz internal high-speed oscillation clock (J) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	DSCCTL Register Note	Waiting for Oscillation Stabilization	DSCCTL Register
	DSCON		SELDSC
(A) → (B) → (J)	1	Necessary (100 μs)	1

Note Check that $V_{DD} \geq 2.7$ V and set DSCON = 1.

(5) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSMC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP	FSEL		MCM0
(B) → (C) (X1 clock: 2 MHz ≤ fX ≤ 10 MHz)	0	1	0	**Note 2**	0	0	Must be checked	1
(B) → (C) (X1 clock: 10 MHz < fX ≤ 20 MHz)	0	1	1	**Note 2**	0	1 Note 3	Must be checked	1
(B) → (C) (external main clock)	1	1	×	**Note 2**	0	0/1	Must not be checked	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Notes 1. The CMC register can be changed only once after reset release. This setting is not necessary if it has already been set.

2. Set the oscillation stabilization time as follows.

- Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS

3. FSEL = 1 when f_{CLK} > 10 MHz

If a divided clock is selected and $f_{CLK} \leq 10$ MHz, use with FSEL = 0 is possible even if f_X > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 31 ELECTRICAL SPECIFICATIONS).

Remarks 1. ×: don't care

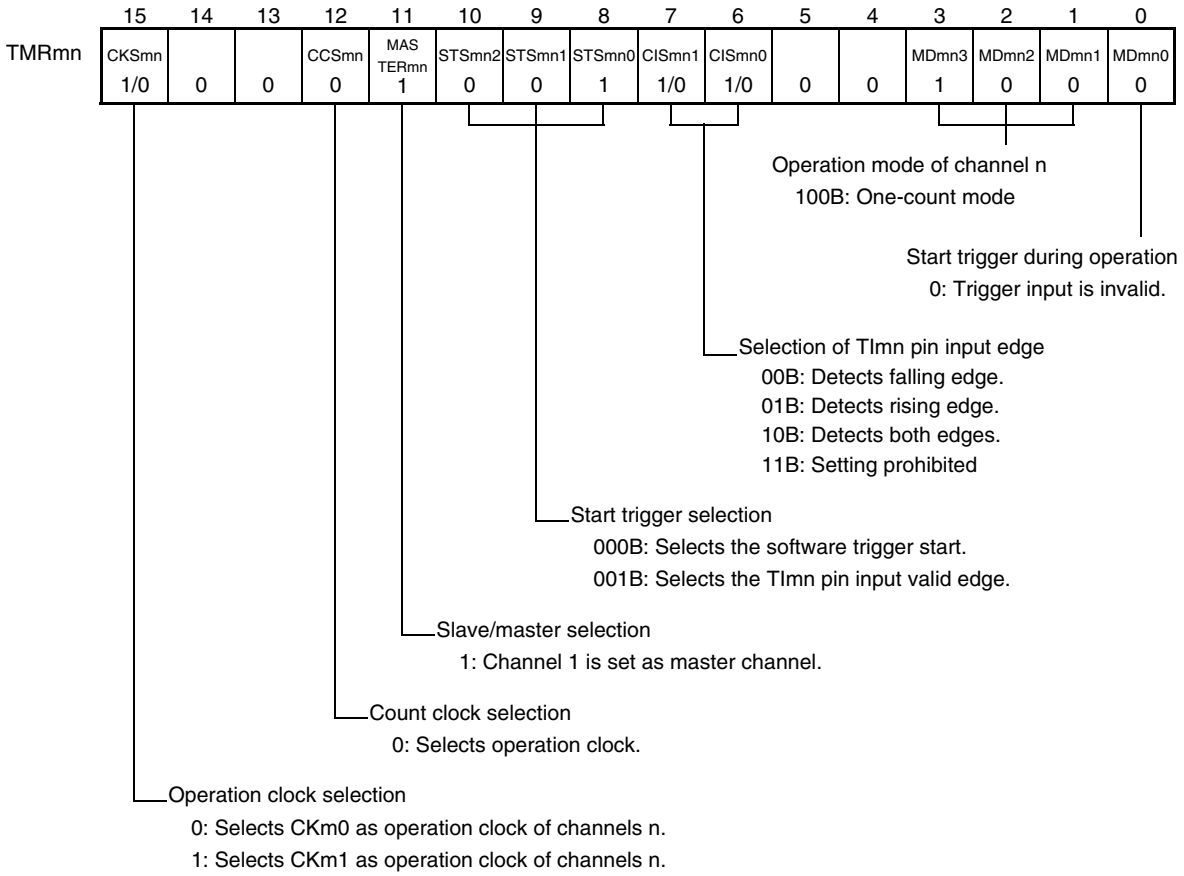
2. (A) to (K) in Table 5-4 correspond to (A) to (K) in Figure 5-15.

Whether each channel of the timer array unit is provided with timer I/O pins differs depending on the product.

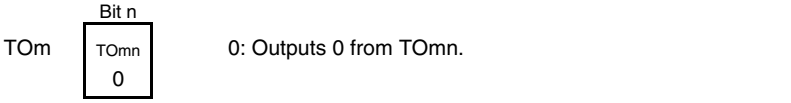
Timer array unit n	Channel m	Input (TIpq) / output (TOpq)	Timer I/O Pins of Each Product		
			78K0R/LF3 (80 pins)	78K0R/LG3 (100 pins)	78K0R/LH3 (128 pins)
0	0	Input	TI00/TO03/P31/RTCDIV/RTCCL/PCLBUZ1/INTP2		
		Output	TO00/TI03/P30RTC1HZ/INTP1		
	1	I/O	TI01/TO01/P32/PCLBUZ0/INTP5		
	2	Input	TI02/P52/SEGxx (78K0R/LF3: xx = 28, 78K0R/LG3: xx = 37, 78K0R/LH3: xx = 51)		
		Output	TO02/P12/SO02/TxD2		
	3	Input	TI03/TO00/P30RTC1HZ/INTP1		
		Output	TO03/TI00/P31/RTCDIV/RTCCL/PCLBUZ1/INTP2		
	4	Input	TI04/P53/SEGxx (78K0R/LF3: xx = 27, 78K0R/LG3: xx = 36, 78K0R/LH3: xx = 50)		
		Output	TO04/P13/SO10/TxD1		
	5	I/O	–	TI05/TO05/P16/INTP10	
	6	I/O		TI06/TO06/P34/INTP8	
	7	I/O	TI07/TO07/P33/INTP3		
1	0	I/O	–		TI10/TO10/P84
	1	I/O			TI11/TO11/P85
	2	I/O			TI12/TO12/P86
	3	I/O			TI13/TO13/P87

Figure 6-64. Example of Set Contents of Registers When One-Shot Pulse Output Function Is Used (Master Channel)

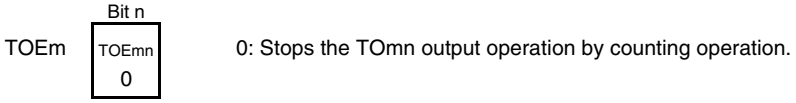
(a) Timer mode register mn (TMRmn)



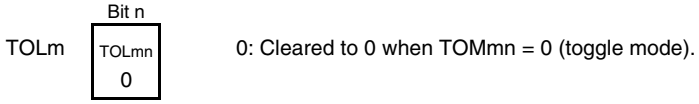
(b) Timer output register m (TOm)



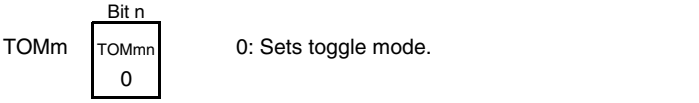
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)



Remarks 1. 78K0R/LF3:
- m = 0, n = 0, 2, 6, p = n+1, TO00 to TO04, TO07, TI00 to TI04, and TI07 pins

2. 78K0R/LG3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07, TI00 to TI07 pins

3. 78K0R/LH3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07, TI00 to TI07 pins
- m = 1, n = 0, 2, p = n+1, TO10 to TO13, TI10 to TI13 pins

Figure 6-66. Operation Procedure of One-Shot Pulse Output Function (1/2)

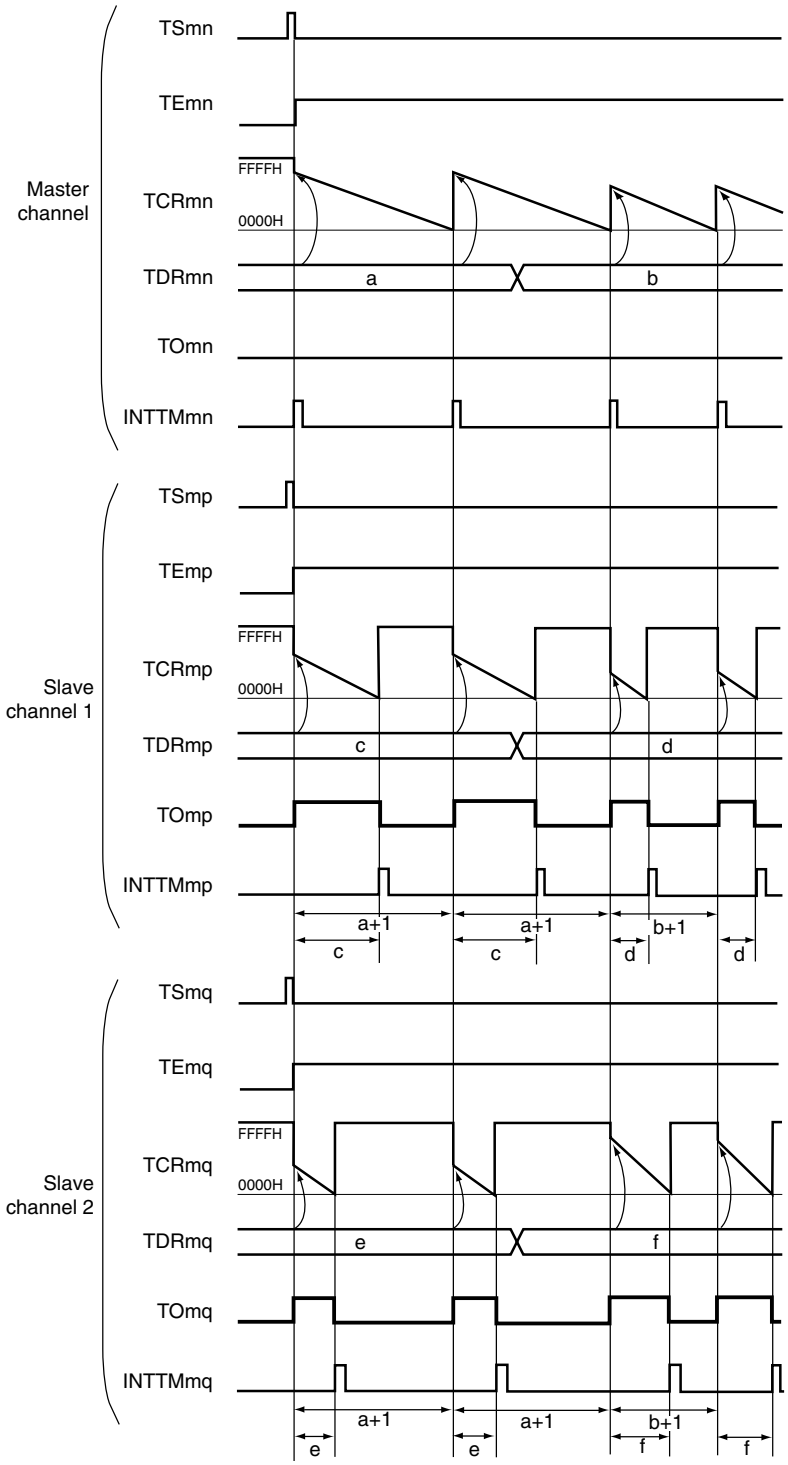
	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN or TAU1EN bits of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSm register. Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the TMRmn and TMRmp registers of two channels to be used (determines operation mode of channels). An output delay is set to the TDRmn register of the master channel, and a pulse width is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of the TOMm register is set to 1 (combination operation mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmn pin goes into Hi-Z output state. The TOmn default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets TOEmp to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

Remarks 1. 78K0R/LF3:
- m = 0, n = 0, 2, 6, p = n+1, TO00 to TO04, and TO07 pins
- Channel 6 of timer array unit 0 can output a one-shot pulse only when software trigger start is selected and it is used as the master channel (because the TI06 pin is not provided).

2. 78K0R/LG3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins

3. 78K0R/LH3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins
- m = 1, n = 0, 2, p = n+1, TO10 to TO13 pins

Figure 6-68. Example of Basic Timing of Operation as Multiple PWM Output Function (output two types of PWMs)



Remarks 1. 78K0R/LF3:
- m = 0, n = 0, 2, p = n+1, q = n+2, TO00 to TO04, and TO07 pins

2. 78K0R/LG3:
- m = 0, n = 0, 2, 4, p = n+1, q = n+2, TO00 to TO07 pins

3. 78K0R/LH3:
- m = 0, n = 0, 2, 4, p = n+1, q = n+2, TO00 to TO07 pins
- m = 1, n = 0, p = 1, q = 2, TO10 to TO13 pins

11.4 Operation of D/A Converter

11.4.1 Operation in normal mode

D/A conversion is performed using write operation to the DACSn register as the trigger. The setting method is described below.

<1> Set bit 6 (DACEN) of peripheral enable register 0 (PER0) to 1 to start the supply of the input clock to the D/A converter.
<2> Set the DAMDn bit of the D/A converter mode register (DAM) to 0 (normal mode).
<3> Use the bit 6 (DAREF) of the DAM register to select the D/A converter reference voltage supply on the positive side.
<4> Use the DARESn bit of the DAM register to select the resolution of the D/A converter.
<5> Set the analog voltage value to be output to the ANOn pin to the D/A conversion value setting register Wn (DACSWn) or D/A conversion value setting register n (DACSn).
Steps <1> and <5> above constitute the initial settings.
<6> Set the DACEn bit of the DAM register to 1 (D/A conversion enable).
After the wait time (20 μs or more) elapses, D/A conversion starts, and then, after the settling time (18 μs (max.)) elapses, the D/A converted analog voltage value is output from the ANOn pin.
<7> To perform subsequent D/A conversions, write to the DACSWn or DACSn register.
The previous D/A conversion result is held until the next D/A conversion is performed.
When the DACEn bit of the DAM register is set to 0 (D/A conversion operation stop), D/A conversion stops, the ANOn pin goes into a high-impedance state when the PM11n bit of the PM11 register = 1 (input mode), and the ANOn pin outputs the set value of the P11 register when the PM11n bit = 0 (output mode).

Cautions 1. Even if 1, 0, and then 1 is set to the DACEn bit, there is a wait after 1 is set for the last time.
2. If the DACSWn or DACSn register is rewritten during the settling time, D/A conversion is aborted and reconversion by using the rewritten values starts.

Remark n = 0, 1

11.4.2 Operation in real-time output mode

D/A conversion is performed using the interrupt request signals (INTTM04 and INTTM05) [Note] of timer channels 4 and 5 as triggers.

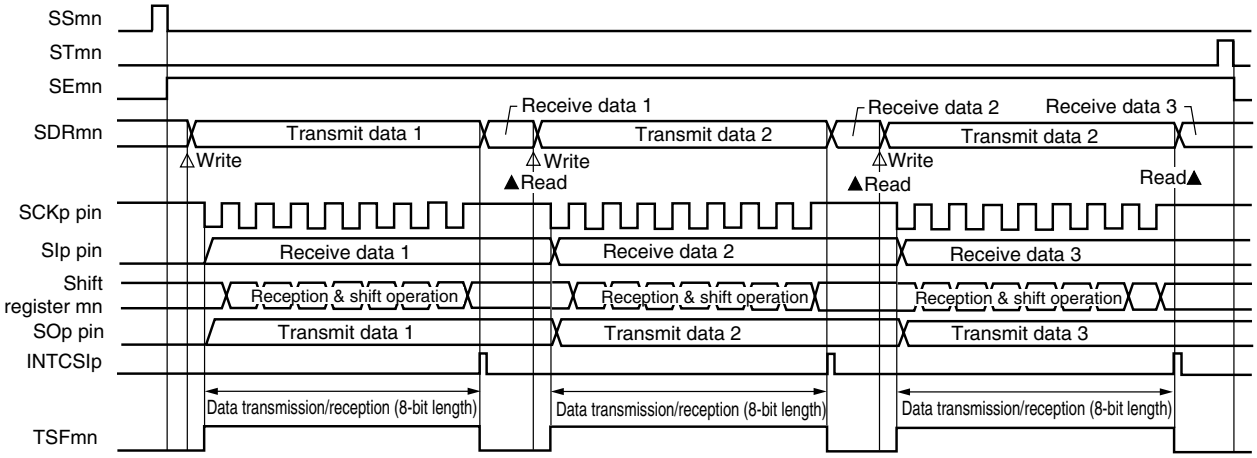
The setting method is described below.

Note Channel 0 of the D/A converter: INTTM04
Channel 1 of the D/A converter: INTTM05

<1> Set bit 6 (DACEN) of peripheral enable register 0 (PER0) to 1 to start the supply of the input clock to the D/A converter.
<2> Set the DAMDn bit of the D/A converter mode register (DAM) to 0 (normal mode).
<3> Use the bit 6 (DAREF) of the DAM register to select the D/A converter reference voltage supply on the positive side.
<4> Use the DARESn bit of the DAM register to select the resolution of the D/A converter.
<5> Set the analog voltage value to be output to the ANOn pin to the D/A conversion value setting register Wn (DACSWn) or D/A conversion value setting register n (DACSn).

(3) Processing flow (in single-transmission/reception mode)

Figure 14-42. Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)

14.7 Operation of Simplified I²C (IIC10, IIC20) Communication

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This communication function is designed to execute single communication with devices such as EEPROM, flash memory, and A/D converter, and therefore, can be used only by the master and does not have a wait detection function. Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function[Note] and ACK detection function
- Data length of 8 bits
  (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Parity error (ACK error)

* [Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection function

Note An ACK is not output when the last data is being received by writing 0 to the SOEmn (SOEm register) bit and stopping the output of serial communication data. See **14.7.3 (2) Processing flow** for details.

Remarks 1. To use the full-function I²C bus, see **CHAPTER 15 SERIAL INTERFACE IICA**.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

The channels supporting simplified I²C (IIC10, IIC20) are channel 2 of SAU0 and channel 0 of SAU1.

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I²C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–

(3) IICA status register (IICS)

This register indicates the status of I^2C.

IICS is read by a 1-bit or 8-bit memory manipulation instruction only when STT = 1 and during the wait period.

Reset signal generation clears this register to 00H.

Caution Reading the IICS register while the address match wakeup function is enabled (WUP = 1) in STOP mode is prohibited. When the WUP bit is changed from 1 to 0 (wakeup operation is stopped), regardless of the INTIICA interrupt request, the change in status is not reflected until the next start condition or stop condition is detected. To use the wakeup function, therefore, enable (SPIE = 1) the interrupt generated by detecting a stop condition and read the IICS register after the interrupt has been detected.

Remark STT: bit 1 of IICA control register 0 (IICCTL0)
WUP: bit 7 of IICA control register 1 (IICCTL1)

Figure 15-7. Format of IICA Status Register (IICS) (1/3)

Address: FFF51H After reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS	MSTS	ALD	EXC	COI	TRC	ACKD	STD	SPD

MSTS	Master status check flag
0	Slave device status or communication standby status
1	Master device communication status

Condition for clearing (MSTS = 0)	Condition for setting (MSTS = 1)
• When a stop condition is detected • When ALD = 1 (arbitration loss) • Cleared by LREL = 1 (exit from communications) • When IICE changes from 1 to 0 (operation stop) • Reset	• When a start condition is generated

ALD	Detection of arbitration loss
0	This status means either that there was no arbitration or that the arbitration result was a “win”.
1	This status indicates the arbitration result was a “loss”. MSTS is cleared.

Condition for clearing (ALD = 0)	Condition for setting (ALD = 1)
• Automatically cleared after IICS is read[Note] • When IICE changes from 1 to 0 (operation stop) • Reset	• When the arbitration result is a “loss”.

EXC	Detection of extension code reception
0	Extension code was not received.
1	Extension code was received.

Condition for clearing (EXC = 0)	Condition for setting (EXC = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL = 1 (exit from communications) • When IICE changes from 1 to 0 (operation stop) • Reset	• When the higher four bits of the received address data is either “0000” or “1111” (set at the rising edge of the eighth clock).

Note This register is also cleared when a 1-bit memory manipulation instruction is executed for bits other than IICS. Therefore, when using the ALD bit, read the data of this bit before the data of the other bits.

Remark LREL: Bit 6 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

Figure 15-8. Format of IICA Flag Register (IICF)

Address: FFF52H After reset: 00H R/W[Note]

Symbol	<7>	<6>	5	4	3	2	<1>	<0>
IICF	STCF	IICBSY	0	0	0	0	STCEN	IICRSV

STCF	STT clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear STT flag

Condition for clearing (STCF = 0)	Condition for setting (STCF = 1)
• Cleared by STT = 1 • When IICE = 0 (operation stop) • Reset	• Generating start condition unsuccessful and STT cleared to 0 when communication reservation is disabled (IICRSV = 1).

IICBSY	I^2C bus status flag
0	Bus release status (communication initial status when STCEN = 1)
1	Bus communication status (communication initial status when STCEN = 0)

Condition for clearing (IICBSY = 0)	Condition for setting (IICBSY = 1)
• Detection of stop condition • When IICE = 0 (operation stop) • Reset	• Detection of start condition • Setting of IICE when STCEN = 0

STCEN	Initial start enable trigger
0	After operation is enabled (IICE = 1), enable generation of a start condition upon detection of a stop condition.
1	After operation is enabled (IICE = 1), enable generation of a start condition without detecting a stop condition.

Condition for clearing (STCEN = 0)	Condition for setting (STCEN = 1)
• Cleared by instruction • Detection of start condition • Reset	• Set by instruction

IICRSV	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation

Condition for clearing (IICRSV = 0)	Condition for setting (IICRSV = 1)
• Cleared by instruction • Reset	• Set by instruction

Note Bits 6 and 7 are read-only.

Cautions 1. Write to STCEN only when the operation is stopped (IICE = 0).

2. As the bus release status (IICBSY = 0) is recognized regardless of the actual bus status when STCEN = 1, when generating the first start condition (STT = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.

3. Write to IICRSV only when the operation is stopped (IICE = 0).

Remark STT: Bit 1 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

Table 16-1. Maximum Number of Pixels (3/3)

(b) 78K0R/LG3

LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
External resistance division	–	Static	COM0 (COM1 to COM3)	54	54 (54 segment signals, 1 common signal)Note 1
	1/2	2	COM0, COM1		108 (54 segment signals, 2 common signals)Note 2
		3	COM0 to COM2		162 (54 segment signals, 3 common signals)Note 3
	1/3	3	COM0 to COM2		
		4	COM0 to COM3		216 (54 segment signals, 4 common signals)Note 4
	1/4	8	COM0 to COM7	50	400 (50 segment signals, 8 common signals)Note 5
Internal voltage boosting	1/3	3	COM0 to COM2	54	162 (54 segment signals, 3 common signals)Note3
		4	COM0 to COM3		216 (54 segment signals, 4 common signals)Note 4
	1/4	8	COM0 to COM7	50	400 (50 segment signals, 8 common signals)Note 5
Capacitor Split	1/3	3	COM0 to COM2	54	162 (54 segment signals, 3 common signals)Note
		4	COM0 to COM3		216 (54 segment signals, 4 common signals)Note 4

Notes 1. 6-digit LCD panel, each digit having an 8-segment configuration.

2. 13-digit LCD panel, each digit having a 4-segment configuration.

3. 20-digit LCD panel, each digit having a 3-segment configuration.

4. 27-digit LCD panel, each digit having a 2-segment configuration.

5. 50-digit LCD panel, each digit having a 1-segment configuration.

Cautions 1. The VLCD setting is valid only when the voltage boost circuit is operating.

2. Bits 5 to 7 must be set to 0.

3. Be sure to change the VLCD value after having stopped the operation of the voltage boost circuit (VLCON = 0).

4. These values above may change after device evaluation.

5. To use the internal voltage boosting method, specify the reference voltage by using the VLCD register (or perform a reset to use the default value of the reference voltage), wait for the reference voltage setup time (2 ms (min.)), and then set VLCON to 1.

(5) Port function register (PFALL)

This register sets whether to use pins P50 to P57, P90 to P97, P100 to P102, and P140 to P147 as port pins (other than segment output pins) or segment output pins.

PFALL is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PFALL to 00H.

Remark The port pins to be used alternatively with the segment output pins vary, depending on the product.

- 78K0R/LF3: P50 to P57, P90 to P92, P100, P140 to P147
- 78K0R/LG3: P50 to P57, P90 to P97, P100, P140 to P147
- 78K0R/LH3: P50 to P57, P90 to P97, P100 to P102, P140 to P147

Figure 16-6. Format of Port Function Register (PFALL) (1/2)

Address: F0080H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	PF14H	PF14L	PF10	PF9H[Note]	PF9L	PF5H	PF5L

PF14H	Port/segment outputs specification of the P144 to P147 pins
0	Used the P144 to P147 pins as port (other than segment output)
1	Used the P144 to P147 pins as segment output

PF14L	Port/segment outputs specification of the P140 to P143 pins
0	Used the P140 to P143 pins as port (other than segment output)
1	Used the P140 to P143 pins as segment output

PF10	Port/segment outputs specification of the P100 to P102 pins
0	Used the P100 to P102 pins as port (other than segment output)
1	Used the P100 to P102 pins as segment output

PF9H	Port/segment outputs specification of the P94 to P97 pins
0	Used the P94 to P97 pins as port (other than segment output)
1	Used the P94 to P97 pins as segment output

PF9L	Port/segment outputs specification of P90 to P93 pins
0	Used the P90 to P93 pins as port (other than segment output)
1	Used the P90 to P93 pins as segment output

Note 78K0R/LG3, 78K0R/LH3 only

Figure 19-9. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (78K0R/LG3) (2/2)

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01H	TMPR004	SREPR02	SRPR02	CSIPR020 IICPR020 STPR02	1	RTCIPR0	RTCPR0	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11H	TMPR104	SREPR12	SRPR12	CSIPR120 IICPR120 STPR12	1	RTCIPR1	RTCPR1	ADPR1

Address: FFFD8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR02L	PPR010	PPR09	PPR08	PPR07	PPR06	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR12L	PPR110	PPR19	PPR18	PPR17	PPR16	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
PR02H	1	1	MDPR0	TMPR013	TMPR012	TMPR011	TMPR010	PPR011

Address: FFFDDH After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
PR12H	1	1	MDPR1	TMPR113	TMPR112	TMPR111	TMPR110	PPR111

XXPR1X	XXPR0X	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Caution Be sure to set bit 3 of PR01H and PR11H, bits 6, 7 of PR02H and PR12H to 1.

CHAPTER 25 REGULATOR

25.1 Regulator Overview

All 78K0R/Lx3 microcontroller products contain a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

The regulator output voltage is normally 2.4 V (TYP.), and in the low-power consumption mode, 1.8 V (TYP.).

25.2 Registers Controlling Regulator

(1) Regulator mode control register (RMC)

This register sets the output voltage of the regulator.

RMC is set with an 8-bit memory manipulation instruction.

Reset input sets this register to 00H.

Figure 25-1. Format of Regulator Mode Control Register (RMC)

Address: F00F4H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
RMC								

RMC[7:0]	Control of output voltage of regulator
5AH	Fixed to low-power consumption mode (1.8 V)
00H	Switches normal power mode (2.4 V) and low-power consumption mode (1.8 V) according to the condition (refer to **Table 25-1**)
Other than above	Setting prohibited

Cautions 1. The RMC register can be rewritten only in the low-power consumption mode (refer to Table 25-1). In other words, rewrite this register during CPU operation with the subsystem clock (f_{XT}) while the high-speed system clock (f_{MX}), the high-speed internal oscillation clock, and the 20 MHz internal high-speed oscillation clock (f_{IH20}) are both stopped.

2. When using the setting fixed to the low consumption current mode, the RMC register can be used in the following cases.

<When the high-speed internal oscillation clock (f_{IH} = 8 MHz (TYP.) or f_{IH} = 1 MHz (TYP.)) is selected as the CPU clock>

$f_{CLK} \leq$ 1 MHz and external oscillator (X1 clock (f_X), external main system clock (f_{EX})) stop.

<When the X1 clock (f_X) or external main system clock (f_{EX}) is selected as the CPU clock>

$f_{CLK} \leq$ 1 MHz, $f_X/f_{EX} \leq$ 5 MHz and the internal high-speed oscillator stop.

<When the subsystem clock (f_{SUB}) is selected as the CPU clock>

Both the internal high-speed oscillator and external oscillator ($f_X/f_{EX} \leq$ 5 MHz) stop or either one stops.

Table 30-5. Operation List (5/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	MOVW	AX, !addr16	3	1	4	AX ← (addr16)			
		!addr16, AX	3	1	–	(addr16) ← AX			
		AX, [DE]	1	1	4	AX ← (DE)			
		[DE], AX	1	1	–	(DE) ← AX			
		AX, [DE + byte]	2	1	4	AX ← (DE + byte)			
		[DE + byte], AX	2	1	–	(DE + byte) ← AX			
		AX, [HL]	1	1	4	AX ← (HL)			
		[HL], AX	1	1	–	(HL) ← AX			
		AX, [HL + byte]	2	1	4	AX ← (HL + byte)			
		[HL + byte], AX	2	1	–	(HL + byte) ← AX			
		AX, word[B]	3	1	4	AX ← (B + word)			
		word[B], AX	3	1	–	(B + word) ← AX			
		AX, word[C]	3	1	4	AX ← (C + word)			
		word[C], AX	3	1	–	(C + word) ← AX			
		AX, word[BC]	3	1	4	AX ← (BC + word)			
		word[BC], AX	3	1	–	(BC + word) ← AX			
		AX, [SP + byte]	2	1	–	AX ← (SP + byte)			
		[SP + byte], AX	2	1	–	(SP + byte) ← AX			
		BC, saddrp	2	1	–	BC ← (saddrp)			
		BC, !addr16	3	1	4	BC ← (addr16)			
		DE, saddrp	2	1	–	DE ← (saddrp)			
		DE, !addr16	3	1	4	DE ← (addr16)			
		HL, saddrp	2	1	–	HL ← (saddrp)			
		HL, !addr16	3	1	4	HL ← (addr16)			
		AX, ES:!addr16	4	2	5	AX ← (ES, addr16)			
		ES:!addr16, AX	4	2	–	(ES, addr16) ← AX			
		AX, ES:[DE]	2	2	5	AX ← (ES, DE)			
		ES:[DE], AX	2	2	–	(ES, DE) ← AX			
		AX, ES:[DE + byte]	3	2	5	AX ← ((ES, DE) + byte)			
		ES:[DE + byte], AX	3	2	–	((ES, DE) + byte) ← AX			
		AX, ES:[HL]	2	2	5	AX ← (ES, HL)			
		ES:[HL], AX	2	2	–	(ES, HL) ← AX			

Notes 1. When the internal RAM area or SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

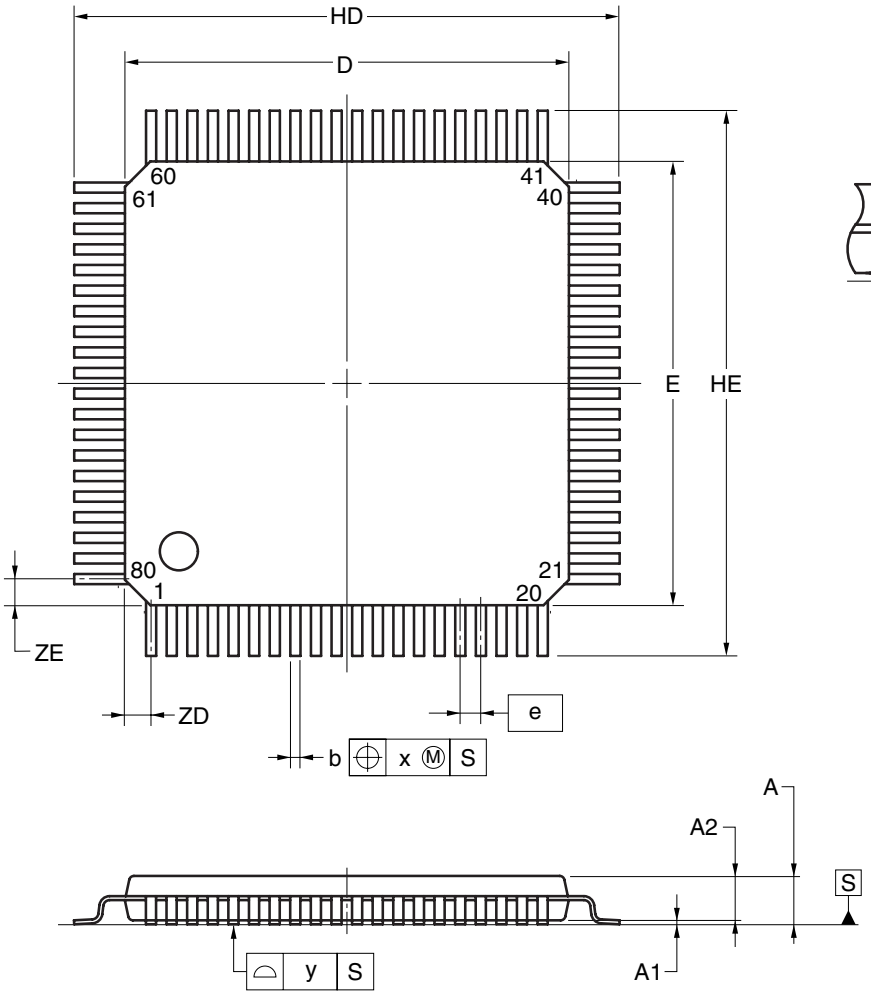
2. This number of clocks is for when the program is in the internal ROM (flash memory) area.

CHAPTER 32 PACKAGE DRAWINGS

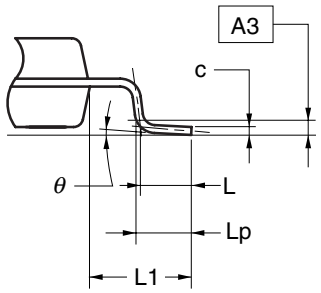
32.1 78K0R/LF3

<R> • μPD78F1500AGC-GAD-AX, 78F1501AGC-GAD-AX, 78F1502AGC-GAD-AX, 78F1510AGC-GAD-AX, 78F1512AGC-GAD-AX

80-PIN PLASTIC LQFP (14x14)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	17.20±0.20
HE	17.20±0.20
A	1.70 MAX.
A1	0.125±0.075
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.80
Lp	0.886±0.15
L1	1.60±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	0.825
ZE	0.825

P80GC-65-GAD

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.