Renesas Electronics America Inc - UPD78F1506AGF-GAT-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1506agf-gat-ax

(1) Port functions (2/2) : 78K0R/LF3

Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG30/RxD3
P51				SEG29/TxD3
P52				SEG28/TI02
P53				SEG27/TI04
P54 to P57				SEG26 to SEG23
P90 to P92	I/O	Port 9. 3-bit I/O port. Inputs/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG22 to SEG20
P100	I/O	Port 10. 1-bit I/O port. Inputs/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG11
<R> P110	I/O	Port 11. 2-bit I/O port. Inputs/output can be specified in 1-bit units.	Input port	ANO0 Note
P111				ANO1 Note
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P130	Output	Port 13. 1-bit output port.	Output port	–
P140 to P147	I/O	Port 14. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG19 to SEG12
<R> P157	I/O	Port 15. 1-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI15/AV_{REFM} Note

<R> **Note** ANOx and AV_{REFM} apply to μPD78F150xA only.

Table 3-5. SFR List (4/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
					1-bit	8-bit	16-bit				
FFF9DH	Real-time counter control register 0	RTCC0		R/W	√	√	–	00H	√	√	√
FFF9EH	Real-time counter control register 1	RTCC1		R/W	√	√	–	00H	√	√	√
FFF9FH	Real-time counter control register 2	RTCC2		R/W	√	√	–	00H	√	√	√
FFFA0H	Clock operation mode control register	CMC		R/W	–	√	–	00H	√	√	√
FFFA1H	Clock operation status control register	CSC		R/W	√	√	–	C0H	√	√	√
FFFA2H	Oscillation stabilization time counter status register	OSTC		R	√	√	–	00H	√	√	√
FFFA3H	Oscillation stabilization time select register	OSTS		R/W	–	√	–	07H	√	√	√
FFFA4H	Clock control register	CKC		R/W	√	√	–	09H	√	√	√
FFFA5H	Clock output select register 0	CKS0		R/W	√	√	–	00H	√	√	√
FFFA6H	Clock output select register 1	CKS1		R/W	√	√	–	00H	√	√	√
FFFA8H	Reset control flag register	RESF		R	–	√	–	Undefined Note 1	√	√	√
FFFA9H	Low-voltage detection register	LVIM		R/W	√	√	–	00H Note 2	√	√	√
FFFAAH	Low-voltage detection level select register	LVIS		R/W	√	√	–	0EH Note 3	√	√	√
FFFABH	Watchdog timer enable register	WDTE		R/W	–	√	–	1A/9A Note 4	√	√	√
FFFB0H	DMA SFR address register 0	DSA0		R/W	–	√	–	00H	√	√	√
FFFB1H	DMA SFR address register 1	DSA1		R/W	–	√	–	00H	√	√	√
FFFB2H	DMA RAM address register 0L	DRA0L	DRA0	R/W	–	√	√	00H	√	√	√
FFFB3H	DMA RAM address register 0H	DRA0H		R/W	–	√		00H	√	√	√
FFFB4H	DMA RAM address register 1L	DRA1L	DRA1	R/W	–	√	√	00H	√	√	√
FFFB5H	DMA RAM address register 1H	DRA1H		R/W	–	√		00H	√	√	√
FFFB6H	DMA byte count register 0L	DBC0L	DBC0	R/W	–	√	√	00H	√	√	√
FFFB7H	DMA byte count register 0H	DBC0H		R/W	–	√		00H	√	√	√
FFFB8H	DMA byte count register 1L	DBC1L	DBC1	R/W	–	√	√	00H	√	√	√
FFFB9H	DMA byte count register 1H	DBC1H		R/W	–	√		00H	√	√	√
FFFBAH	DMA mode control register 0	DMC0		R/W	√	√	–	00H	√	√	√
FFFBBH	DMA mode control register 1	DMC1		R/W	√	√	–	00H	√	√	√
FFFBCH	DMA operation control register 0	DRC0		R/W	√	√	–	00H	√	√	√
FFFBDH	DMA operation control register 1	DRC1		R/W	√	√	–	00H	√	√	√
FFFBEH	Back ground event control register	BECTL		R/W	√	√	–	00H	√	√	√
FFFC0H	–	PFCMD Note 5		–	–	–	–	Undefined	√	√	√
FFFC2H	–	PFS Note 5		–	–	–	–	Undefined	√	√	√
FFFC4H	–	FLPMC Note 5		–	–	–	–	Undefined	√	√	√

Notes 1. The reset value of RESF varies depending on the reset source.

2. The reset value of LVIM varies depending on the reset source and the setting of the option byte.

3. The reset value of LVIS varies depending on the reset source.

4. The reset value of WDTE is determined by the setting of the option byte.

5. Do not directly operate this SFR, because it is to be used in the self programming library.

Remark pq: Unit number + Channel number (only for channels provided with timer I/O pins)

<1> 78K0R/LF3:

- p = 0, q = 0 to 4, 7 (q = 0, 2, 4 for master channel)
  q < r ≤ 7 (where r is a consecutive integer greater than q)

<2> 78K0R/LG3:

- p = 0, q = 0 to 7 (q = 0, 2, 4, 6 for master channel)
  q < r ≤ 7 (where r is a consecutive integer greater than q)

<3> 78K0R/LH3:

- p = 0, q = 0 to 7 (q = 0, 2, 4, 6 for master channel)
  q < r ≤ 7 (where r is a consecutive integer greater than q)
- p = 1, q = 0 to 3 (q = 0, 2 for master channel)
  q < r ≤ 3 (where r is a consecutive integer greater than q)

(13) Input switch control register (ISC)

ISC is used to implement LIN-bus communication operation with channel 7 of timer array unit 0 in association with serial array unit 1.

When bit 1 of this register is set to 1, the input signal of the serial data input pin (RxD3) is selected as a timer input signal.

ISC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6-22. Format of Input Switch Control Register (ISC)

Address: FFF3CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	ISC4	ISC3	ISC2	ISC1	ISC0

ISC1	Switching channel 7 input of timer array unit
0	Uses the input signal of the TI07 pin as a timer input (normal operation).
1	Input signal of RxD3 pin is used as timer input (wakeup signal detection).

Caution Be sure to clear bits 5 to 7 to "0".

Remarks 1. When the LIN-bus communication function is used, select the input signal of the RxD3 pin by setting ISC1 to 1.

2. Bits 0 and 2 to 4 of ISC are not used with TAU0.

7.4.2 Shifting to STOP mode after starting operation

Perform one of the following processing when shifting to STOP mode immediately after setting RTCE to 1.

However, after setting RTCE to 1, this processing is not required when shifting to STOP mode after the first INTRTC interrupt has occurred.

- Shifting to STOP mode when at least two subsystem clocks (f_{SUB}) (about 62 μs) have elapsed after setting RTCE to 1 (see **Figure 7-20**, **Example 1**).
- Checking by polling RWST to become 1, after setting RTCE to 1 and then setting RWAIT to 1. Afterward, setting RWAIT to 0 and shifting to STOP mode after checking again by polling that RWST has become 0 (see **Figure 7-20**, **Example 2**).

Figure 7-20. Procedure for Shifting to STOP Mode After Setting RTCE to 1

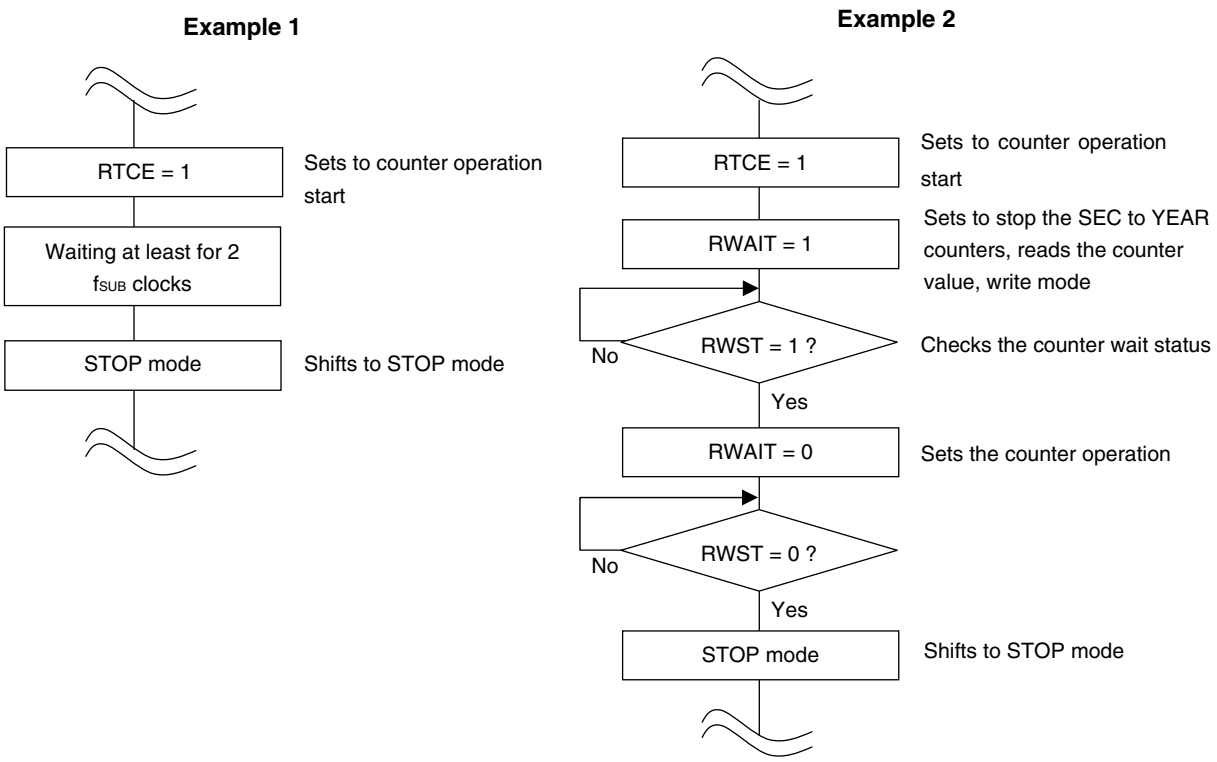
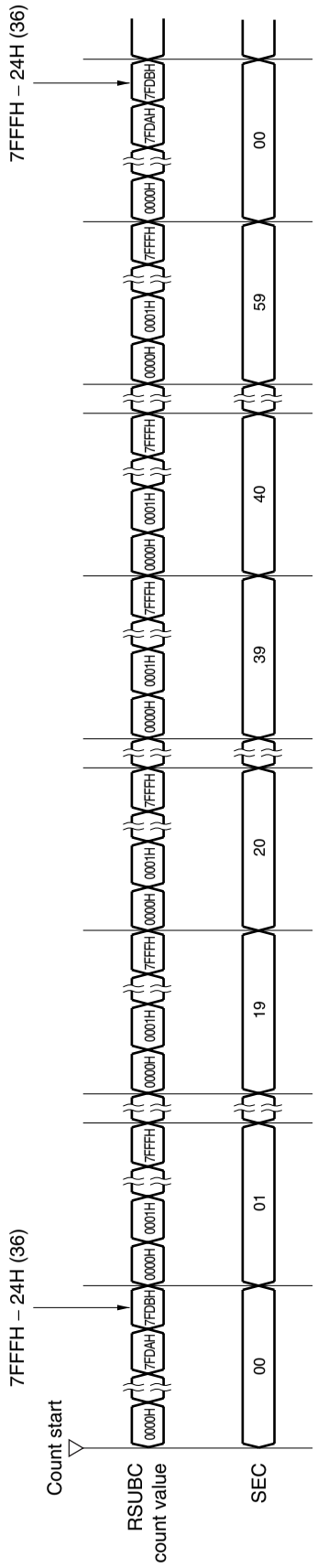


Figure 7-28. Operation When (DEV, F6, F5, F4, F3, F2, F1, F0) = (1, 1, 1, 0, 1, 1, 1, 0)



10.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

(1) ANI0 to ANI10, ANI15 pins

These are the analog input pins of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

Remark 78K0R/LF3: ANI0-ANI6, ANI15
78K0R/LG3, 78K0R/LH3: ANI0-ANI10, ANI15

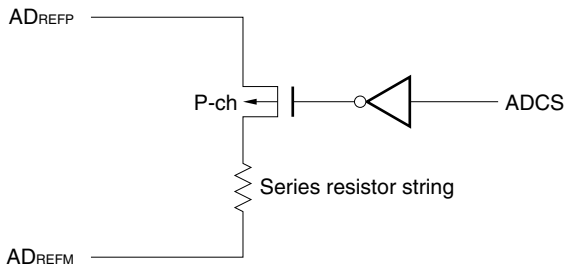
(2) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

(3) Series resistor string

The series resistor string is connected between AD_{REFP} and AD_{REFM}, and generates a voltage to be compared with the sampled voltage value.

Figure 10-3. Circuit Configuration of Series Resistor String



(4) Voltage comparator

The voltage comparator compares the sampled voltage value and the output voltage of the series resistor string.

(5) Successive approximation register (SAR)

This register converts the result of comparison by the voltage comparator, starting from the most significant bit (MSB). When the voltage value is converted into a digital value down to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register are transferred to the A/D conversion result register (ADCR).

Table 10-2. A/D Conversion Time Selection

A/D Converter Mode Register (ADM)					Mode	Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0			f_{CLK} = 1 MHz	f_{CLK} = 8 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	
0	0	0	0	0	Normal mode 1 Note 1	240/f_{CLK}	Setting prohibited	30 μs	24 μs	12 μs	f_{CLK}/12
0	0	1				160/f_{CLK}		20 μs	16 μs	8 μs	f_{CLK}/8
0	1	0				120/f_{CLK}		15 μs	12 μs	6 μs	f_{CLK}/6
0	1	1				100/f_{CLK}		12.5 μs	10 μs	5 μs	f_{CLK}/5
1	0	0				80/f_{CLK}		10 μs	8 μs	Setting prohibited	f_{CLK}/4
1	0	1				60/f_{CLK}		7.5 μs	6 μs		f_{CLK}/3
1	1	0				40/f_{CLK}	40 μs	5 μs	Setting prohibited		f_{CLK}/2
1	1	1				20/f_{CLK}	20 μs	Setting prohibited			f_{CLK}
0	0	0	0	1	Normal mode 2 Note 2	240/f_{CLK}	Setting prohibited	30 μs	24 μs	12 μs	f_{CLK}/12
0	0	1				160/f_{CLK}		20 μs	16 μs	8 μs	f_{CLK}/8
0	1	0				120/f_{CLK}		15 μs	12 μs	6 μs	f_{CLK}/6
0	1	1				100/f_{CLK}		12.5 μs	10 μs	5 μs	f_{CLK}/5
1	0	0				80/f_{CLK}		10 μs	8 μs	Setting prohibited	f_{CLK}/4
1	0	1				60/f_{CLK}		7.5 μs	6 μs		f_{CLK}/3
1	1	0				40/f_{CLK}	40 μs	5 μs	Setting prohibited		f_{CLK}/2
1	1	1				20/f_{CLK}	20 μs	Setting prohibited			f_{CLK}
0	0	0	1	0	Low voltage mode Note 3	300/f_{CLK}	Setting prohibited	37.5 μs	30 μs	15 μs Note 4	f_{CLK}/12
0	0	1				200/f_{CLK}		25 μs	20 μs Note 4	10 μs Note 4	f_{CLK}/8
0	1	0				150/f_{CLK}		18.8 μs Note 4	15 μs Note 4	7.5 μs Note 4	f_{CLK}/6
0	1	1				125/f_{CLK}		15.6 μs Note 4	12.5 μs Note 4	6.25 μs Note 4	f_{CLK}/5
1	0	0				100/f_{CLK}		12.5 μs Note 4	10 μs Note 4	Setting prohibited	f_{CLK}/4
1	0	1				75/f_{CLK}		9.38 μs Note 4	7.5 μs Note 4		f_{CLK}/3
1	1	0				50/f_{CLK}	50 μs	6.25 μs Note 4	Setting prohibited		f_{CLK}/2
1	1	1				25/f_{CLK}	25 μs	Setting prohibited			f_{CLK}
Other than above					Setting prohibited						

Notes 1. Normal mode 1: 2.7 V ≤ AV_{DD0} ≤ 5.5 V, when operation of the input gate voltage boost circuit for the A/D converter is stopped.

2. Normal mode 2: 2.3 V ≤ AV_{DD0} ≤ 5.5 V, when operation of the input gate voltage boost circuit for the A/D converter is operating.

3. Low voltage mode: 1.8 V ≤ AV_{DD0} ≤ 5.5 V, when operation of the input gate voltage boost circuit for the A/D converter is operating.

4. When T_A = 0 to 50°C and 2.3 V ≤ AV_{DD0} ≤ 3.6 V.

Caution When using the A/D converter in normal mode 2 (LV1 = 0, LV0 = 1) or low voltage mode (LV1 = 1, LV0 = 0), enable the input gate voltage boost circuit for the A/D converter by using the analog reference voltage control register (ADVRC), and then set ADCE and ADCS to 1. After the voltage boost circuit stabilization time (10 μs) passes after the input gate voltage boost circuit for the A/D converter has been enabled, set ADCS to 1.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

11.3 Registers Used in D/A Converter

The D/A converter uses the following four registers.

- Peripheral enable register 0 (PER0)
- D/A converter mode register (DAM)
- D/A conversion value setting registers W0, W1 (DACSW0, DACSW1)
- D/A conversion value setting registers 0, 1 (DACS0, DACS1)

(1) Peripheral enable register 0 (PER0)

PER0 is used to enable or disable use of each peripheral hardware macro. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the D/A converter is used, be sure to set bit 6 (DACEN) of this register to 1.

PER0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Cautions When setting the D/A converter, be sure to set DACEN to 1 first. If DACEN = 0, writing to a control register of the D/A converter is ignored, and, even if the register is read, only the default value is read.

Figure 11-2. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	DACEN	ADCEN	IICAEN Note	SAU1EN	SAU0EN	TAU1EN	TAU0EN

DACEN	Control of D/A converter input clock
0	Stops supply of input clock. • SFR used by the D/A converter cannot be written. • The D/A converter is in the reset status.
1	Supplies input clock. • SFR used by the D/A converter can be read/written.

Note 78K0R/LG3, 78K0R/LH3 only

(1) Shift register

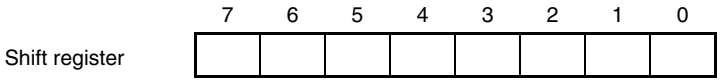
This is an 8-bit register that converts parallel data into serial data or vice versa.

During reception, it converts data input to the serial pin into parallel data.

When data is transmitted, the value set to this register is output as serial data from the serial output pin.

The shift register cannot be directly manipulated by program.

To read or write the shift register, use the lower 8 bits of serial data register mn (SDRmn).



(2) Lower 8 bits of the serial data register mn (SDRmn)

SDRmn is the transmit/receive data register (16 bits) of channel n. Bits 7 to 0 function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (MCK).

When data is received, parallel data converted by the shift register is stored in the lower 8 bits. When data is to be transmitted, set transmit to be transferred to the shift register to the lower 8 bits.

The data stored in the lower 8 bits of this register is as follows, depending on the setting of bits 0 to 2 (DLSmn0 to DLSmn2) of the SCRmn register, regardless of the output sequence of the data.

- 5-bit data length (stored in bits 0 to 4 of SDRmn register) (settable in UART mode only)
- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)

SDRmn can be read or written in 16-bit units.

The lower 8 bits of SDRmn of SDRmn can be read or written[Note] as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

Reset signal generation clears this register to 0000H.

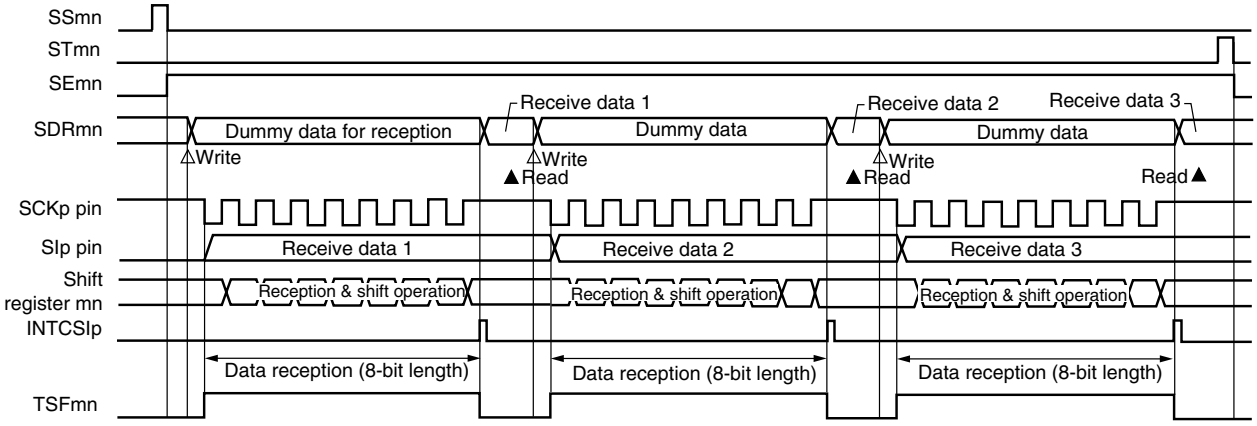
Note Writing in 8-bit units is prohibited when the operation is stopped (SEmn = 0).

Remarks 1. After data is received, “0” is stored in bits 0 to 7 in bit portions that exceed the data length.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 20), q: UART number (q = 0 to 3), r: IIC number (r = 10, 20)

(3) Processing flow (in single-reception mode)

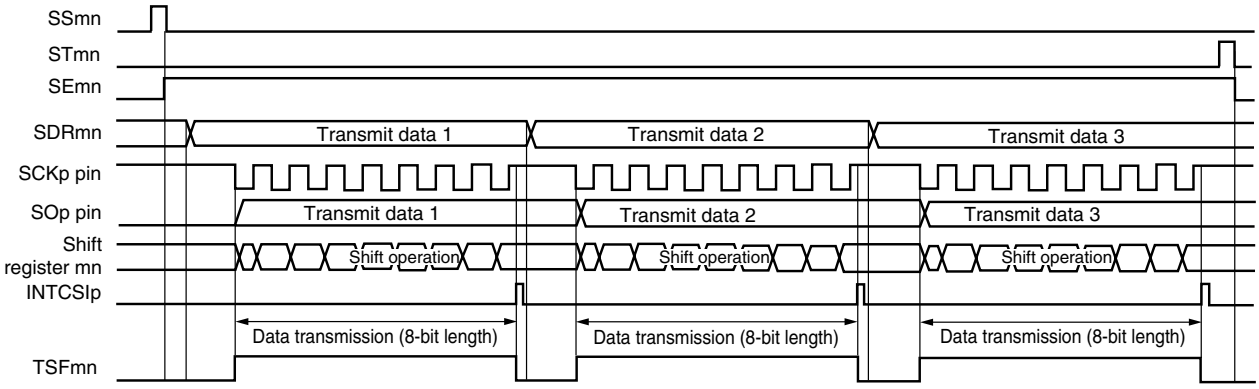
Figure 14-36. Timing Chart of Master Reception (in Single-Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)

(3) Processing flow (in single-transmission mode)

Figure 14-50. Timing Chart of Slave Transmission (in Single-Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)

14.6 Operation of UART (UART0, UART1, UART2, UART3) Communication

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. It transmits or receives data in asynchronization with the party of communication (by using an internal baud rate). Full-duplex UART communication can be realized by using two channels, one dedicated to transmission (even channel) and the other to reception (odd channel).

[Data transmission/reception]

- Data length of 5, 7, or 8 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

The LIN-bus is supported in UART3 (2, 3 channels of unit 1)

[LIN-bus functions]

- Wakeup signal detection
- Sync break field (SBF) detection
- Sync field measurement, baud rate calculation

} External interrupt (INTP0) or timer array unit (TAU) is used.

UART0 uses channels 0 and 1 of SAU0.
UART1 uses channels 2 and 3 of SAU0.
UART2 uses channels 0 and 1 of SAU1.
UART3 uses channels 2 and 3 of SAU1.

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–

Caution When using serial array units 0 and 1 as UARTs, the channels of both the transmitting side (even-number channel) and the receiving side (odd-number channel) can be used only as UARTs.

Remark For 78K0R/LF3, UART0 is not mounted.

14.8 Processing Procedure in Case of Error

The processing procedure to be followed if an error of each type occurs is described in Figures 14-100 to 14-102.

Figure 14-100. Processing Procedure in Case of Parity Error or Overrun Error

Software Manipulation	Hardware Status	Remark
Reads SDRmn register. →	BFF = 0, and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads SSRmn register.		Error type is identified and the read value is used to clear error flag.
Writes SIRmn register. →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

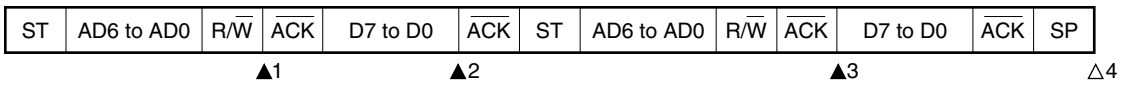
Figure 14-101. Processing Procedure in Case of Framing Error

Software Manipulation	Hardware Status	Remark
Reads SDRmn register. →	BFF = 0, and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads SSRmn register.		Error type is identified and the read value is used to clear error flag.
Writes SIRmn register. →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets STmn bit to 1. →	SEmn = 0, and channel n stops operation.	
Synchronization with other party of communication		Synchronization with the other party of communication is re-established and communication is resumed because it is considered that a framing error has occurred because the start bit has been shifted.
Sets SSmn bit to 1. →	SEmn = 1, and channel n is enabled to operate.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

(d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

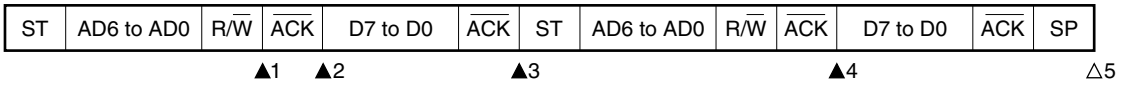
(i) When WTIM = 0 (after restart, does not match address (= not extension code))



▲1: IICS = 00100010B
▲2: IICS = 00100000B
▲3: IICS = 00000110B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, does not match address (= not extension code))



▲1: IICS = 00100010B
▲2: IICS = 00100110B
▲3: IICS = 00100×00B
▲4: IICS = 00000110B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(2) Internal voltage boosting method

<1> Set the internal voltage boosting method via the MDSET0 and MDSET1 bits (bits 4 and 5 of the LCDMD register) (MDSET0 = 1, MDSET1 = 0).
<2> To use segment output only pins, use the SEGEN register to enable segment output to them.
To use segment output pins, which are alternatively used with port pins, use the PFALL register to set them to segment output. In addition, to use the segment output pins, which are alternatively used with the TI04, TI02, and RxD3 pins, use the ISC register to disable input to the Schmitt trigger buffer.
<3> Set the display data in LCD display RAM.
<4> Set the number of time slices and the bias mode via the LCDM0 to LCDM2 bits (bits 0 to 2 of the LCDM register).
- When setting Static, 2-time-slice, 3-time-slice, or 4-time-slice → Go to step <5>
- When setting 8-time-slice → Go to step <6>

(Only 1/3 bias mode and 1/4 bias mode can be set for the internal voltage boost method.)
<5> Select the display data area via the LCDSEL and BLON bits (bits 3 and 4 of the LCDM register).
<6> Set the LCD source clock and LCD clock via the LCDC0 register.
<7> Set the reference voltage (adjust the contrast) via the VLCD register.
<8> Wait for the reference voltage setup time (2 ms (min.)) after setting of the VLCD register.
<9> Set (VLCON = 1) the VLCON bit (bit 5 of the LCDM register) to start the voltage boost circuit operation.
<10> Wait for the voltage boost wait time after setting of VLCON (see **CHAPTER 31 ELECTRICAL SPECIFICATIONS**).
<11> Set (SCOC = 1) the SCOC bit (bit 6 of the LCDM register).
Non-selected waveforms are output from all the segment and common pins, and the non-display status is entered.
<12> Start output corresponding to each data memory by setting (LCDON = 1) the LCDON bit (bit 7 of the LCDM register).

Caution When stopping the operation of the voltage boost circuit, be sure to set SCOC and LCDON to 0 before setting VLCON to 0.

(3) Capacitor split method

<1> Set the capacitor split method via the MDSET0 and MDSET1 bits (bits 4 and 5 of the LCDMD register) (MDSET0 = 0, MDSET1 = 1).
<2> To use segment output only pins, use the SEGEN register to enable segment output to them.
To use segment output pins, which are alternatively used with port pins, use the PFALL register to set them to segment output. In addition, to use the segment output pins, which are alternatively used with the TI04, TI02, and RxD3 pins, use the ISC register to disable input to the Schmitt trigger buffer.
<3> Set the display data in LCD display RAM.
<4> Set the number of time slices and the bias mode via the LCDM0 to LCDM2 bits (bits 0 to 2 of the LCDM register).
(Only 1/3 bias mode can be set for the capacitor split method)
<5> Select the display data area via the LCDSEL and BLON bits (bits 3 and 4 of the LCDM register).
<6> Set the LCD source clock and LCD clock via the LCDC0 register.
<7> Set (VLCON = 1) the VLCON bit (bit 5 of the LCDM register) to start the voltage reduction circuit operation.
<8> Wait for the voltage capacitor split wait time after setting of VLCON (see **CHAPTER 31 ELECTRICAL SPECIFICATIONS**).

16.7.4 Four-time-slice display example

Figure 16-26 shows how the 12-digit LCD panel having the display pattern shown in Figure 16-25 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM3). This example displays data "123456.789012" in the LCD panel. The contents of the display data memory (addresses F0400H to F0417H) correspond to this display.

The following description focuses on numeral "6." (6.) displayed in the seventh digit. To display "6." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 and SEG13 pins according to Table 16-8 at the timing of the common signals COM0 to COM3; see Figure 16-25 for the relationship between the segment signals and LCD segments.

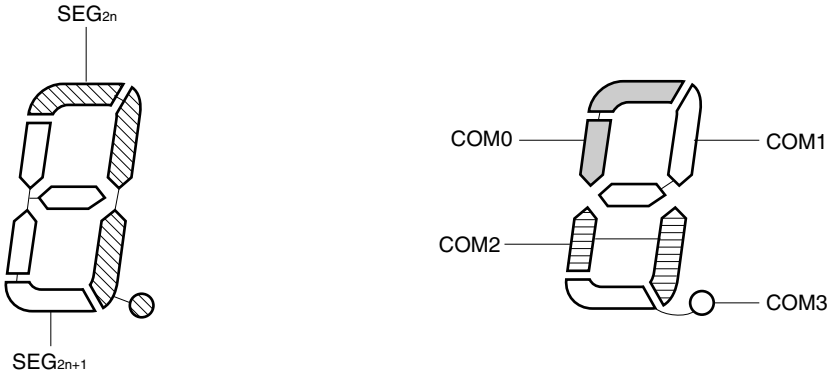
Table 16-8. Select and Deselect Voltages (COM0 to COM3)

Segment / Common	SEG12	SEG13
COM0	Select	Select
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

According to Table 16-8, it is determined that the display data memory location (F040CH) that corresponds to SEG12 must contain 1101.

Figure 16-27 shows examples of LCD drive waveforms between the SEG12 signal and each common signal. When the select voltage is applied to SEG12 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 16-25. Four-Time-Slice LCD Display Pattern and Electrode Connections



Remark 78K0R/LF3: n = 0 to 14
78K0R/LG3: n = 0 to 19
78K0R/LH3: n = 0 to 26

19.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)
- External interrupt rising edge enable registers (EGP0, EGP1)
- External interrupt falling edge enable registers (EGN0, EGN1)
- Program status word (PSW)

Table 19-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 19-2. Flags Corresponding to Interrupt Request Sources (1/2)

LF3	LG3	LH3	Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
					Register		Register		Register
√	√	√	INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L
√	√	√	INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1	
√	√	√	INTP0	PIF0		PMK0		PPR00, PPR10	
√	√	√	INTP1	PIF1		PMK1		PPR01, PPR11	
√	√	√	INTP2	PIF2		PMK2		PPR02, PPR12	
√	√	√	INTP3	PIF3		PMK3		PPR03, PPR13	
√	√	√	INTP4	PIF4		PMK4		PPR04, PPR14	
√	√	√	INTP5	PIF5		PMK5		PPR05, PPR15	
√	√	√	INTST3	STIF3	IF0H	STMK3	MK0H	STPR03, STPR13	PR00H, PR10H
√	√	√	INTSR3	SRIF3		SRMK3		SRPR03, SRPR13	
√	√	√	INTSRE3	SREIF3		SREMK3		SREPR03, SREPR13	
√	√	√	INTDMA0	DMAIF0		DMAMK0		DMAPR00, DMAPR10	
√	√	√	INTDMA1	DMAIF1		DMAMK1		DMAPR01, DMAPR11	
–	√	√	INTST0 Note 1	STIF0 Note 1		STMK0 Note 1		STPR00, STPR10 Note 1	
–	√	√	INTCSI00 Note 1	CSIIF00 Note 1		CSIMK00 Note 1		CSIPR000, CSIPR100 Note1	
–	√	√	INTSR0 Note 2	SRIF0 Note 2		SRMK0 Note 2		SRPR00, SRPR10 Note 2	
–	–	√	INTCSI01 Note 2	CSIIF01 Note 2		CSIMK01 Note 2		CSIPR001, CSIPR101 Note2	
√	√	√	INTSRE0	SREIF0		SREMK0		SREPR00, SREPR10	

Notes 1. Do not use UART0 and CSI00 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTST0 and INTCSI00 is generated, bit 5 of IF1H is set to 1. Bit 5 of MK0H, PR00H, and PR10H supports these two interrupt sources.

2. Do not use UART0 and CSI01 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTSR0 and INTCSI01 is generated, bit 6 of IF0H is set to 1. Bit 6 of MK0H, PR00H, and PR10H supports these two interrupt sources.

Figure 24-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFFA9H After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
LVIM	LVION	0	0	0	0	LVISEL	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVISEL[Note 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from external input pin (EXLVI)

LVIMD[Note 3]	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when LVI operation is disabled • LVISEL = 1: Input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI}), or when LVI operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI})

Notes 1. The reset value changes depending on the reset source and the setting of the option byte.
This register is not cleared (00H) by LVI reset.
It is set to “82H” when a reset signal other than LVI is applied if option byte LVIOFF = 0, and to “00H” if option byte LVIOFF = 1.

2. Bit 0 is read-only.

3. LVION, LVIMD, and LVISEL are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	Typ. = 10 MHz, Max. = 20 MHz				6	20	mA
Number of rewrites per chip	C_{erwr}	1 erase + 1 write after erase = 1 rewrite Note	When a flash memory programmer is used, and the libraries provided by Renesas Electronics are used	Retention: 15 years	1000			Times
			When the EEPROM emulation libraries provided by Renesas Electronics are used	Retention :5 years	10000			Times

Note When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

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