Renesas Electronics America Inc - UPD78F1507AGF-GAT-AX Datasheet

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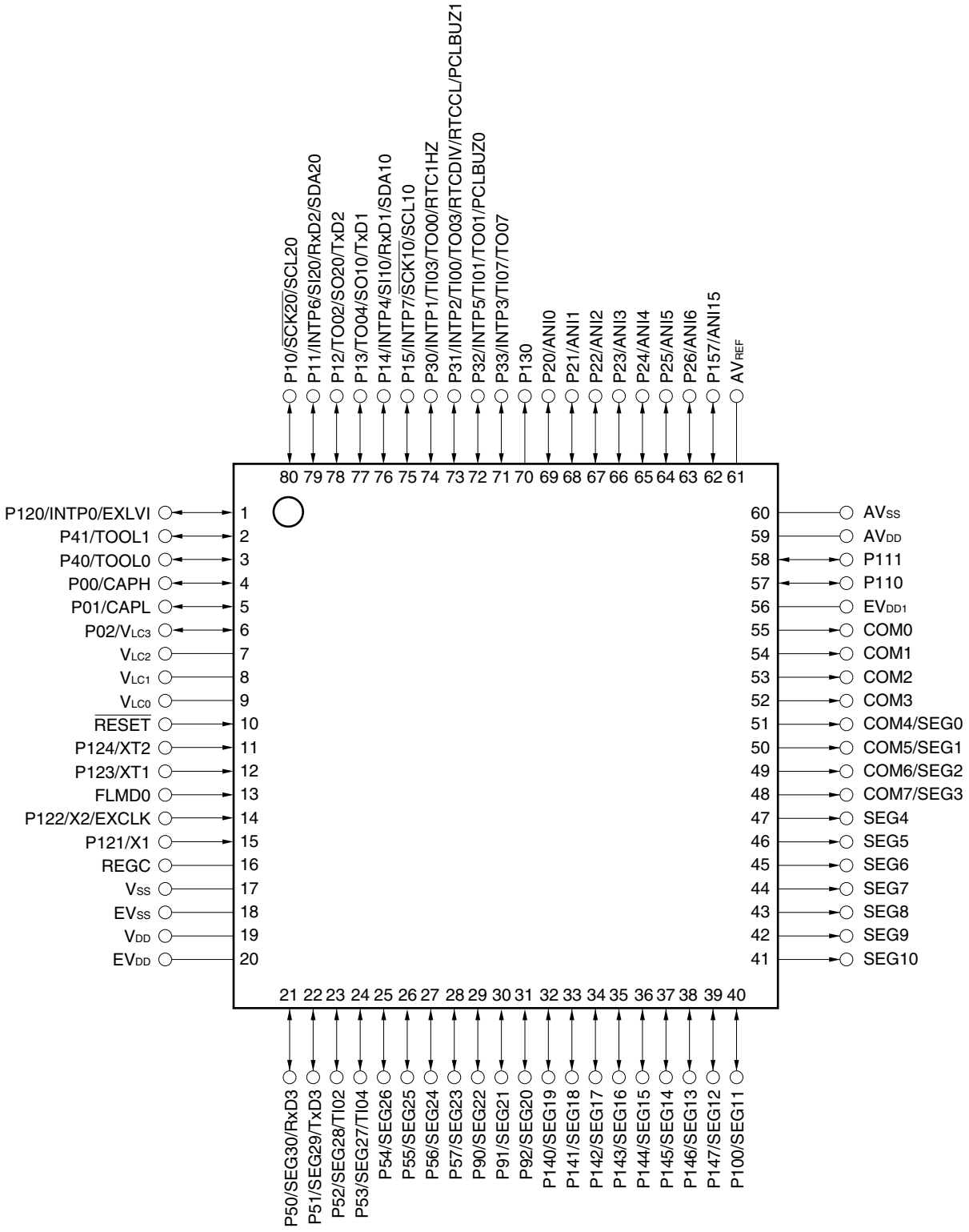
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1507agf-gat-ax

<R> (2) μPD78F150xA



Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

(2) Non-port functions (4/4) : 78K0R/LF3

Function Name	I/O	Function	After Reset	Alternate Function
<R> AV_{DD} Note 1 AV_{DD} Note 2	–	Positive power supply for P20 to P26, P157	–	–
AV_{DD1} Note 1 EV_{DD1} Note 2	–	Positive power supply for P110, P111	–	–
V_{SS}	–	Ground potential (Pins other than port and $\overline{RESET}$, FLMD0 pins)	–	–
EV_{SS}	–	Ground potential for $\overline{RESET}$, FLMD0 pins, and port pins other than P20 to P26, P110, P111, P157	–	–
AV_{SS}	–	Ground potential for P20 to P26, P110, P111, P157	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

<R> **Notes 1.** AV_{DD0} and AV_{DD1} apply to μPD78F150xA only.

2. AV_{DD} and EV_{DD1} apply to μPD78F151xA only.

4.2.11 Port 10

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P100/SEGxx	√ (xx = 11)	√ (xx = 15)	√ (xx = 29)
P101/SEGxx	–	–	√ (xx = 28)
P102/SEGxx	–	–	√ (xx = 27)

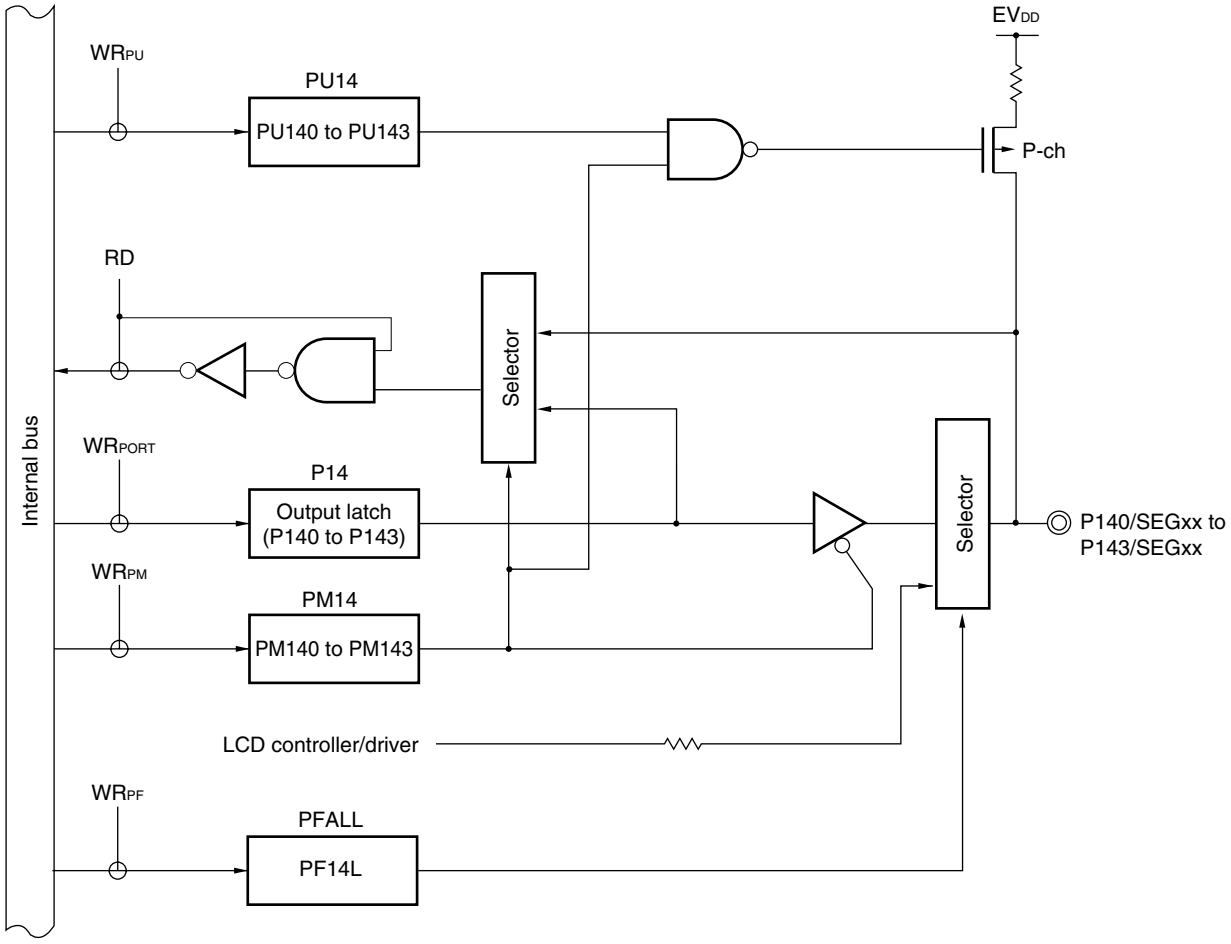
Port 10 is an I/O port with an output latch. Port 10 can be set to the input mode or output mode in 1-bit units using port mode register 10 (PM10). When the P100 to P102 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 10 (PU10).

This port can also be used for segment output.

Reset signal generation sets port 10 to input mode.

Figure 4-27 shows a block diagram of port 10.

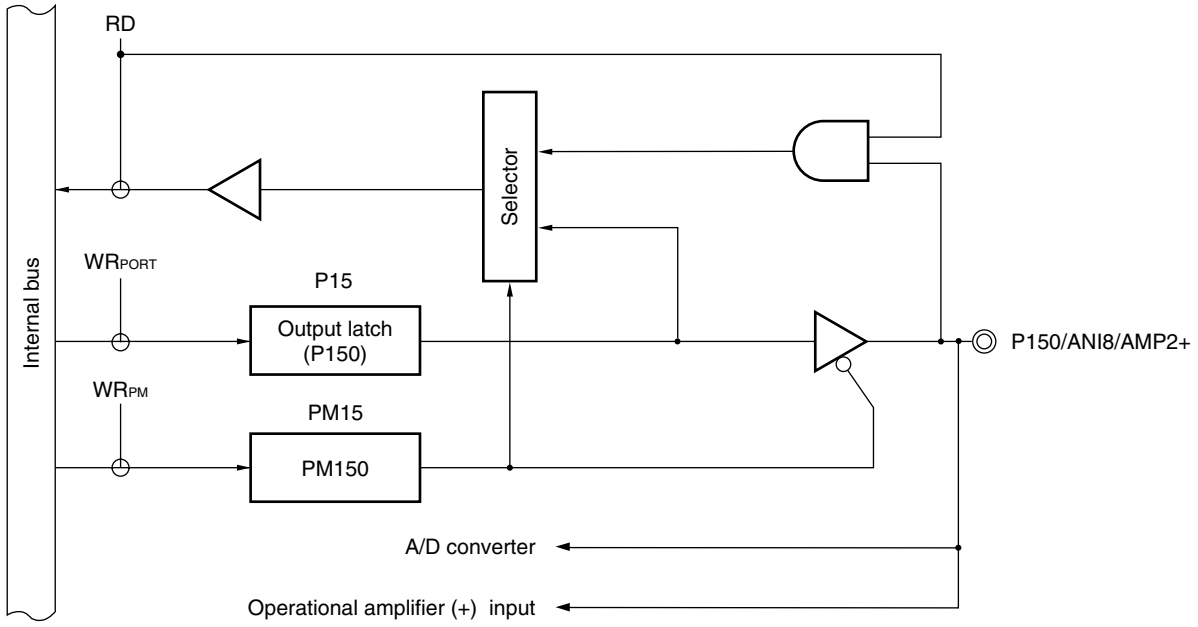
Figure 4-33. Block Diagram of P140 to P143



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
PFALL: Port function register
RD: Read signal
WR××: Write signal

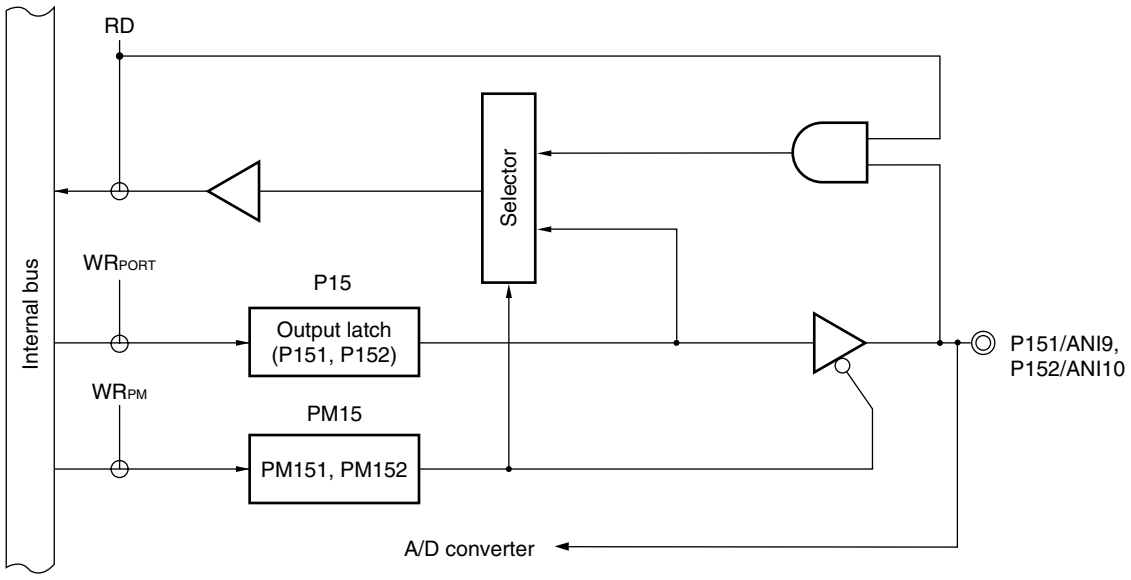
Remark 78K0R/LF3: P140/SEG19 to P143/SEG16
78K0R/LG3: P140/SEG23 to P143/SEG20
78K0R/LH3: P140/SEG37 to P143/SEG34

Figure 4-35. Block Diagram of P150



P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

Figure 4-36. Block Diagram of P151, P152



P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

4.6 Cautions on 1-bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0R/Lx3 Microcontrollers.

<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-52. Bit Manipulation Instruction (P10)

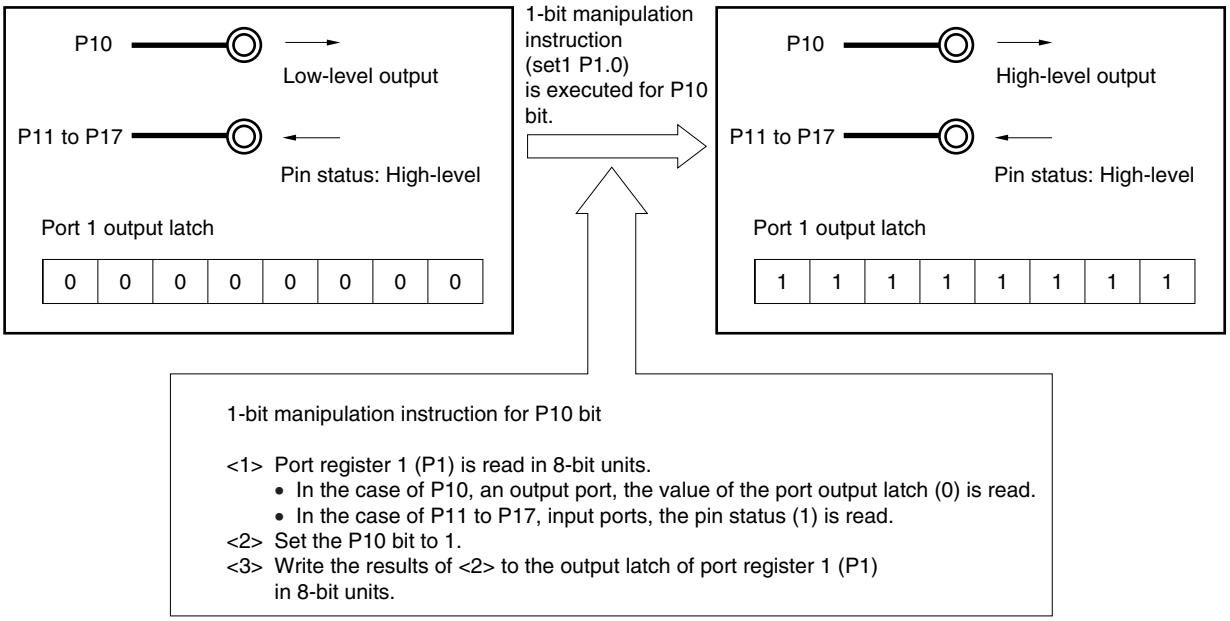


Figure 6-7. Format of Timer Mode Register mn (TMRmn) (3/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKS mn	0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

MD mn3	MD mn2	MD mn1	MD mn0	Operation mode of channel n	Count operation of TCR	Independent operation
0	0	0	1/0	Interval timer mode	Counting down	Possible
0	1	0	1/0	Capture mode	Counting up	Possible
0	1	1	0	Event counter mode	Counting down	Possible
1	0	0	1/0	One-count mode	Counting down	Impossible
1	1	0	0	Capture & one-count mode	Counting up	Possible
Other than above				Setting prohibited		
The operation of MDmn0 bits varies depending on each operation mode (see following table).						

Cautions 1. Be sure to clear bits 14, 13, 5, and 4 to "0".

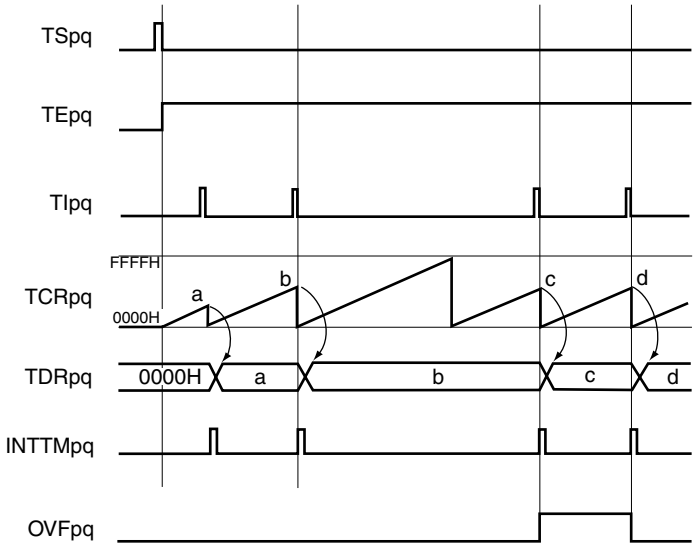
2. Channel 5 of timer array unit 0 and channels 0 to 3 of timer array unit 1 of the 78K0R/LF3 can be set only to the interval mode.

3. Channel 6 of timer array unit 0 of the 78K0R/LF3 can be set only to the interval mode and one-count mode (when using as master).

4. Channels 0 to 3 of timer array unit 1 of the 78K0R/LG3 can be set only to the interval mode.

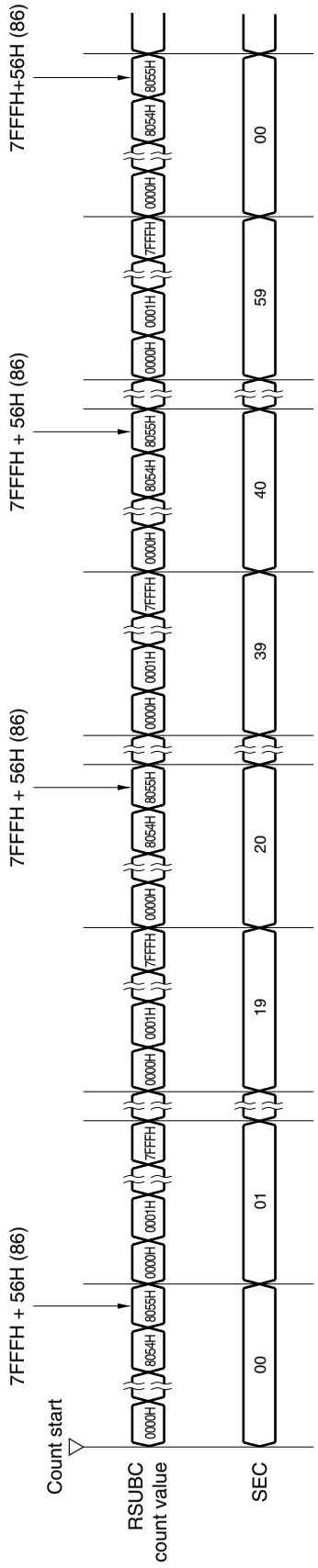
Remark mn: Unit number + Channel number
mn = 00 to 07, 10 to 13

Figure 6-50. Example of Basic Timing of Operation as Input Pulse Interval Measurement (MDpq0 = 0)



Remark pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: pq = 00 to 04, 07
78K0R/LG3: pq = 00 to 07
78K0R/LH3: pq = 00 to 07, 10 to 13

Figure 7-27. Operation When (DEV, F6, F5, F4, F3, F2, F1, F0) = (0, 0, 1, 0, 1, 1, 0, 0)



(10) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to A/D converter mode register (ADM), A/D converter mode register 1 (ADM1), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADM1, ADS, or ADPC. Using a timing other than the above may cause an incorrect conversion result to be read.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 10-30. Internal Equivalent Circuit of ANIn Pin

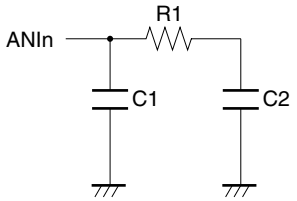


Table 10-8. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

R1	C1	C2
11.5 kΩ	8.0 pF	8.0 pF

Remarks 1. The resistance and capacitance values shown in Table 10-8 are not guaranteed values.

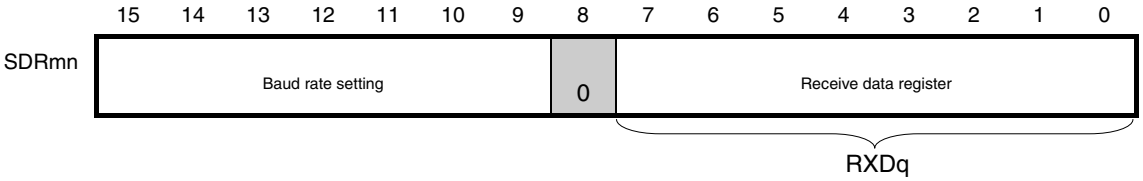
2. 78K0R/LF3: n = 0 to 6, 15, 78K0R/LG3, 78K0R/LH3: n = 0 to 10, 15

(12) Rewriting DACSWn during A/D conversion

Rewriting DACSWn (n = 0, 1) during A/D conversion is prohibited when both the positive reference voltage of A/D converter (AD_{REFP}) and the positive reference voltage of the D/A converter (DA_{REFP}) are the voltage reference output (V_{REFOUT}) (VRSEL = 1 and DAREF = 1). Rewrite it when conversion operation is stopped (ADCS = 0).

Figure 14-76. Example of Contents of Registers for UART Reception of UART (UART0, UART1, UART2, UART3) (2/2)

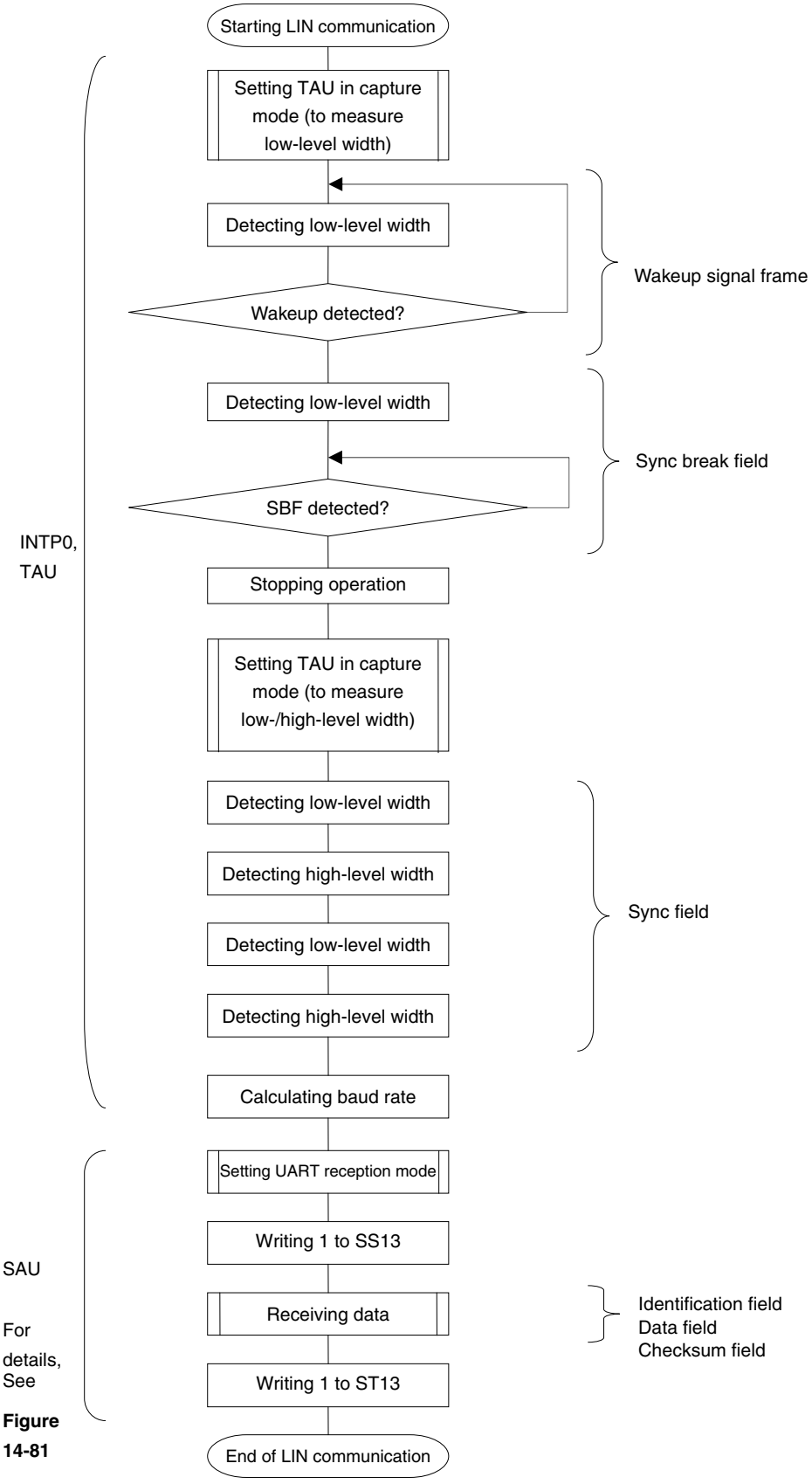
(g) Serial data register mn (SDRmn) (lower 8 bits: RXDq)



Caution For the UART reception, be sure to set SMRmr of channel r that is to be paired with channel n.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), r: Channel number (r = n − 1),
q: UART number (q = 0 to 3)
□: Setting is fixed in the UART reception mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 14-86. Flowchart of LIN Reception

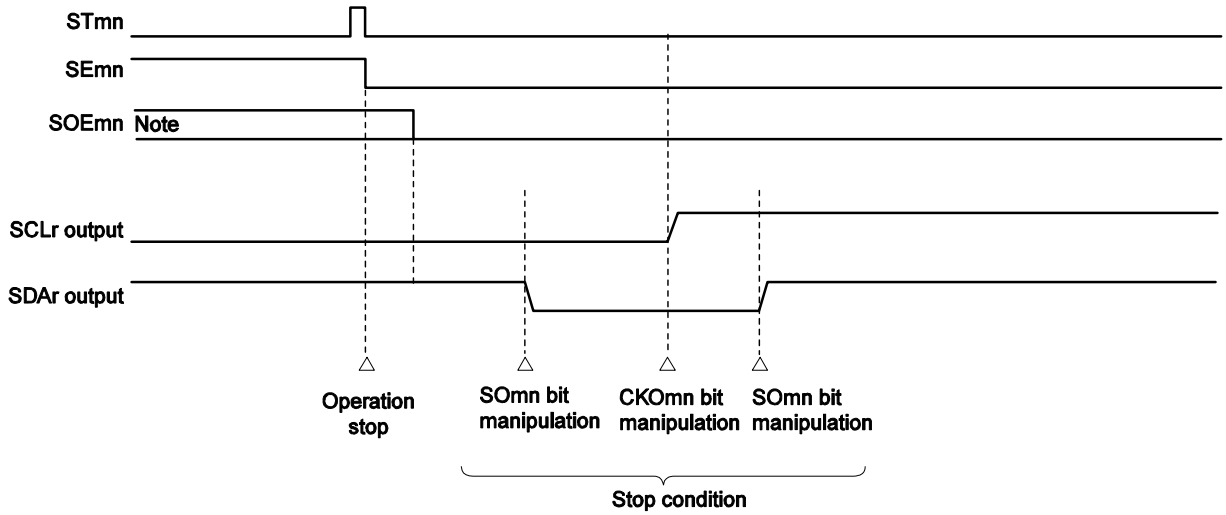


14.7.4 Stop condition generation

After all data are transmitted to or received from the target slave, a stop condition is generated and the bus is released.

(1) Processing flow

Figure 14-98. Timing Chart of Stop Condition Generation



Note During the receive operation, the SOEmn bit is set to 0 before receiving the last data.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)

15.5.8 Interrupt request (INTIICA) generation timing and wait control

The setting of bit 3 (WTIM) of IICA control register 0 (IICCTL0) determines the timing by which INTIICA is generated and the corresponding wait control, as shown in Table 15-2.

Table 15-2. INTIICA Generation Timing and Wait Control

WTIM	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Notes 1. The slave device's INTIICA signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to the slave address register (SVA).
At this point, $\overline{ACK}$ is generated regardless of the value set to IICCTL0's bit 2 (ACKE). For a slave device that has received an extension code, INTIICA occurs at the falling edge of the eighth clock.
However, if the address does not match after restart, INTIICA is generated at the falling edge of the 9th clock, but wait does not occur.

2. If the received address does not match the contents of the slave address register (SVA) and extension code is not received, neither INTIICA nor a wait occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- Writing data to IICA shift register (IICA)
- Setting bit 5 (WREL) of IICA control register 0 (IICCTL0) (canceling wait)
- Setting bit 1 (STT) of IICCTL0 register (generating start condition) Note
- Setting bit 0 (SPT) of IICCTL0 register (generating stop condition) Note

Note Master only.

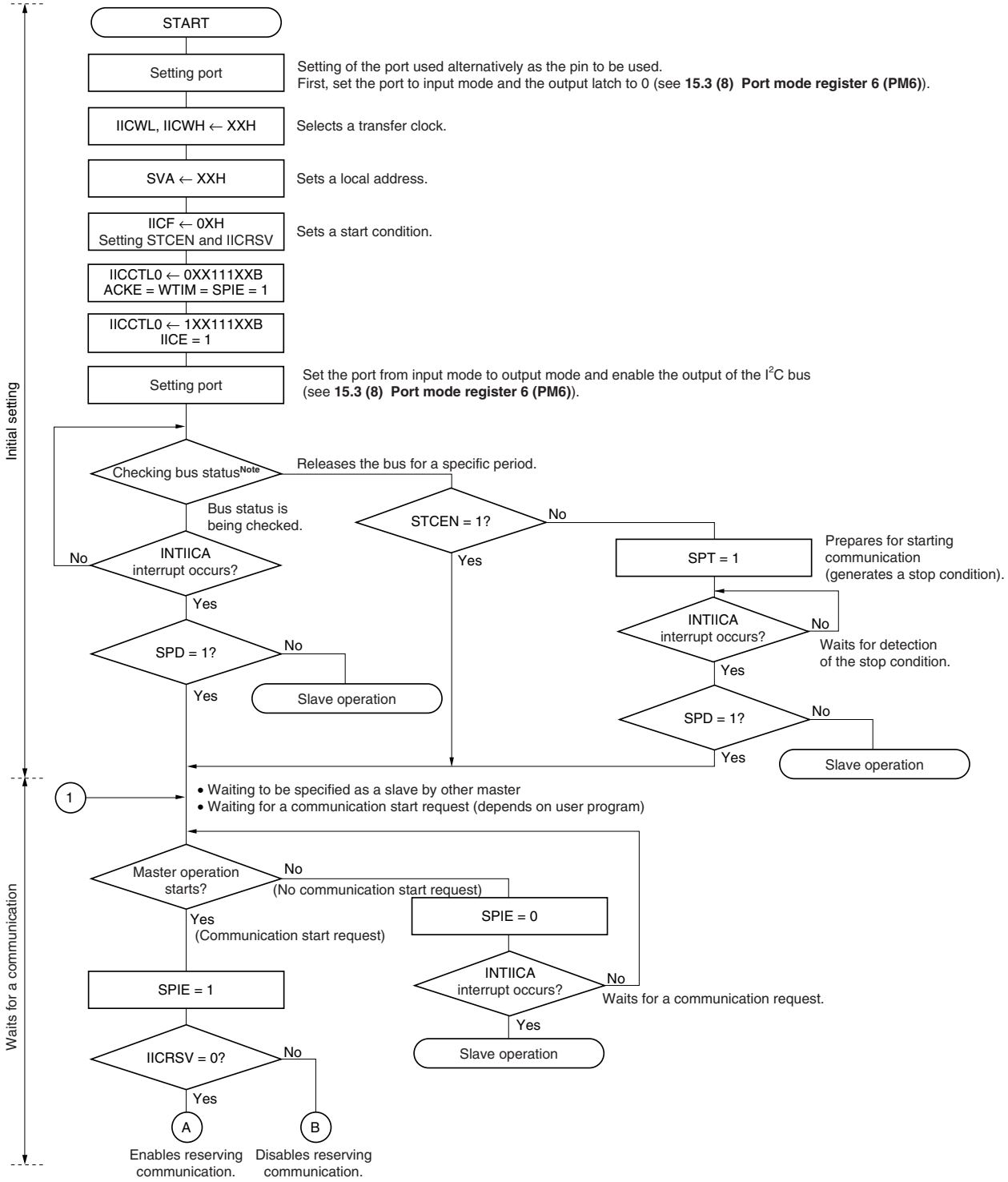
When an 8-clock wait has been selected (WTIM = 0), the presence/absence of $\overline{ACK}$ generation must be determined prior to wait cancellation.

(5) Stop condition detection

INTIICA is generated when a stop condition is detected (only when SPIE = 1).

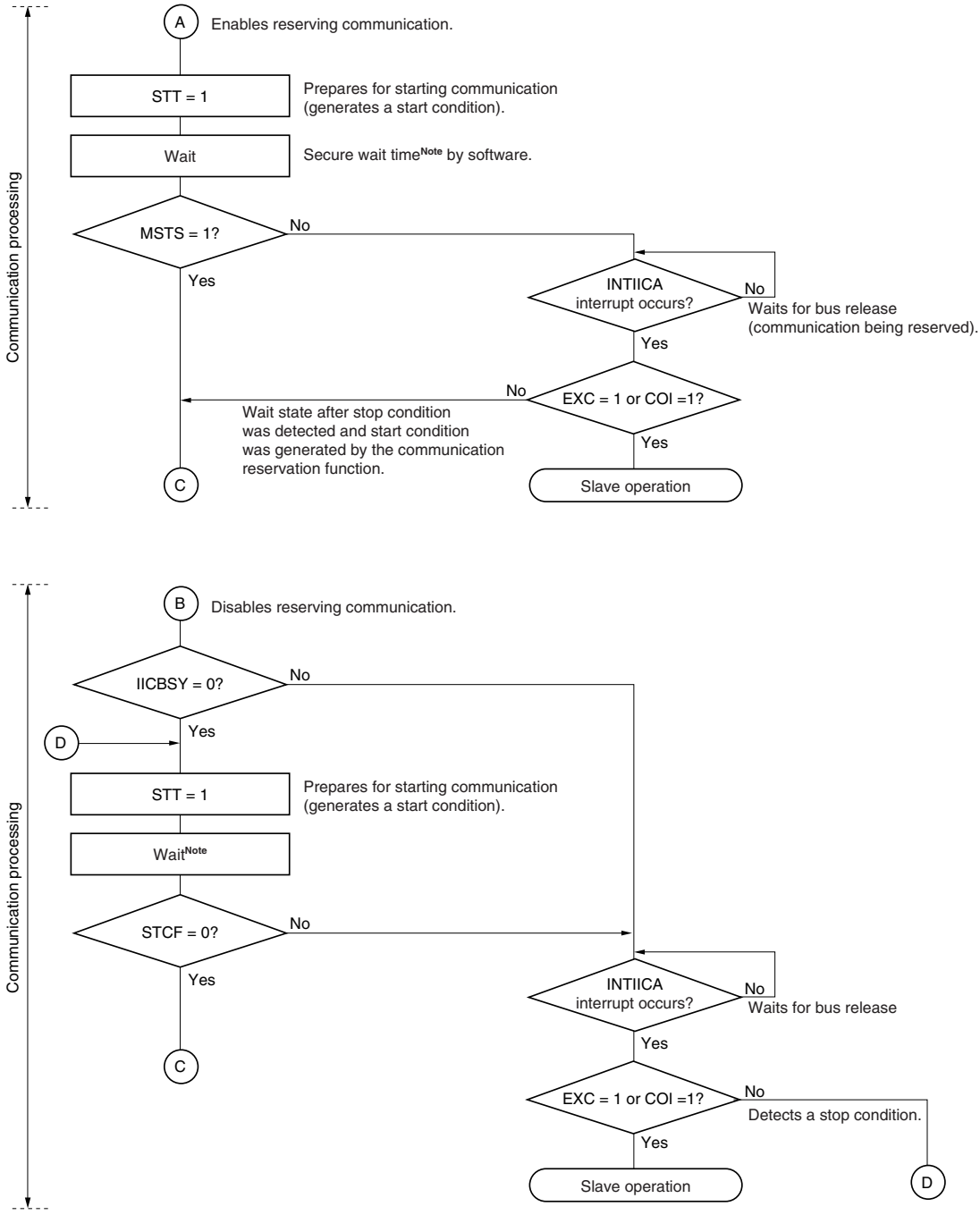
(2) Master operation in multi-master system

Figure 15-29. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD bit = 1, DAD bit = 1) for a specific period (for example, for a period of one frame). If the SDA0 pin is constantly at low level, decide whether to release the I^2C bus (SCL0 and SDA0 pins = high level) in conformance with the specifications of the product that is communicating.

Figure 15-29. Master Operation in Multi-Master System (2/3)

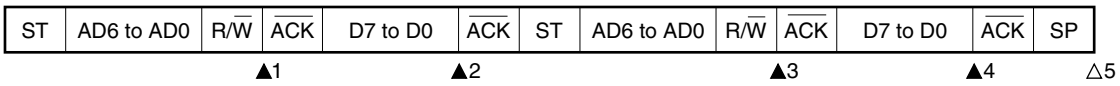


Note The wait time is calculated as follows.
(IICWL setting value + IICWH setting value + 4 clocks) / f_{CLK} + $t_F \times 2$

Remark IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
f_{CLK}: CPU/peripheral hardware clock frequency

(c) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

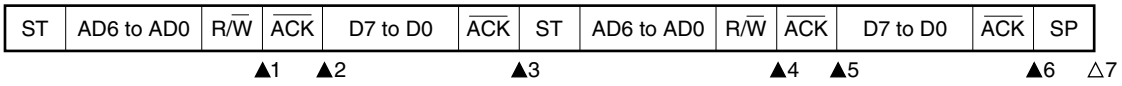
(i) When WTIM = 0 (after restart, extension code reception)



▲1: IICS = 0010×010B
▲2: IICS = 0010×000B
▲3: IICS = 0010×010B
▲4: IICS = 0010×000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, extension code reception)



▲1: IICS = 0010×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010××00B
▲4: IICS = 0010×010B
▲5: IICS = 0010×110B
▲6: IICS = 0010××00B
△7: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(7) Input switch control register (ISC)

The segment output pins to be used alternatively with the TI04, TI02, and RxD3 pins are internally connected with a Schmitt trigger buffer. To use these pins as segment outputs, input to the Schmitt trigger buffer must be disabled, in order to prevent through-currents from entering.

ISC is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ISC to 00H.

Remark The segment output pins to be used alternatively with the TI02, TI04, and RxD3 pins vary, depending on the product.

- 78K0R/LF3: TI04/SEG27/P53, TI02/SEG28/P52, RxD3/SEG30/P50
- 78K0R/LG3: TI04/SEG36/P53, TI02/SEG37/P52, RxD3/SEG39/P50
- 78K0R/LH3: TI04/SEG50/P53, TI02/SEG51/P52, RxD3/SEG53/P50

Figure 16-8. Format of Input Switch Control Register (ISC)

Address: FFF3CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	ISC4	ISC3	ISC2	ISC1	ISC0

ISC4	TI04/SEGxx/P53 schmitt trigger buffer control
0	Disables input
1	Enables input

ISC3	TI02/SEGxx/P52 schmitt trigger buffer control
0	Disables input
1	Enables input

ISC2	RxD3/SEGxx/P50 schmitt trigger buffer control
0	Disables input
1	Enables input

Caution Be sure to clear bits 5 to 7 to "0".

Remark Bits 0 and 1 of ISC are not used with the LCD controller driver.

To use the TI04/SEGxx/P53, TI02/SEGxx/P52, and RxD3/SEGxx/P50 pins, set the PF5L and ISCn (n = 2 to 4) bits as follows, according to the function to be used.

PF5L	ISCn	Pin function
0	0	Port output (default)
0	1	Port input, timer input, or serial data input
1	0	Segment output
1	1	Setting prohibited

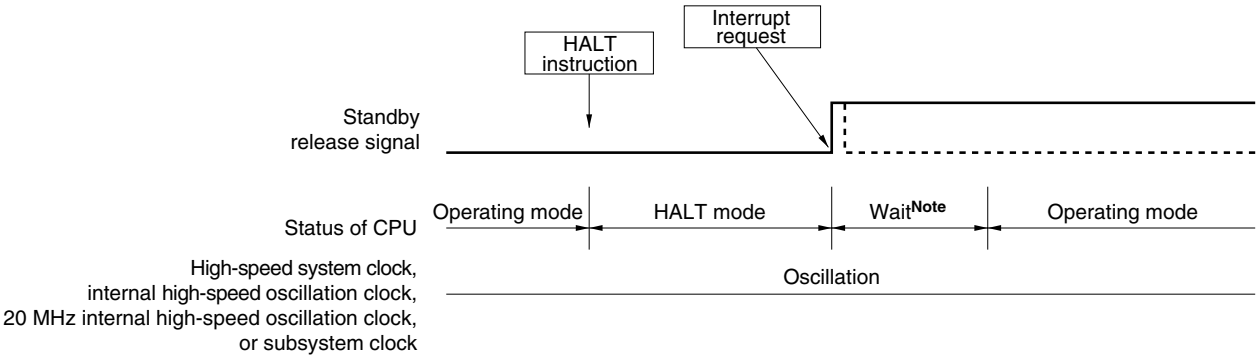
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 21-3. HALT Mode Release by Interrupt Request Generation



Note The wait time is as follows:

- When vectored interrupt servicing is carried out
  - When main system clock is used: 10 to 12 clocks
  - When subsystem clock is used: 8 to 10 clocks
- When vectored interrupt servicing is not carried out
  - When main system clock is used: 5 or 6 clocks
  - When subsystem clock is used: 3 or 4 clocks

Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

30.2 Operation List

Table 30-5. Operation List (1/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	r, #byte	2	1	–	r ← byte			
		saddr, #byte	3	1	–	(saddr) ← byte			
		sfr, #byte	3	1	–	sfr ← byte			
		!addr16, #byte	4	1	–	(addr16) ← byte			
		A, r Note 3	1	1	–	A ← r			
		r, A Note 3	1	1	–	r ← A			
		A, saddr	2	1	–	A ← (saddr)			
		saddr, A	2	1	–	(saddr) ← A			
		A, sfr	2	1	–	A ← sfr			
		sfr, A	2	1	–	sfr ← A			
		A, !addr16	3	1	4	A ← (addr16)			
		!addr16, A	3	1	–	(addr16) ← A			
		PSW, #byte	3	3	–	PSW ← byte	×	×	×
		A, PSW	2	1	–	A ← PSW			
		PSW, A	2	3	–	PSW ← A	×	×	×
		ES, #byte	2	1	–	ES ← byte			
		ES, saddr	3	1	–	ES ← (saddr)			
		A, ES	2	1	–	A ← ES			
		ES, A	2	1	–	ES ← A			
		CS, #byte	3	1	–	CS ← byte			
		A, CS	2	1	–	A ← CS			
		CS, A	2	1	–	CS ← A			
		A, [DE]	1	1	4	A ← (DE)			
		[DE], A	1	1	–	(DE) ← A			
		[DE + byte], #byte	3	1	–	(DE + byte) ← byte			
		A, [DE + byte]	2	1	4	A ← (DE + byte)			
		[DE + byte], A	2	1	–	(DE + byte) ← A			
		A, [HL]	1	1	4	A ← (HL)			
		[HL], A	1	1	–	(HL) ← A			
		[HL + byte], #byte	3	1	–	(HL + byte) ← byte			

Notes 1. When the internal RAM area or SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area.