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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1510agc-gad-ax

Pin Identification

AMP0- to AMP2- : Amplifier Input Minus
AMP0+ to AMP2+ : Amplifier Input Plus
AMP0O to AMP2O : Amplifier Output
ANI0 to ANI10, ANI15 : Analog Input (ADC)
ANO0, ADO1 : Analog Output (DAC)
<R> AV_{REF} : Analog Reference Voltage
AV_{REFM} : Analog Reference Voltage Minus
AV_{REFP} : Analog Reference Voltage Plus
AV_{SS} : Analog Ground
<R> AV_{DD} : Analog Power Supply
AV_{DD0} : Analog Power Supply (ADC/VREF/OPAMP)
AV_{DD1} : Analog Power Supply (DAC)
CAPH, CAPL : Capacitor for LCD
COM0 to COM7 : LCD Common Output
<R> EV_{DD}, EV_{DD1}: Power Supply for Port
EV_{SS} : GND for Port
EXCLK : External Clock Input (Main system clock)
EXLVI : External Potential Input for Low Voltage Detector
FLMD0 : Flash Programming Mode
INTP0 to INTP11 : External Interrupt Input
KR0 to KR7 : Key Return
P00 to P02 : Port 0
P10 to P17 : Port 1
P20 to P27 : Port 2
P30 to P34 : Port 3
P40, P41 : Port 4
P50 to P57 : Port 5
P60, P61 : Port 6
P70 to P77 : Port 7
P80 to P87 : Port 8
P90 to P97 : Port 9
P100 to P102 : Port 10
P110, P111 : Port 11
P120 to P124 : Port 12
P130 : Port 13
P140 to P147 : Port 14
P150 to P152, P157 : Port 15
PCLBUZ0, PCLBUZ1 : Programmable Clock Output /Buzzer Output
REGC : Regulator Capacitance
$\overline{RESET}$: Reset
RTC1HZ : Real-time Counter Correction Clock (1Hz) Output
RTCCL : Real-time Counter Clock (32 kHz Original Oscillation) Output
RTCDIV : Real-time Counter Clock (32 kHz Divided Frequency) Output
RxD0 to RxD3 : Receive Data
$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$: Serial Clock Input/Output
SCL0, SCL10, SCL20 : Serial Clock Input/Output
SDA0, SDA10, SDA20 : Serial Data Input/Output
SEG0 to SEG53 : LCD Segment Output
SI00, SI01, SI10, SI20 : Serial Data Input
SO00, SO01, SO10, SO20 : Serial Data Output
TI00 to TI07, TI10 to TI13 : Timer Input
TO00 to TO07, TO10 to TO13 : Timer Output
TOOL0 : Data Input/Output for Tool
TOOL1 : Clock Output for Tool
TxD0 to TxD3 : Transmit Data
V_{DD} : Power Supply
V_{LC0} to V_{LC3} : LCD Power Supply
V_{REFOUT} : Voltage Reference Output
V_{SS} : Ground
X1, X2 : Crystal Oscillator (Main system clock)
XT1, XT2 : Crystal Oscillator (Subsystem Clock)

2.2.11 P100 to P102

P100 to P102 function as an I/O port. This port can also be used for segment output of LCD controller/driver.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P100/SEGxx	√ (xx = 11)	√ (xx = 15)	√ (xx = 29)
P101/SEGxx	–	–	√ (xx = 28)
P102/SEGxx	–	–	√ (xx = 27)

The following operation modes can be specified in 1-bit units.

(1) Port mode

P100 to P102 function as an I/O port. P100 to P102 can be set to input or output port in 1-bit units using port mode register 10 (PM10). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 10 (PU10).

(2) Control mode

P100 to P102 function as segment output of LCD controller/driver (SEGxx).

2.2.12 P110, P111

P110 and P111 function as an I/O port. This port can also be used for D/A converter analog output.

<R>

	μPD78F150xA			μPD78F151xA		
	78K0R/LF3 (80 pins)	78K0R/LG3 (100 pins)	78K0R/LH3 (128 pins)	78K0R/LF3 (80 pins)	78K0R/LG3 (100 pins)	78K0R/LH3 (128 pins)
P110/ANO0	√			P110		
P111/ANO1	√			P111		

The following operation modes can be specified in 1-bit units.

(1) Port mode

P110 and P111 function as an I/O port. P110 and P111 can be set to input or output port in 1-bit units using port mode register 11 (PM11).

(2) Control mode

P110 and P111 function as D/A converter analog output (ANO0, ANO1).

Caution When using at least one port of P110/ANO0 and P111/ANO1 as a digital port, set AV_{DD1} to the same potential as EV_{DD} or V_{DD}.

Table 4-11. Settings of Port Mode Register and Output Latch When Using Alternate Function (5/5)

LF3	LG3	LH3	Pin Name	Alternate Function		PFALL	ISC	PM××	P××
				Function Name	I/O	(PFxxx)	(ISCx)		
√	–	–	P50[Note]	SEG30	Output	PF5L=1	ISC2 = 0	×	×
			P51[Note]	SEG29	Output	PF5L=1	–	×	×
			P52[Note]	SEG28	Output	PF5L=1	ISC3 = 0	×	×
			P53[Note]	SEG27	Output	PF5L=1	ISC4 = 0	×	×
			P54 to 57	SEG26 to SEG23	Output	PF5H=1	–	×	×
			P90 to 92	SEG22 to SEG20	Output	PF9L=1	–	×	×
			P140 to 143	SEG19 to SEG16	Output	PF14L=1	–	×	×
			P144 to 147	SEG15 to SEG12	Output	PF14H=1	–	×	×
			P100	SEG11	Output	PF10=1	–	×	×
–	√	–	P50[Note]	SEG39	Output	PF5L=1	ISC2 = 0	×	×
			P51[Note]	SEG38	Output	PF5L=1	–	×	×
			P52[Note]	SEG37	Output	PF5L=1	ISC3 = 0	×	×
			P53[Note]	SEG36	Output	PF5L=1	ISC4 = 0	×	×
			P54 to 57	SEG35 to SEG32	Output	PF5H=1	–	×	×
			P90 to 93	SEG31 to SEG28	Output	PF9L=1	–	×	×
			P94 to 97	SEG27 to SEG24	Output	PF9H=1	–	×	×
			P140 to 143	SEG23 to SEG20	Output	PF14L=1	–	×	×
			P144 to 147	SEG19 to SEG16	Output	PF14H=1	–	×	×
			P100	SEG15	Output	PF10=1	–	×	×
–	–	√	P50[Note]	SEG53	Output	PF5L=1	ISC2 = 0	×	×
			P51[Note]	SEG52	Output	PF5L=1	–	×	×
			P52[Note]	SEG51	Output	PF5L=1	ISC3 = 0	×	×
			P53[Note]	SEG50	Output	PF5L=1	ISC4 = 0	×	×
			P54 to 57	SEG49 to SEG46	Output	PF5H=1	–	×	×
			P90 to 93	SEG45 to SEG42	Output	PF9L=1	–	×	×
			P94 to 97	SEG41 to SEG38	Output	PF9H=1	–	×	×
			P140 to 143	SEG37 to SEG34	Output	PF14L=1	–	×	×
			P144 to 147	SEG33 to SEG30	Output	PF14H=1	–	×	×
			P100 to 102	SEG29 to SEG27	Output	PF10=1	–	×	×

Note For alternate function other than the segment output (SEGxx), refer to **Table 4-11 Settings of Port Mode Register and Output Latch When Using Alternate Function (3/5).**

Remark ×: don't care
–: Not applicable
PFALL: Port function register
ISC: Input switch control register
PM××: Port mode register
P××: Port output latch

Remarks 1. f_{IH}: Internal high-speed oscillation clock frequency
f_{IH20}: 20 MHz Internal high-speed oscillation clock frequency
f_{MX}: High-speed system clock frequency
f_{SUB} Subsystem clock frequency
2. ×: don't care

Cautions 1. The clock set by CSS, MCM0, SDIV, and MDIV2 to MDIV0 is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time counter, timer array unit (when $f_{SUB}/2$, $f_{SUB}/4$, the valid edge of TI0mn input, or the valid edge of INTRTCI is selected as the count clock), clock output/buzzer output, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral operating hardware clock.
2. If the peripheral hardware clock is used as the subsystem clock, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 31 ELECTRICAL SPECIFICATIONS.

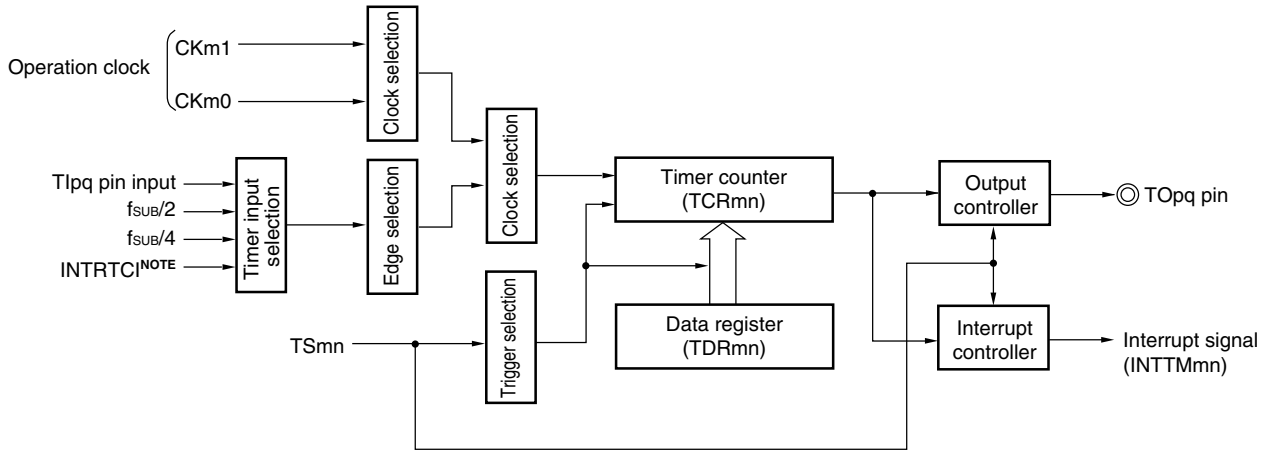
The fastest instruction can be executed in 1 clock of the CPU clock in the 78K0R/Lx3 microcontrollers. Therefore, the relationship between the CPU clock (f_{CLK}) and the minimum instruction execution time is as shown in Table 5-3.

Table 5-3. Relationship Between CPU Clock and Minimum Instruction Execution Time

CPU Clock (Value set by the SDIV, and MDIV2 to MDIV0 bits)	Minimum Instruction Execution Time: $1/f_{CLK}$				
	Main System Clock (CSS = 0)				Subsystem Clock (CSS = 1)
	High-Speed System Clock (MCM0 = 1)		Internal High-Speed Oscillation Clock (MCM0 = 0)		
	At 10 MHz Operation	At 20 MHz Operation	At 8 MHz (TYP.) Operation	At 20 MHz (TYP.) Operation	At 32.768 kHz Operation
f_{MAIN}	0.1 μs	0.05 μs	0.125 μs (TYP.)	0.05 μs (TYP.)	–
$f_{MAIN}/2$	0.2 μs	0.1 μs	0.25 μs (TYP.) (default)	0.1 μs (TYP.)	–
$f_{MAIN}/2^2$	0.4 μs	0.2 μs	0.5 μs (TYP.)	0.2 μs (TYP.)	–
$f_{MAIN}/2^3$	0.8 μs	0.4 μs	1.0 μs (TYP.)	0.4 μs (TYP.)	–
$f_{MAIN}/2^4$	1.6 μs	0.8 μs	2.0 μs (TYP.)	0.8 μs (TYP.)	–
$f_{MAIN}/2^5$	3.2 μs	1.6 μs	4.0 μs (TYP.)	1.6 μs (TYP.)	–
f_{SUB}	–		–		30.5 μs
$f_{SUB}/2$	–		–		61 μs

Remark f_{MAIN}: Main system clock frequency (f_{IH}, f_{IH20}, or f_{MX})
f_{SUB}: Subsystem clock frequency

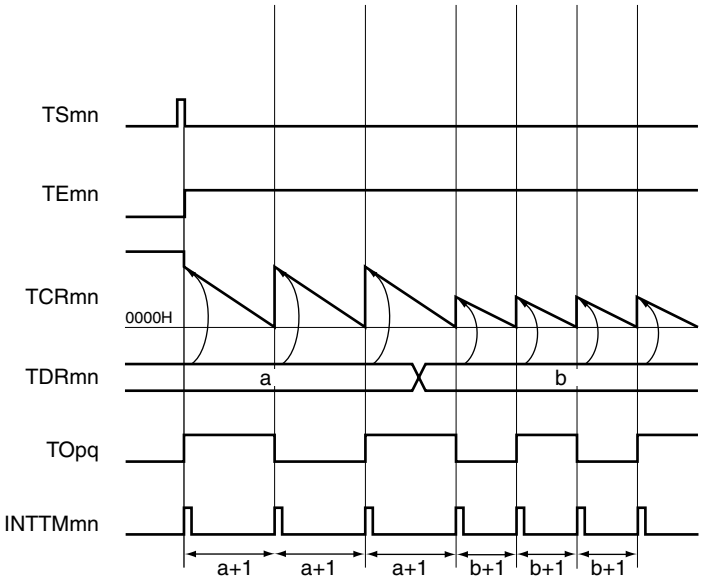
Figure 6-37. Block Diagram of Operation as Interval Timer/Square Wave Output



Note Channels 0 and 4 of timer array unit 0 only

Remark mn: Unit number + Channel number, pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 04, 07
78K0R/LG3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 07
78K0R/LH3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 07, 10 to 13

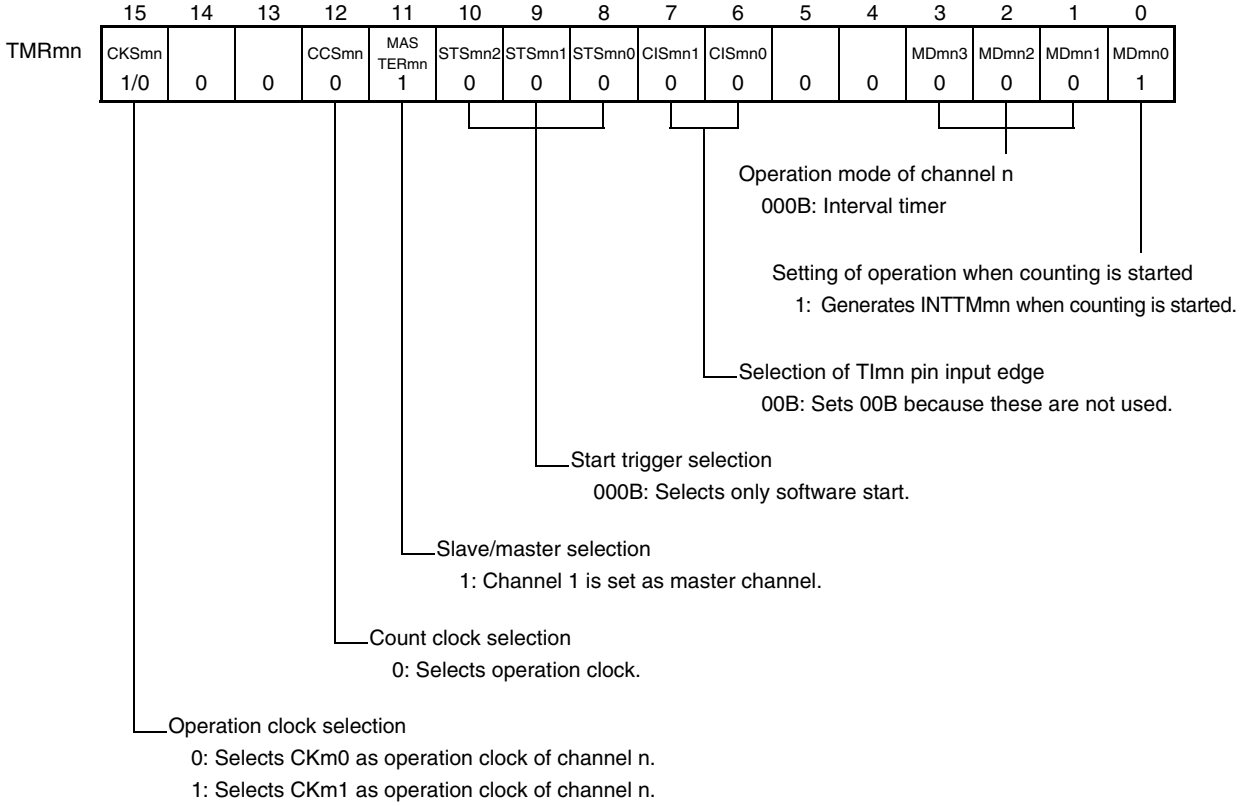
Figure 6-38. Example of Basic Timing of Operation as Interval Timer/Square Wave Output (MDmn0 = 1)



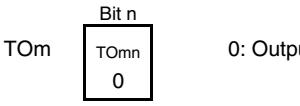
Remark mn: Unit number + Channel number, pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: mn = 00 to 07, 10 to 13, pq = 00 to 04, 07
78K0R/LG3: mn = 00 to 07, 10 to 13, pq = 00 to 07
78K0R/LH3: mn = 00 to 07, 10 to 13, pq = 00 to 07, 10 to 13

Figure 6-69. Example of Set Contents of Registers When Multiple PWM Output Function (Master Channel) Is Used

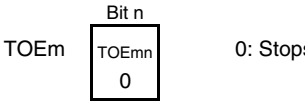
(a) Timer mode register mn (TMRmn)



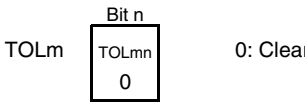
(b) Timer output register m (TOm)



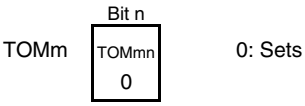
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)



Remarks 1. 78K0R/LF3:
- m = 0, n = 0, 2, TO00 to TO04, TO07, TI00 to TI04, and TI07 pins

2. 78K0R/LG3:
- m = 0, n = 0, 2, 4, TO00 to TO07, and TI00 to TI07 pins

3. 78K0R/LH3:
- m = 0, n = 0, 2, 4, TO00 to TO07, and TI00 to TI07 pins
- m = 1, n = 0, TO10 to TO13 , and TI10 to TI13 pins

7.4.7 512 Hz or 16.384 kHz output of real-time counter

Figure 7-26. 512 Hz or 16.384 kHz Output Setting Procedure

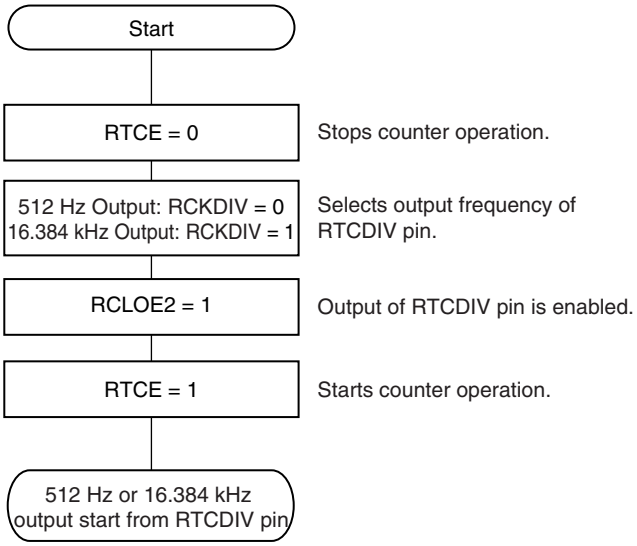
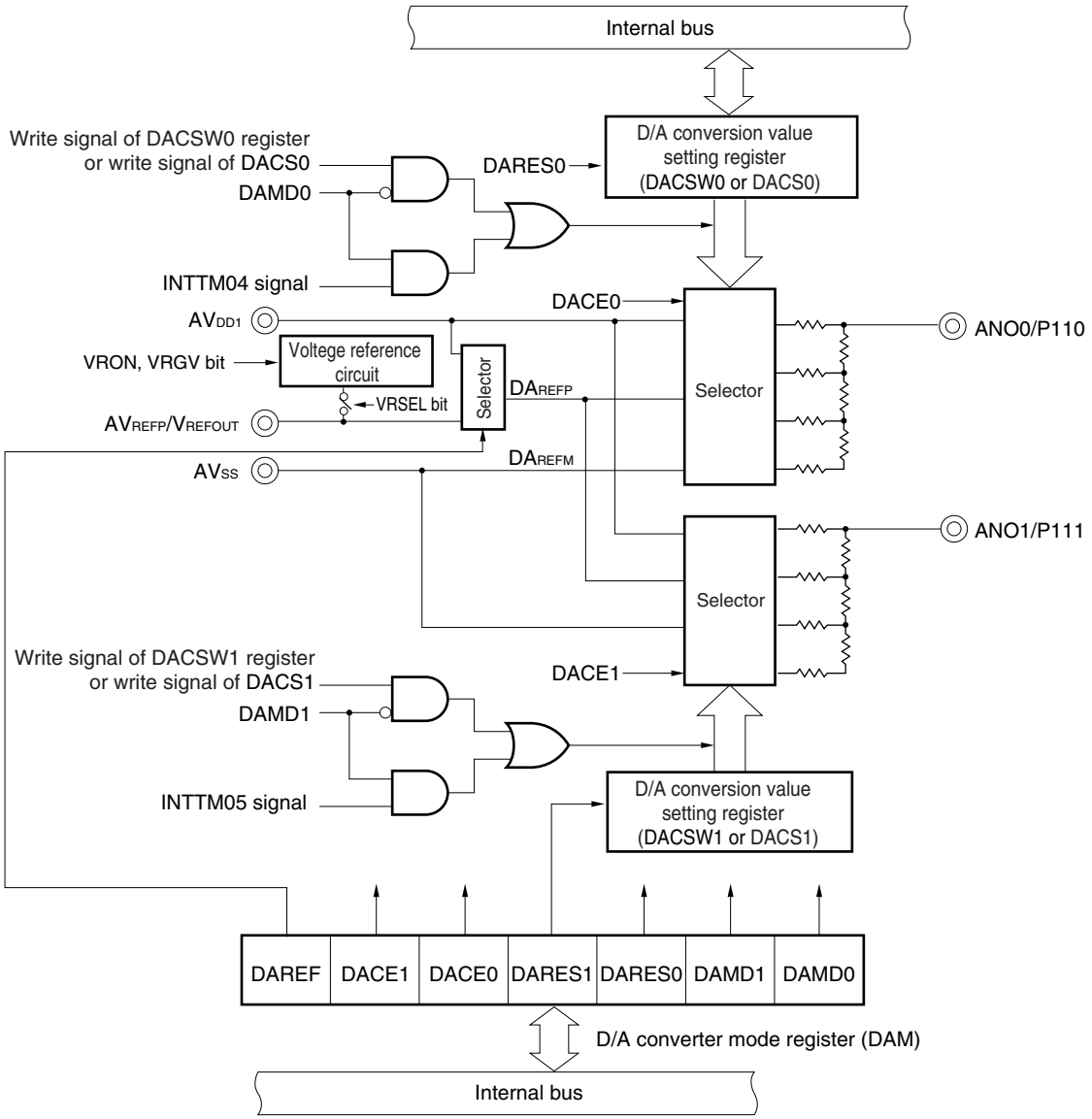


Figure 11-1. Block Diagram of D/A Converter



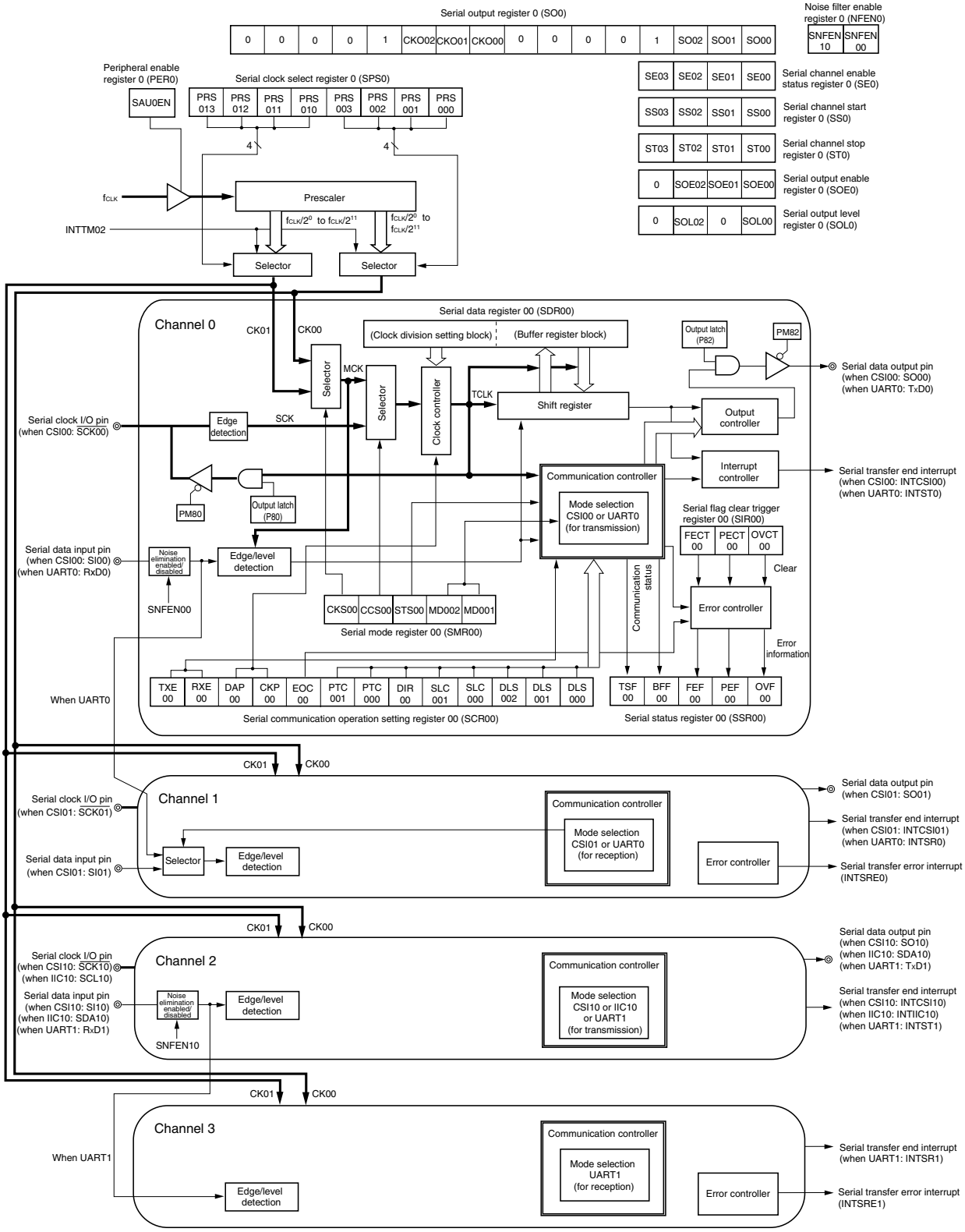
Remarks 1. INTTM04 and INTTM05 are timer trigger signals (interrupt signals from timer channels 5 and 6) that are used in the real-time output mode.

2. Channels 0 and 1 of the D/A converter share the AV_{REF1} pin and the AV_{REFP}/V_{REFOUT} pin.

3. Channels 0 and 1 of the D/A converter share the AV_{SS} pin. The AV_{SS} pin is also shared with an A/D converter, an operational amplifier, and a voltage reference.

Figure 14-1 shows the block diagram of serial array unit 0.

Figure 14-1. Block Diagram of Serial Array Unit 0

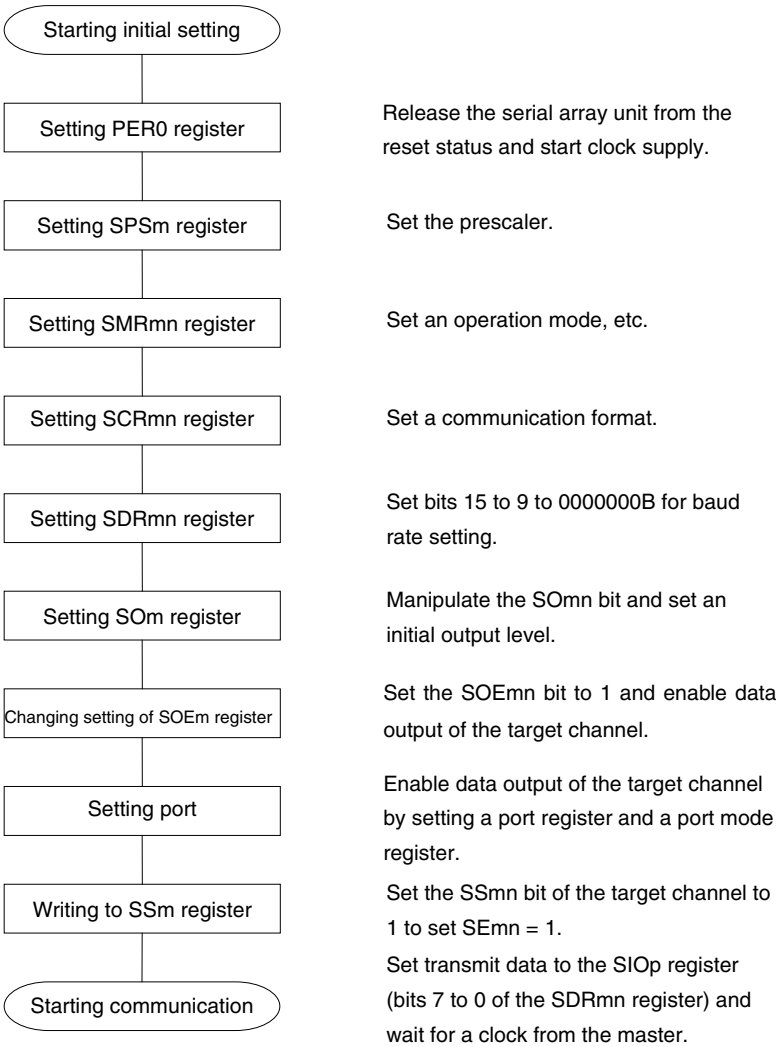


Remarks 1. For 78K0R/LF3, the channels 0 and 1 are not mounted.

2. For 78K0R/LG3, CSI01 is not mounted.

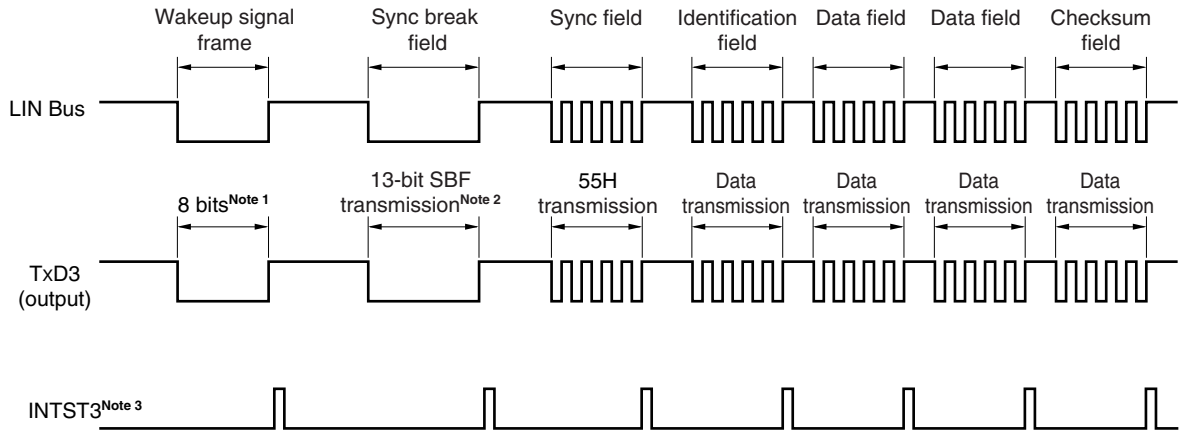
(2) Operation procedure

Figure 14-47. Initial Setting Procedure for Slave Transmission



Caution After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Figure 14-82. Transmission Operation of LIN



Notes 1. The baud rate is set so as to satisfy the standard of the wakeup signal and data of 00H is transmitted.

2. A sync break field is defined to have a width of 13 bits and output a low level. Where the baud rate for main transfer is N [bps], therefore, the baud rate of the sync break field is calculated as follows.

(Baud rate of sync break field) = 9/13 × N

By transmitting data of 00H at this baud rate, a sync break field is generated.

3. INTST3 is output upon completion of transmission. INTST3 is also output when SBF transmission is executed.

Remark The interval between fields is controlled by software.

Figure 15-6. Format of IICA Control Register 0 (IICCTL0) (3/4)

STT[Note]	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in standby state, when IICBSY = 0): If this bit is set (1), a start condition is generated (startup as the master). When a third party is communicating: • When communication reservation function is enabled (IICRSV = 0) Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released. • When communication reservation function is disabled (IICRSV = 1) Even if this bit is set (1), the STT bit is cleared and the STT clear flag (STCF) is set (1). No start condition is generated. In the wait state (when master device): Generates a restart condition after releasing the wait.

Cautions concerning set timing
- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when ACKE has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A start condition cannot be generated normally during the acknowledge period. Set to 1 during the wait period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as SPT.
- Setting STT to 1 and then setting it again before it is cleared to 0 is prohibited.

Condition for clearing (STT = 0)	Condition for setting (STT = 1)
• Cleared by setting STT to 1 while communication reservation is prohibited. • Cleared by loss in arbitration • Cleared after start condition is generated by master device • Cleared by LREL = 1 (exit from communications) • When IICE = 0 (operation stop) • Reset	• Set by instruction

Note The signal of this bit is invalid while IICE0 is 0.

Remarks 1. Bit 1 (STT) becomes 0 when it is read after data setting.

2. IICRSV: Bit 0 of IIC flag register (IICF)
STCF: Bit 7 of IIC flag register (IICF)

15.4.2 Setting transfer clock by using IICWL and IICWH registers

(1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{CLK}}{IICWL + IICWH + f_{CLK}(t_R + t_F)}$$

At this time, the optimal setting values of IICWL and IICWH are as follows.
(The fractional parts of all setting values are rounded up.)

- When the fast mode

$$IICWL = \frac{0.52}{\text{Transfer clock}} \times f_{CLK}$$
$$IICWH = \left(\frac{0.48}{\text{Transfer clock}} - t_R - t_F\right) \times f_{CLK}$$

- When the standard mode

$$IICWL = \frac{0.47}{\text{Transfer clock}} \times f_{CLK}$$
$$IICWH = \left(\frac{0.53}{\text{Transfer clock}} - t_R - t_F\right) \times f_{CLK}$$

(2) Setting IICWL and IICWH on slave side

(The fractional parts of all setting values are truncated.)

- When the fast mode

$$IICWL = 1.3\ \mu s \times f_{CLK}$$
$$IICWH = (1.2\ \mu s - t_R - t_F) \times f_{CLK}$$

- When the standard mode

$$IICWL = 4.7\ \mu s \times f_{CLK}$$
$$IICWH = (5.3\ \mu s - t_R - t_F) \times f_{CLK}$$

Caution Note the minimum f_{CLK} operation frequency when setting the transfer clock. The minimum f_{CLK} operation frequency for serial interface IICA is determined according to the mode.

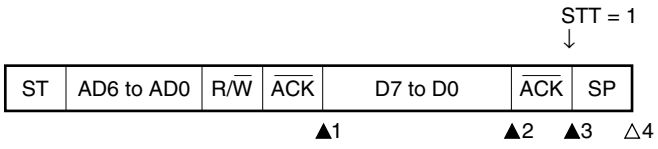
Fast mode: f_{CLK} = 3.5 MHz (MIN.)
Standard mode: f_{CLK} = 1 MHz (MIN.)

Remarks 1. Calculate the rise time (t_R) and fall time (t_F) of the SDA0 and SCL0 signals separately, because they differ depending on the pull-up resistance and wire load.

2. IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
t_R: SDA0 and SCL0 signal rising times
f_{CLK}: CPU/peripheral hardware clock frequency

(g) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

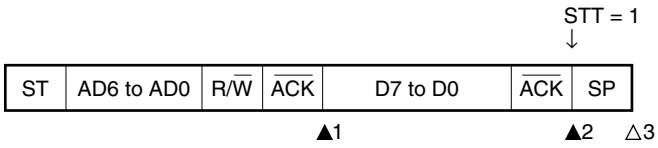
(i) When WTIM = 0



▲1: IICS = 1000×110B
▲2: IICS = 1000×000B (Sets WTIM to 1)
▲3: IICS = 1000××00B (Sets STT to 1)
△4: IICS = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1



▲1: IICS = 1000×110B
▲2: IICS = 1000××00B (Sets STT to 1)
△3: IICS = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

Figure 16-16. Example of Connecting Static LCD Panel

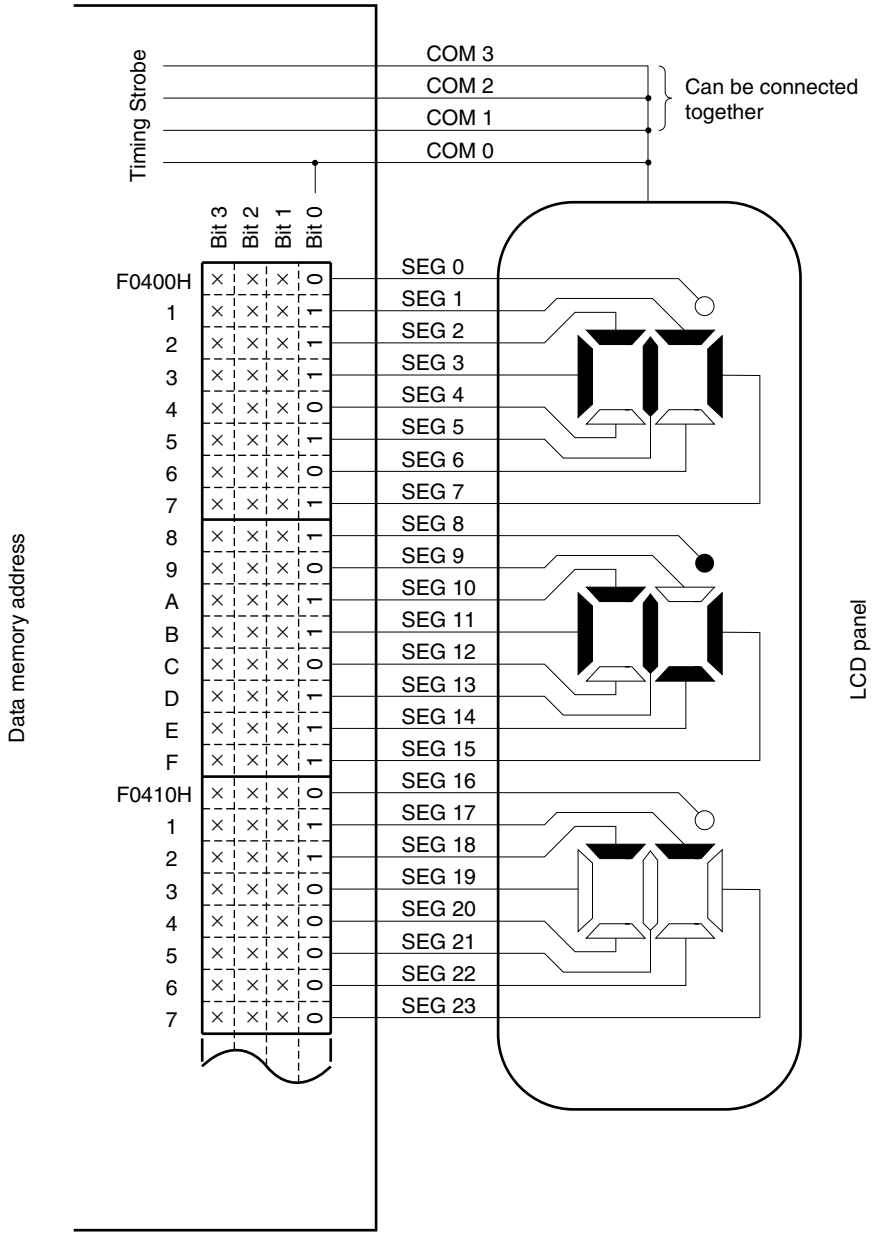
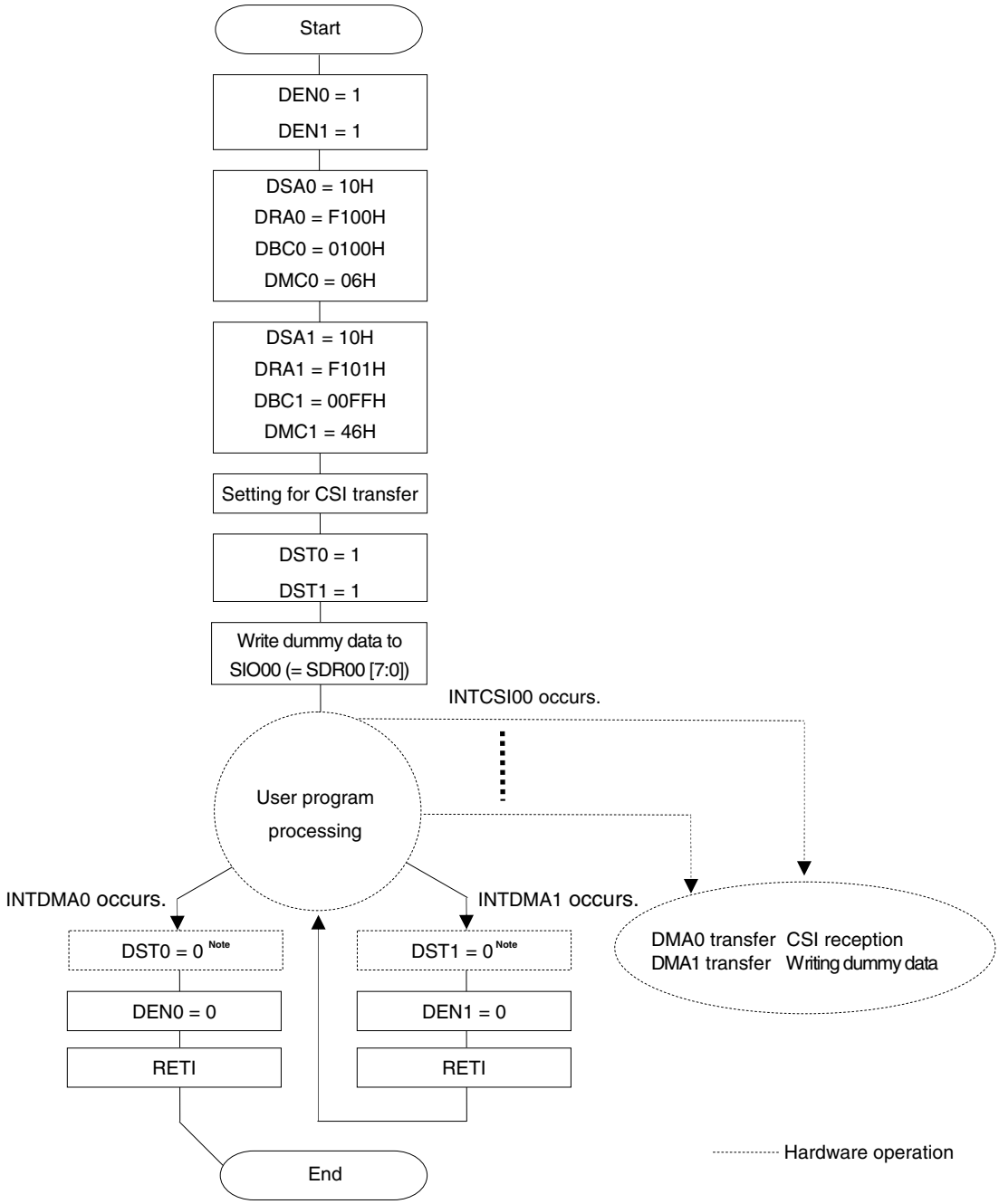


Figure 18-8. Example of Setting of Consecutively Capturing A/D Conversion Results



Note The DSTn flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DENn flag is enabled only when DSTn = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMAn (INTDMAn), set DSTn to 0 and then DENn to 0 (for details, refer to **18.5.7 Forcible termination by software**).

Because no CSI interrupt is generated when reception starts during CSI master reception, dummy data is written using software in this example.

The received data is automatically transferred from the first byte (In successive reception mode, the data that is to be received when the first buffer empty interrupt occurs is invalid because the valid data has not been received.).

A DMA interrupt (INTDMA1) occurs when the last dummy data has been writing to the data register. A DMA interrupt (INTDMA0) occurs when the last received data has been read from the data register. To restart the DMA transfer, the CSI transfer must be completed.

(2) When detecting level of input voltage from external input pin (EXLVI)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 1 (detects level of input voltage from external input pin (EXLVI)).
    Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <4> Use software to wait for the following periods of time (Total 210 μs).
    - Operation stabilization time (10 μs (MAX.))
    - Minimum pulse width (200 μs (MIN.))
  - <5> Confirm that "input voltage from external input pin (EXLVI) $\geq$ detection voltage (V_{EXLVI} = 1.21 V (TYP.))" when detecting the falling edge of EXLVI, or "input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI} = 1.21 V (TYP.))" when detecting the rising edge of EXLVI, at bit 0 (LVIF) of LVIM.
  - <6> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <7> Release the interrupt mask flag of LVI (LVIMK).
  - <8> Execute the EI instruction (when vector interrupts are used).

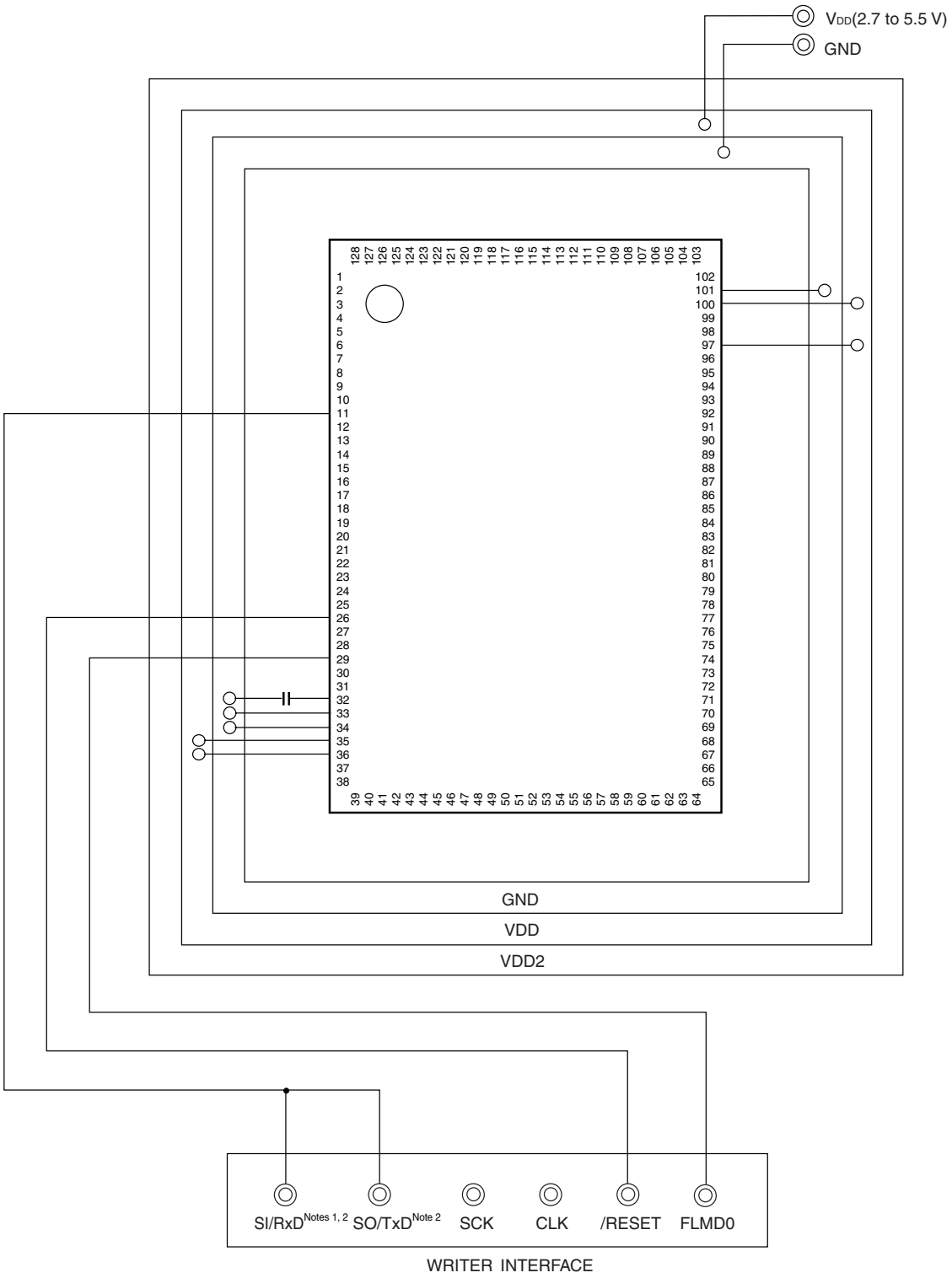
  Figure 24-10 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <7> above.

  Caution Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

- When stopping operation
  Be sure to clear (0) LVION by using a 1-bit memory manipulation instruction.

Examples of the recommended connection (μPD78F1508A) when using the adapter for flash memory writing are shown below.

Figure 27-3. Example of Wiring Adapter for Flash Memory Writing (μPD78F1508A)

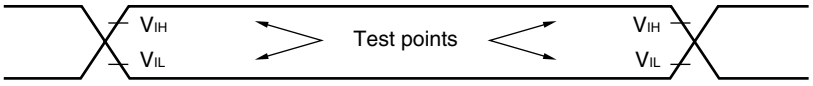


Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

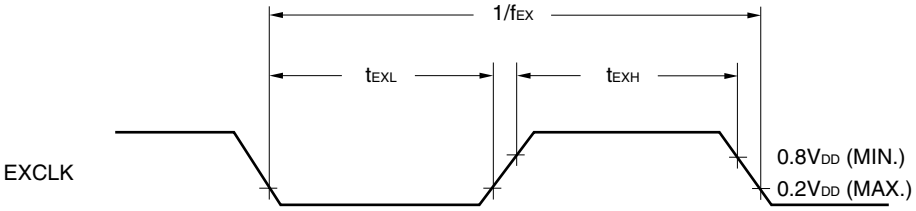
2. Connect SI/RxD or SO/TxD when using QB-MINI2.

(1) Basic operation (6/6)

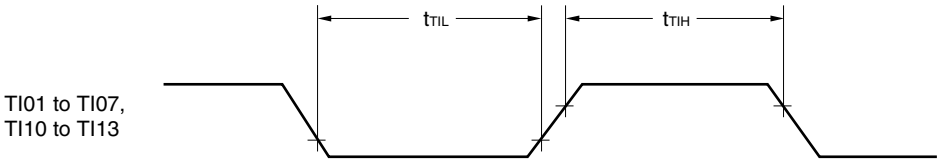
AC Timing Test Points



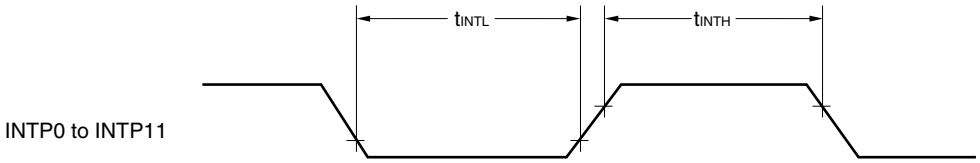
External Main System Clock Timing



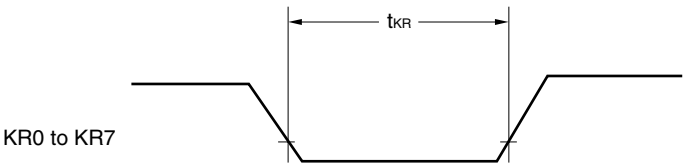
TI Timing



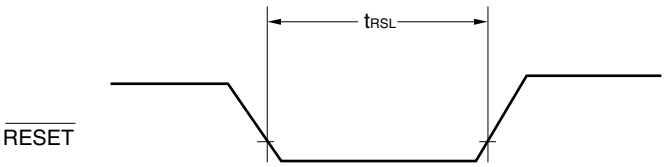
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(3/3)

Page	Description	Classification
CHAPTER 11 D/A CONVERTER (μPD78F150xA only)		
p.418	Addition of (μPD78F150xA only) to chapter title	(d)
CHAPTER 12 OPERATIONAL AMPLIFIER (μPD78F150xA only)		
p.425	Addition of (μPD78F150xA only) to chapter title	(d)
CHAPTER 13 VOLTAGE REFERENCE (μPD78F150xA only)		
p.434	Addition of (μPD78F150xA only) to chapter title	(d)
CHAPTER 31 ELECTRICAL SPECIFICATIONS		
Throughout	Addition of specifications of AV_{DD}, EV_{DD1}, and AV_{REF}	(d)
pp.892, 893	Addition of AMPHS1 = 1 to Conditions of Supply current when f_{SUB} = 32.768 kHz	(b)
p.894	Separation of μPD78F150xA and μPD78F151xA in P110, P111 of I_{ADC} Conditions	(d)
p.922	Addition of (μPD78F150xA only) to (1) 12-bit A/D Converter	(d)
p.923	Addition of (μPD78F150xA only) to (2) 10-bit A/D Converter Addition of (μPD78F150xA only) to (3) Operational amplifier Addition of (μPD78F150xA only) to (4) Voltage Reference	(d)
p.924	Addition of (μPD78F150xA only) to (5) D/A Converter	(d)
CHAPTER 32 PACKAGE DRAWINGS		
pp.934, 935	Addition of 78F1510AGC-GAD-AX and 78F1512AGC-GAD-AX to 78K0R/LF3 product series	(d)
p.936	Addition of 78F1513AGC-UEU-AX and 78F1515AGC-UEU-AX to 78K0R/LF3 product series	(d)
p.937	Addition of 78F1516AGF-GAT-AX and 78F1518AGF-GAT-AX to 78K0R/LH3 product series	(d)
CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS		
p.938	Addition of 78F1510AGC-GAD-AX and 78F1512AGC-GAD-AX to 80 pins Addition of 78F1513AGC-UEU-AX and 78F1515AGC-UEU-AX to 100 pins Addition of 78F1516AGF-GAT-AX and 78F1518AGF-GAT-AX to 128 pins Change of Caution: from "μPD78F1503A to 78F1508A" to 78K0R/Lx3	(d)
p.939	Addition of 78F1510AGC-GAD-AX and 78F1512AGC-GAD-AX to 80 pins (14 x14) Change of Caution: from "μPD78F1503A to 78F1508A" to 78K0R/Lx3	(d)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents