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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1510agk-gak-ax

Table 4-4. Port functions (78K0R/LH3) (2/3)

Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG53/RxD3
P51				SEG52/TxD3
P52				SEG51/TI02
P53				SEG50/TI04
P54 to P57				SEG49 to SEG46
P60	I/O	Port 6. 2-bit I/O port. Output is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P70 to P74	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Input of P75 and P76 can be set to TTL buffer. Output of P75 and P77 can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR4
P75				KR5/$\overline{SCK01}$
P76				KR6/SI01
P77				KR7/SO01
P80	I/O	Port 8. 8-bit I/O port. Inputs/output can be specified in 1-bit units. Output of P80 and P82 can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$/INTP11
P81				RxD0/SI00/INTP9
P82				TxD0/SO00
P83				–
P84				TI10/TO10
P85				TI11/TO11
P86				TI12/TO12
P87				TI13/TO13
P90 to P97	I/O	Port 9. 8-bit I/O port. Inputs/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG45 to SEG38
P100 to P102	I/O	Port 10. 3-bit I/O port. Inputs/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG29 to SEG27
<R> P110	I/O	Port 11. 2-bit I/O port. Inputs/output can be specified in 1-bit units.	Input port	ANO0 Note
P111				ANO1 Note
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2

<R> **Note** ANOx applies to μPD78F150xA only.

4.2.9 Port 8

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P80/$\overline{\text{SCK00}}$/INTP11	–	√	√
P81/RxD0/SI00/INTP9	–	√	√
P82/TxD0/SO00	–	√	√
P83	–	–	√
P84/TO10/TI10	–	–	√
P85/TO11/TI11	–	–	√
P86/TO12/TI12	–	–	√
P87/TO13/TI13	–	–	√

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8). When the P80 to P87 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 8 (PU8).

Output from the P80 and P82 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 8 (POM8).

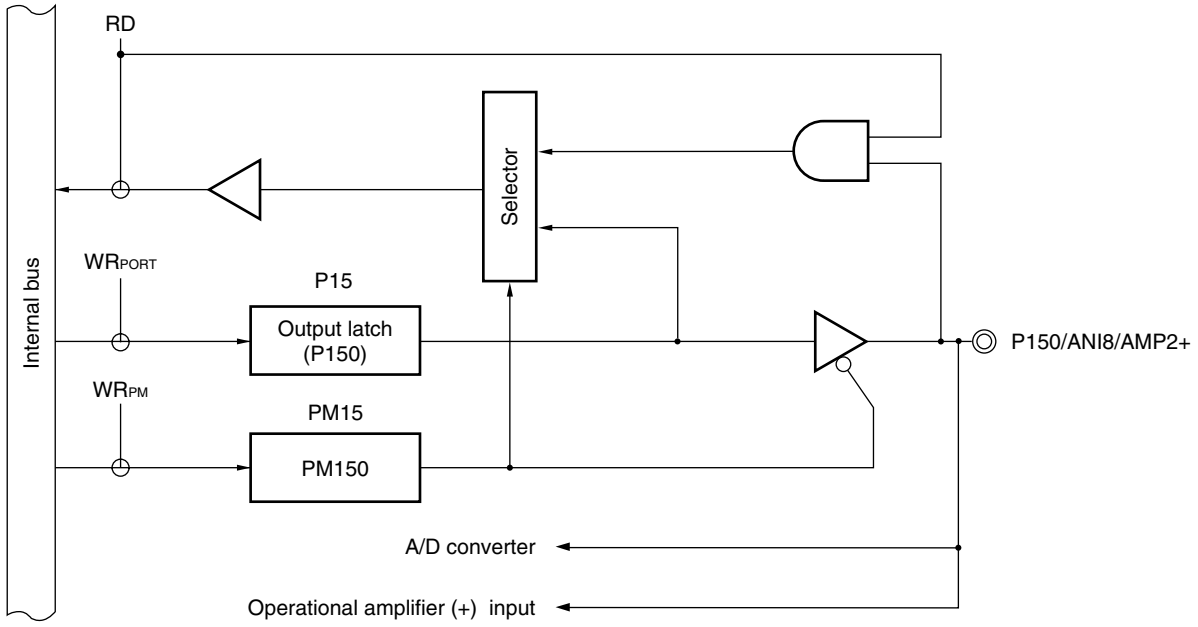
This port can also be used for serial interface clock I/O, data I/O, timer I/O, and external interrupt request input.

Reset signal generation sets port 8 to input mode.

Figures 4-20 to 4-24 show block diagrams of port 8.

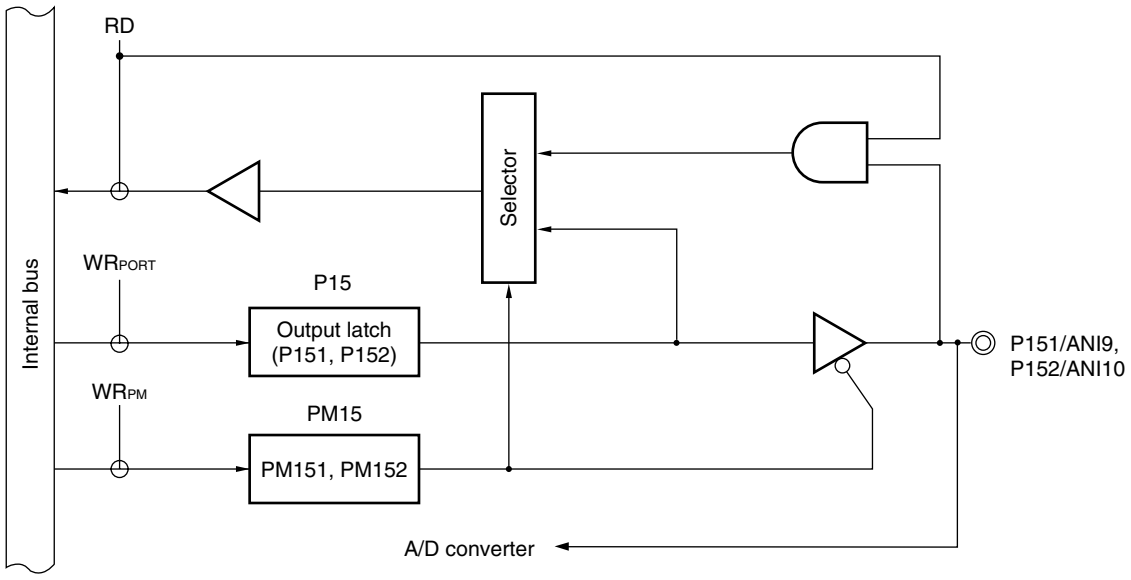
Caution To use P80/$\overline{\text{SCK00}}$/INTP11, P81/RxD0/SI00/INTP9, and P82/SO00/TxD0, as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 14-5 Relationship Between Register Settings and Pins (Channel 0 of unit 0: CSI00, UART0 Reception).

Figure 4-35. Block Diagram of P150



P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

Figure 4-36. Block Diagram of P151, P152



P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

(5) Port output mode registers (POMx)

These registers set the output mode of P10 to P15, P75, P77, P80, or P82 in 1-bit units.

N-ch open drain output (V_{DD} tolerance) mode can be selected during serial communication with an external device of the different potential, and for the SDA10, SDA20 pin during simplified I^2C communication with an external device of the same potential.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4-48. Format of Port Output Mode Register

- 78K0R/LF3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W

- 78K0R/LG3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM8	0	0	0	0	0	POM82	0	POM80	F0058H	00H	R/W

- 78K0R/LH3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM7	POM77	0	POM75	0	0	0	0	0	F0057H	00H	R/W
POM8	0	0	0	0	0	POM82	0	POM80	F0058H	00H	R/W

POMmn	Pmn pin output mode selection (m = 1, 7, and 8; n = 0 to 5 and 7)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

Figure 13-3. Format of Analog Reference Voltage Control Register (ADVRC)

Address: FFF36H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADVRC	ADREF	0	0	0	VRSEL	0	VRGV	VRON

ADREF	Negative reference voltage supply of A/D converter selection
0	AV_{SS}
1	AV_{REFM} (external voltage reference input)

VRSEL	VRGV	VRON	Positive reference voltage supplies selection of A/D and D/A converters	Operation control of voltage reference	Output voltage selection of voltage reference	Operation control of input gate voltage boost circuit for A/D converter	Relationship with the conversion mode used
0	0	0	AV_{REFP} (external voltage reference input)	Stops operation (Hi-Z)	2.5 V	Stops operation	Can be set in normal mode 1.
0	1	0			2.0 V	Enables operation	Can be set in normal mode 2 or low voltage mode.
1	0	0	V_{REFOUT} (voltage reference output)	Stops operation (pull-down output)	2.5 V	Stops operation	–
1	0	1		Enables operation	2.5 V	Enables operation	Can be set in normal mode 2 or low voltage mode.
1	1	0		Stops operation (pull-down output)	2.0 V		–
1	1	1		Enables operation	2.0 V		Can be set in normal mode 2 or low voltage mode.
Other than the above			Setting prohibited				

Cautions 1. During voltage reference operation, be sure to connect a tantalum capacitor (capacitance: 10 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) and a ceramic capacitor (capacitance: 0.1 μF±30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) to the V_{REFOUT}/AV_{REFP} pin for stabilizing the reference voltage. Furthermore, do not apply a voltage from the V_{REFOUT}/AV_{REFP} pin during voltage reference operation.

2. To use voltage reference output (V_{REFOUT}) to the positive reference voltage of the A/D converter (AD_{REFP}) and the positive reference voltage of the D/A converter (DA_{REFP}), be sure to set VRON to 1 after setting VRSEL to 1.

Cautions 3. Rewriting DACSWn (n = 0, 1) during A/D conversion is prohibited when both the positive reference voltage of the A/D converter (AD_{REFP}) and the positive reference voltage of the D/A converter (DA_{REFP}) are the voltage reference output (V_{REFOUT}) (VRSEL = 1 and DAREF = 1). Rewrite it when conversion operation is stopped (ADCS = 0).

4. Do not change the output voltage of the reference voltage by using VRGV during the voltage reference operation (VRON = 1).

13.4 Voltage Reference Operations

The voltage reference has the following mode.

- **Reference voltage output mode**

  A reference voltage is output from the V_{REFOUT} pin. Furthermore, the generated reference voltage is supplied to the internal A/D and D/A converters. 2.0 V (TYP.) or 2.5 V (TYP.) can be selected as the output voltage.

13.4.1 Reference voltage output mode

The procedure for starting operation is described below.

<1> Set bit 5 (ADCEN) of peripheral enable register 0 (PER0) to 1 to start the supply of the input clock to the voltage reference.

<2> Set bit 3 (VRSEL) of the analog reference voltage control register (ADVRC) to 1. The positive reference voltage of both the A/D and D/A converters or only the A/D converter is set to voltage reference output.

<3> Specify the reference voltage value by using bit 1 (VRGV) of ADVRC.

<4> Enable voltage reference operation by setting bit 0 (VRON) of ADVRC to 1.

<5> Use software to wait until the voltage reference operation stabilizes (settling time: 17 ms (max.)).

13.5 Cautions for Voltage Reference

Observe the following cautions when using the voltage reference.

- The V_{REFOUT} output voltage can be used only as the positive reference voltage of the internal A/D and D/A converters of the microcontroller. Do not connect an external circuit other than a tantalum capacitor (capacitance: 10 μF$\pm$30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) and a ceramic capacitor (capacitance: 0.1 μF$\pm$30 %, ESR: 2 Ω (max.), ESL: 10 nH (max.)) to the V_{REFOUT} pin for stabilizing the reference voltage.

(5) Higher 7 bits of the serial data register mn (SDRmn)

SDRmn is the transmit/receive data register (16 bits) of channel n. Bits 7 to 0 function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (MCK).

If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 0, the clock set by dividing the operating clock by the higher 7 bits of SDRmn is used as the transfer clock.

For the function of the lower 8 bits of SDRmn, see **14.2 Configuration of Serial Array Unit**.

SDRmn can be read or written in 16-bit units.

However, the higher 7 bits can be written or read only when the operation is stopped (SEmn = 0). During operation (SEmn = 1), a value is written only to the lower 8 bits of SDRmn. When SDRmn is read during operation, 0 is always read.

Reset signal generation clears this register to 0000H.

Figure 14-8. Format of Serial Data Register mn (SDRmn)

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01), FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03), FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11), FFF14H, FFF15H (SDR12), FFF16H, FFF17H (SDR13) — After reset: 0000H — R/W

FFF11H (SDR00) | FFF10H (SDR00)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn								0								

SDRmn[15:9]							Transfer clock setting by dividing the operating clock (MCK)
0	0	0	0	0	0	0	MCK/2
0	0	0	0	0	0	1	MCK/4
0	0	0	0	0	1	0	MCK/6
0	0	0	0	0	1	1	MCK/8
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	MCK/254
1	1	1	1	1	1	1	MCK/256

Cautions 1. Be sure to clear bit 8 to "0".

2. Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.

3. Setting SDRmn[15:9] = 0000000B is prohibited when the simplified I^2C is used. Set SDRmn[15:9] to 0000001B or greater.

Remarks 1. For the function of the lower 8 bits of SDRmn, see **14.2 Configuration of Serial Array Unit**.

2. m: Unit number (m = 0, 1)

n: Channel number (n = 0 to 3)

(7) Serial flag clear trigger register mn (SIRmn)

SIRmn is a trigger register that is used to clear each error flag of channel n.

When each bit (FECTmn, PECTmn, OVCTmn) of this register is set to 1, the corresponding bit (FEFmn, PEFmn, OVFmn) of serial status register mn is cleared to 0. Because SIRmn is a trigger register, it is cleared immediately when the corresponding bit of SSRmn is cleared.

SIRmn can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of SIRmn can be set with an 8-bit memory manipulation instruction with SIRmnL.

Reset signal generation clears this register to 0000H.

Figure 14-10. Format of Serial Flag Clear Trigger Register mn (SIRmn)

Address: F0108H, F0109H (SIR00) to F010EH, F010FH (SIR03), F0148H, F0149H (SIR10), F014AH, F014BH (SIR11), F014EH, F014FH (SIR13) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	FEC Tmn	PEC Tmn	OVC Tmn

FEC Tmn	Clear trigger of framing error of channel n
0	No trigger operation
1	Clears the FEFmn bit of the SSRmn register to 0.

PEC Tmn	Clear trigger of parity error flag of channel n
0	No trigger operation
1	Clears the PEFmn bit of the SSRmn register to 0.

OVC Tmn	Clear trigger of overrun error flag of channel n
0	No trigger operation
1	Clears the OVFmn bit of the SSRmn register to 0.

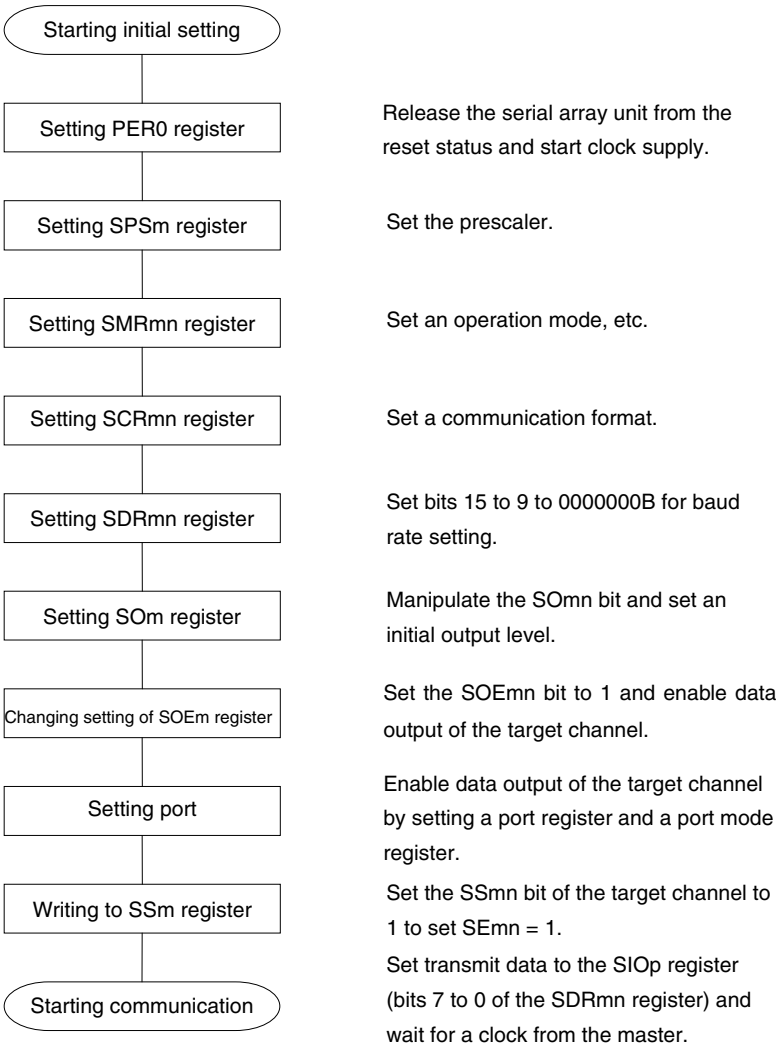
Caution Be sure to clear bits 15 to 3 to "0".

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

2. When the SIRmn register is read, 0000H is always read.

(2) Operation procedure

Figure 14-47. Initial Setting Procedure for Slave Transmission



Caution After setting the SAUmEN to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

15.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the 78K0R/Lx3 microcontrollers as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the 78K0R/Lx3 microcontrollers take part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the 78K0R/Lx3 microcontrollers loose in arbitration and are specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

An example of when the 78K0R/Lx3 microcontrollers are used as the I^2C bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICA interrupt occurrence (communication waiting). When an INTIICA interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

The meanings of <3> to <10> in (2) Address ~ data ~ data in Figure 15-32 are explained below.

<3> If the address received matches the address of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock, and the slave device whose address matched the transmitted slave address also issues an interrupt (INTIICA: address match). The master device and slave device also set a wait status (SCL0 = 0)[Note] when the addresses match.

<5> The master device writes the data to transmit to the IICA shift register (IICA) and releases the wait status that it set by the master device.

<6> If the slave device releases the wait status (WREL = 1), the master device starts transferring data to the slave device.

<7> When data transfer is complete, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<9> The master device writes the data to transmit to the IICA register and releases the wait status that it set by the master device.

<10> The slave device reads the received data and releases the wait status (WREL = 1). The master device then starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

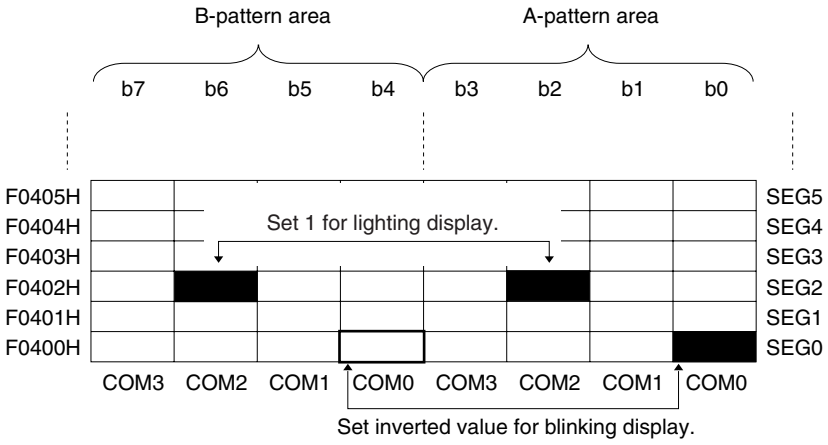
Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

16.9.2 Blinking display (Alternately displaying A-pattern and B-pattern area data)

When BLON = 1 has been set, A-pattern and B-pattern area data will be alternately displayed, according to the constant-period interrupt (INTRTC) timing of the real-time counter (RTC). Refer to **CHAPTER 7 REAL-TIME COUNTER** about the setting of the RTC constant-period interrupt (INTRTC) timing.

For blinking display of the LCD, set inverted values to the B-pattern area bits corresponding to the A-pattern area bits. (Example: Set 1 to bit 0 of 00H, and set 0 to bit 4 of F0400H for blinking display.) When not setting blinking display of the LCD, set the same values. (Example: Set 1 to bit 2 of F0402H, and set 1 to bit 6 of F0402H for lighting display.)

Figure 16-34. Example of LCD Display Data Setting During Pattern-Switching Display



Refer to **16.4 LCD Display Data Memory** about the display area.
Next, the timing operation of display switching is shown.

Figure 16-35. Switching Operation from A-Pattern Display to Blinking Display

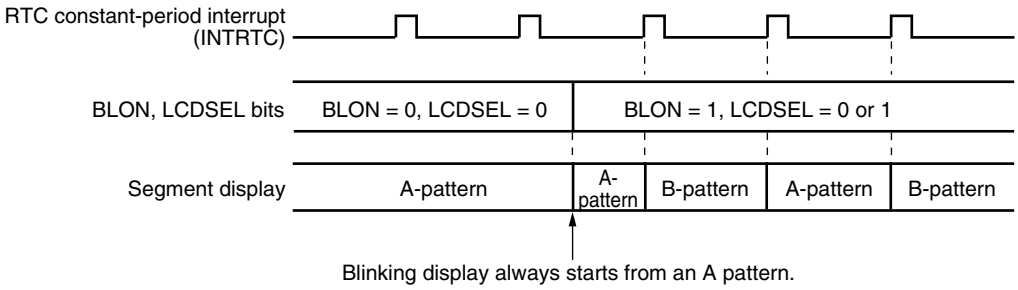


Figure 16-36. Switching Operation from Blinking Display to A-Pattern Display

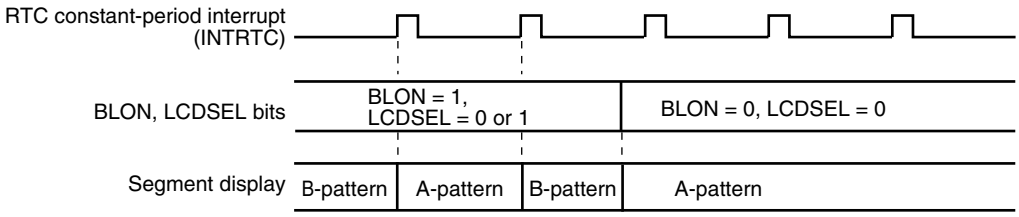


Figure 19-7. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H) (78K0R/LH3)

Address: FFFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	SREMK0	CSIMK01 SRMK0	CSIMK00 STMK0	DMAMK1	DMAMK0	SREMK3	SRMK3	STMK3

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	IICAMK	SREMK1	SRMK1	CSIMK10 IICMK10 STMK1

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1H	TMMK04	SREMK2	SRMK2	CSIMK20 IICMK20 STMK2	KRMK	RTCIMK	RTCMK	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK2L	PMK10	PMK9	PMK8	PMK7	PMK6	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
MK2H	1	1	MDMK	TMMK13	TMMK12	TMMK11	TMMK10	PMK11

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution Be sure to set bits 6, 7 of MK2H to 1.

22.1 Register for Confirming Reset Source

Many internal reset generation sources exist in the 78K0R/Lx3 microcontrollers. The reset control flag register (RESF) is used to store which source has generated the reset request.

RESF can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset by power-on-clear (POC) circuit, and reading RESF clear TRAP, WDRF, and LVIRF.

Figure 22-5. Format of Reset Control Flag Register (RESF)

Address: FFFA8H After reset: Undefined R

Symbol	7	6	5	4	3	2	1	0
RESF	TRAP Note 1	Undefined	Undefined	WDRF Note 1	Undefined	Undefined	Undefined	LVIRF Note 1

TRAP	Internal reset request by execution of illegal instruction Note 2
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

WDRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by low-voltage detector (LVI)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

Notes 1. The value after reset varies depending on the reset source.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Cautions 1. Do not read data by a 1-bit memory manipulation instruction.

2. Do not make a judgment based on only the read value of the RESF register 8-bit data, because bits other than TRAP, WDRF, and LVIRF become undefined.

3. When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, LVIRF flag may become 1 from the beginning depending on the power-on waveform.

The status of RESF when a reset request is generated is shown in Table 22-3.

Table 22-3. RESF Status When Reset Request Is Generated

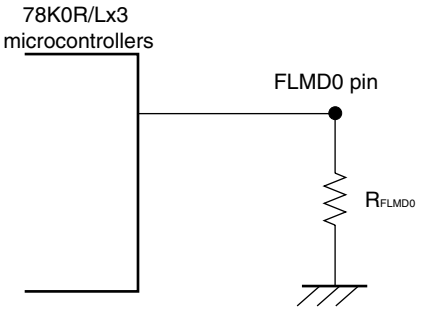
Flag \ Reset Source	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by LVI
TRAP	Cleared (0)	Cleared (0)	Set (1)	Held	Held
WDRF			Held	Set (1)	Held
LVIRF			Held	Held	Set (1)

DC Characteristics (7/11)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{DD0} ≤ V_{DD}, 1.8 V ≤ AV_{DD1} ≤ V_{DD}, 1.8 V ≤ AV_{DD} ≤ V_{DD}, 1.8 V ≤ EV_{DD1} = V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P02, P10 to P17, P30 to P34, P40, P41, P50 to P57, P60, P61, P70 to P77, P80 to P87, P90 to P97, P100 to P102, P120, P140 to P147, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P27, P150 to P152, P157 (μPD78F150xA)	$V_I = AV_{DD0}$				1	μA
<R>		P20 to P27, P150 to P152, P157 (μPD78F151xA)	$V_I = AV_{DD}$				1	μA
		P110, P111 (μPD78F150xA)	$V_I = AV_{DD1}$				1	μA
<R>		P110, P111 (μPD78F151xA)	$V_I = EV_{DD1}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	In input port			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P10 to P17, P30 to P34, P40, P41, P50 to P57, P60, P61, P70 to P77, P80 to P87, P90 to P97, P100 to P102, P120, P140 to P147, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P20 to P27, P150 to P152, P157	$V_I = V_{SS}$				–1	μA
		P110, P111	$V_I = V_{SS}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	In input port			–1	μA
				In resonator connection			–10	μA
On-chip pll-up resistance	R_U	P00 to P02, P10 to P17, P30 to P34, P40, P41, P50 to P57, P70 to P77, P80 to P87, P90 to P97, P100 to P102, P120, P140 to P147	$V_I = V_{SS}$, In input port		10	20	100	kΩ
FLMD0 pin external pull-down resistance Note	R_{FLMD0}	When enabling the self-programming mode setting with software			100			kΩ

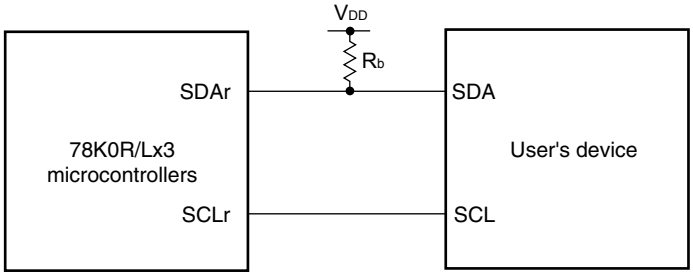
Note It is recommended to leave the FLMD0 pin open. If the pin is required to be pulled down externally, set R_{FLMD0} to 100 kΩ or more.



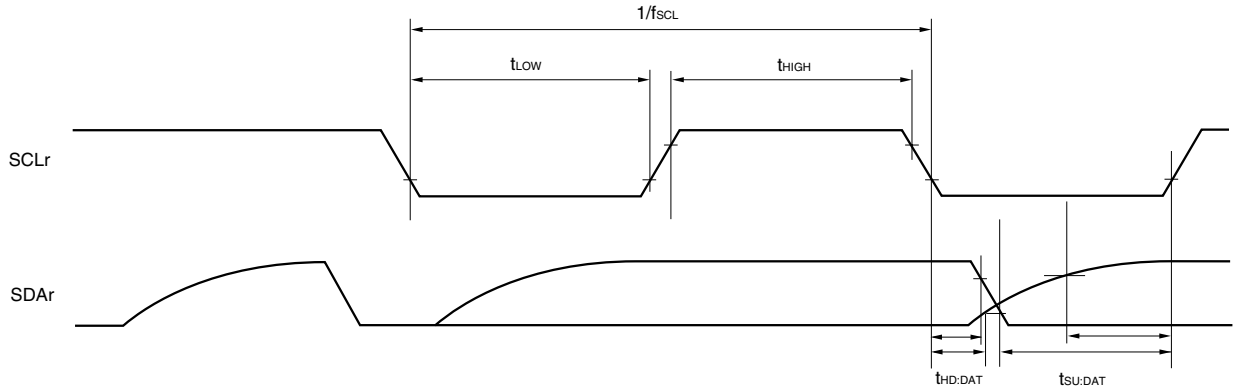
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Serial interface: Serial array unit (6/18)

Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance,
C_b[F]: Communication line (SCLr, SDAr) load capacitance

2. r: IIC number (r = 10, 20)

(2) Serial interface: Serial array unit (15/18)

Caution Select the TTL input buffer for SIp and $\overline{SCKp}$ and the N-ch open drain output (V_{DD} tolerance) mode for SOp by using the PIMg and POMx registers.

Remarks 1. p: CSI number (p = 00, 01, 10, 20), g: PIM number (g = 1, 7), x: POM number (x = 1, 7, 8)

2. R_b[Ω]:Communication line (SOp) pull-up resistance,
C_b[F]: Communication line (SOp, $\overline{SCKp}$) load capacitance, V_b[V]: Communication line voltage

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of the SMRmn register. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

(2) Serial interface: Serial array unit (17/18)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AVss = 0 V)

(h) Communication at different potential (2.5 V, 3 V) (simplified I^2C mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, R_b = 1.4 kΩ, C_b = 100 pF		400	kHz
		2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, R_b = 2.7 kΩ, C_b = 100 Pf		400	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, R_b = 1.4 kΩ, C_b = 100 pF	1275		ns
		2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, R_b = 2.7 kΩ, C_b = 100 pF,	1275		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, R_b = 1.4 kΩ, C_b = 100 pF	655		ns
		2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, R_b = 2.7 kΩ, C_b = 100 pF	655		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, R_b = 1.4 kΩ, C_b = 100 pF	1/f_{MCK} + 190		ns
		2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, R_b = 2.7 kΩ, C_b = 100 pF	1/f_{MCK} + 190		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, R_b = 1.4 kΩ, C_b = 100 pF	0	640	ns
		2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, R_b = 2.7 kΩ, C_b = 100 pF	0	660	ns

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for SDAr and the N-ch open drain output (V_{DD} tolerance) mode for SCLr by using the PIMg and POMx registers.

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 10, 20), g: PIM number (g = 1, 7), x: POM number (x = 1, 7, 8)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of the SMRmn register. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 02, 10)

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I^2C mode mode.
4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} = EV_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 4	Soft	Port functions	P14/SI10/RxD1/SDA10/INTP4, P15/$\overline{\text{SCK10}}$/SCL10/INTP7	To use P14/SI10/RxD1/SDA10/INTP4 and P15/$\overline{\text{SCK10}}$/SCL10/INTP7 as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 14-7 Relationship Between Register Settings and Pins (Channel 2 of unit 0: CSI10, UART1 Transmission, IIC10)	p.133 ☐
			P16/TO05/TI05/INTP10	To use P16/TO05/TI05/INTP10 as a general-purpose port, set bit 5 (TO05) of timer output register 0 (TO0) and bit 5 (TOE05) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.	p.133 ☐
	Hard		Port 2	Make the AV_{DD0} pin the same potential as the EV_{DD} or V_{DD} pin when port 2 is used as a digital port.	p.138 ☐
	Soft		P30/TO00/TI03/RTC1HZ/INTP1	To use P30/TO00/TI03/RTC1HZ/INTP1 as a general-purpose port, set bit 5 (RCLOE1) of real-time counter control register 0 (RTCC0), bit 0 (TO00) of timer output register 0 (TO0) and bit 0 (TOE00) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.	p.142 ☐
			P31/TO03/TI00/RTCDIV/RTCCL/PCLBUZ1/INTP2	To use P31/TO03/TI00/RTCDIV/RTCCL/PCLBUZ1/INTP2 as a general-purpose port, set bit 4 (RCLOE0) of real-time counter control register 0 (RTCC0), bit 6 (RCLOE2) of real-time counter control register 2 (RTCC2), bit 3 (TO03) of timer output register 0 (TO0), bit 3 (TOE03) of timer output enable register 0 (TOE0) and bit 7 of clock output select register 1 (CKS1) to "0", which is the same as their default status setting.	p.142 ☐
			P32/TO01/TI01/INTP5/PCLBUZ0	To use P32/TO01/TI01/INTP5/PCLBUZ0 as a general-purpose port, set bit 1 (TO01) of timer output register 0 (TO0), bit 1 (TOE01) of timer output enable register 0 (TOE0) and bit 7 of clock output select register 0 (CKS0) to "0", which is the same as their default status setting.	p.142 ☐
			P33/TO07/TI07/INTP3, P34/TO06/TI06/INTP8	To use P33/TO07/TI07/INTP3 and P34/TO06/TI06/INTP8 as a general-purpose port, set bit 7, 6 (TO07, TO06) of timer output register 0 (TO0), and bit 7, 6 (TOE07, TOE06) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.	p.142 ☐
	Hard		P40, P41	When a tool is connected, the P40 pin cannot be used as a port pin. When the on-chip debug function is used, P41 pin can be used as follows by the mode setting on the debugger. • 1-line mode: can be used as a port (P41). • 2-line mode: used as a TOOL1 pin and cannot be used as a port (P41).	p.144 ☐
	Soft		P60/SCL0, P61/SDA0	When using P60/SCL0 and P61/SDA0 as a general-purpose port, stop the operation of serial interface IICA.	p.150 ☐
			P75/$\overline{\text{SCK01}}$/KR5, P76/SI01/KR6, P77/SO01/KR7	To use P75/$\overline{\text{SCK01}}$/KR5, P76/SI01/KR6 and P77/SO01/KR7, as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 14-6 Relationship Between Register Settings and Pins (Channel 1 of unit 0: CSI01, UART0 Reception).	p.151 ☐
			P80/$\overline{\text{SCK00}}$/INTP11, P81/RxD0/SI00/INTP9, P82/SO00/TxD0	To use P80/$\overline{\text{SCK00}}$/INTP11, P81/RxD0/SI00/INTP9 and P82/SO00/TxD0, as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 14-5 Relationship Between Register Settings and Pins (Channel 0 of unit 0: CSI00, UART0 Reception).	p.156 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 10	Soft	A/D converter	ADS: Analog input channel specification register	Be sure to clear bits 4 to 7 to “0”.	p.398 ☐
				Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 and 15 (PM2, PM15).	p.398 ☐
				Do not set the pin that is set by ADPC as digital I/O by ADS.	p.398 ☐
				When using an operational amplifier n, the output signal of an operational amplifier n can be used as an analog input.	p.398 ☐
			ADPC: A/D port configuration register	Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 and 15 (PM2, PM15).	p.399 ☐
				Do not set the pin that is set by ADPC as digital I/O by ADS.	p.399 ☐
			PM2, PM15: Port mode registers 2 and 15	If a pin is set as an analog input port, not the pin level but “0” is always read.	p.400 ☐
				When an operational amplifier is used, pins AMPn+, AMPn−, and AMPnO are used, so the alternative analog input functions cannot be used. The operational amplifier output signals, however, can be used as analog inputs.	p.401 ☐
			Basic operations of A/D converter	Make sure the period of <4> to <8> is 1 μs or more.	p.404 ☐
				To use an operational amplifier output for an analog input, start operating the operational amplifier before setting the A/D conversion operation (see CHAPTER 12 OPERATIONAL AMPLIFIER). Furthermore, do not change the operational amplifier setting during the A/D conversion operation.	p.404 ☐
				To use an output voltage of the voltage reference for a positive reference voltage of the A/D converter, start operating the voltage reference before setting the A/D conversion operation (see CHAPTER 13 VOLTAGE REFERENCE). Furthermore, do not change the voltage reference setting during the A/D conversion operation.	p.404 ☐
				When using the A/D converter in normal mode 2 (LV1 = 0, LV0 = 1) or low voltage mode (LV1 = 1, LV0 = 0), enable the input gate voltage boost circuit for the A/D converter by using the analog reference voltage control register (ADVRC), and then set ADCE and ADCS to 1. After the voltage boost circuit stabilization time (10 μs) passes after the input gate voltage boost circuit for the A/D converter has been enabled, set ADCS to 1.	p.404 ☐
			A/D conversion operation	Make sure the period of <4> to <8> is 1 μs or more.	p.411 ☐
				<4> may be done between <5> and <7>.	p.411 ☐
				<4> can be omitted. However, ignore data of the first conversion after <8> in this case.	p.411 ☐
				The period from <9> to <13> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM. The period from <12> to <13> is the conversion time set using FR2 to FR0, LV1, and LV0.	p.411 ☐
				To use an operational amplifier output for an analog input, start operating the operational amplifier before setting the A/D conversion operation (see CHAPTER 12 OPERATIONAL AMPLIFIER). Furthermore, do not change the operational amplifier setting during the A/D conversion operation.	p.411 ☐
				To use an output voltage of the voltage reference for a positive reference voltage of the A/D converter, start operating the voltage reference before setting the A/D conversion operation (see CHAPTER 13 VOLTAGE REFERENCE). Furthermore, do not change the voltage reference setting during the A/D conversion operation.	p.411 ☐
				When using the A/D converter in normal mode 2 (LV1 = 0, LV0 = 1) or low voltage mode (LV1 = 1, LV0 = 0), enable the input gate voltage boost circuit for the A/D converter by using the analog reference voltage control register (ADVRC), and then set ADCE and ADCS to 1. After the voltage boost circuit stabilization time (10 μs) passes after the input gate voltage boost circuit for the A/D converter has been enabled, set ADCS to 1.	p.411 ☐