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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1512agc-gad-ax

1.5 Outline of Functions

<R> μPD78F150xA (1/2)

Item			78K0R/LF3			78K0R/LG3			78K0R/LH3		
			μPD78F1500A	μPD78F1501A	μPD78F1502A	μPD78F1503A	μPD78F1504A	μPD78F1505A	μPD78F1506A	μPD78F1507A	μPD78F1508A
Internal memory	Flash memory (self-programming supported)		64 KB	96 KB	128 KB	64 KB	96 KB	128 KB	64 KB	96 KB	128 KB
	RAM		4 KB	6KB	7KB	4 KB	6KB	7KB	4 KB	6KB	7KB
Memory space			1 MB								
Main system clock (Oscillation frequency)	High-speed system clock		X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V								
	Internal high-speed oscillation clock		Internal oscillation 1 MHz (TYP.) or 8 MHz (TYP.) selected by an option byte								
	20 MHz Internal high-speed oscillation clock		Internal oscillation 20 MHz (TYP.) : V_{DD} = 2.7 to 5.5 V								
Subsystem clock (Oscillation frequency)			XT1 (crystal) oscillation 32.768 kHz (TYP.)								
Internal low-speed oscillation clock (For WDT)			Internal oscillation 30 kHz (TYP.)								
General-purpose register			8 bits × 32 registers (8 bits × 8 registers × 4 banks)								
Minimum instruction execution time			0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)								
			0.125 μs (Internal high-speed oscillation clock: f_{IH} = 8 MHz (TYP.) operation)								
			30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
Instruction set			• 8-bit operation, 16-bit operation • Multiply (16 bits × 16 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.								
I/O port	Total		51			67			83		
	I/O	CMOS	46			60			76		
		N-ch	–			2			2		
	Output	CMOS	1			1			1		
	Input	CMOS	4			4			4		
Timer			• 16-bit timer: 12 channels • Watchdog timer: 1 channel • Real-time counter: 1 channel								
	Timer outputs		6 (PWM output: 5 (Timer array unit 0))			8 (PWM output: 7 (Timer array unit 0))			12 (PWM output: 7 (Timer array unit 0), 3 (Timer array unit 1))		
	RTC outputs		2 • 1 Hz (Subsystem clock: f_{SUB} = 32.768 kHz) • 512 Hz or 16.384 kHz or 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz)								
Clock output/buzzer output			2 • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
A/D converter			12-bit resolution × 8 channels			12-bit resolution × 12 channels					
D/A converter			12-bit resolution × 2 channels								

Table 3-5. SFR List (1/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
					1-bit	8-bit	16-bit				
FFF00H	Port register 0	P0		R/W	√	√	–	00H	√	√	√
FFF01H	Port register 1	P1		R/W	√	√	–	00H	√	√	√
FFF02H	Port register 2	P2		R/W	√	√	–	00H	√	√	√
FFF03H	Port register 3	P3		R/W	√	√	–	00H	√	√	√
FFF04H	Port register 4	P4		R/W	√	√	–	00H	√	√	√
FFF05H	Port register 5	P5		R/W	√	√	–	00H	√	√	√
FFF06H	Port register 6	P6		R/W	√	√	–	00H	–	√	√
FFF07H	Port register 7	P7		R/W	√	√	–	00H	–	–	√
FFF08H	Port register 8	P8		R/W	√	√	–	00H	–	√	√
FFF09H	Port register 9	P9		R/W	√	√	–	00H	√	√	√
FFF0AH	Port register 10	P10		R/W	√	√	–	00H	√	√	√
FFF0BH	Port register 11	P11		R/W	√	√	–	00H	√	√	√
FFF0CH	Port register 12	P12		R/W	√	√	–	Undefined	√	√	√
FFF0DH	Port register 13	P13		R/W	√	√	–	00H	√	√	√
FFF0EH	Port register 14	P14		R/W	√	√	–	00H	√	√	√
FFF0FH	Port register 15	P15		R/W	√	√	–	00H	√	√	√
FFF10H	Serial data register 00	TXD0/ SIO00	SDR00	R/W	–	√	√	0000H	–	√	√
FFF11H		–			–	–			–	√	√
FFF12H	Serial data register 01	RXD0/ SIO01	SDR01	R/W	–	√	√	0000H	–	√	√
FFF13H		–			–	–			–	√	√
FFF14H	Serial data register 12	TXD3	SDR12	R/W	–	√	√	0000H	√	√	√
FFF15H		–			–	–			√	√	√
FFF16H	Serial data register 13	RXD3	SDR13	R/W	–	√	√	0000H	√	√	√
FFF17H		–			–	–			√	√	√
FFF18H	Timer data register 00	TDR00		R/W	–	–	√	0000H	√	√	√
FFF19H											
FFF1AH	Timer data register 01	TDR01		R/W	–	–	√	0000H	√	√	√
FFF1BH											
FFF1EH	12-bit A/D conversion result register Note	ADCR		R	–	–	√	0000H	√	√	√
FFF1FH	8-bit A/D conversion result register	ADCRH		R	–	√	–	00H	√	√	√
FFF20H	Port mode register 0	PM0		R/W	√	√	–	FFH	√	√	√
FFF21H	Port mode register 1	PM1		R/W	√	√	–	FFH	√	√	√
FFF22H	Port mode register 2	PM2		R/W	√	√	–	FFH	√	√	√
FFF23H	Port mode register 3	PM3		R/W	√	√	–	FFH	√	√	√
FFF24H	Port mode register 4	PM4		R/W	√	√	–	FFH	√	√	√
FFF25H	Port mode register 5	PM5		R/W	√	√	–	FFH	√	√	√
FFF26H	Port mode register 6	PM6		R/W	√	√	–	FFH	–	√	√
FFF27H	Port mode register 7	PM7		R/W	√	√	–	FFH	–	–	√

<R> **Note** For μ PD78F151xA, 10-bit A/D conversion result register is applied.

Table 3-5. SFR List (2/5)

	Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
					1-bit	8-bit	16-bit				
	FFF28H	Port mode register 8	PM8	R/W	√	√	–	FFH	–	√	√
	FFF29H	Port mode register 9	PM9	R/W	√	√	–	FFH	√	√	√
	FFF2AH	Port mode register 10	PM10	R/W	√	√	–	FFH	√	√	√
	FFF2BH	Port mode register 11	PM11	R/W	√	√	–	FFH	√	√	√
	FFF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH	√	√	√
	FFF2EH	Port mode register 14	PM14	R/W	√	√	–	FEH	√	√	√
	FFF2FH	Port mode register 15	PM15	R/W	√	√	–	FFH	√	√	√
	FFF30H	A/D converter mode register	ADM	R/W	√	√	–	00H	√	√	√
	FFF31H	Analog input channel specification register	ADS	R/W	√	√	–	00H	√	√	√
	FFF32H	A/D converter mode register 1	ADM1	R/W	√	√	–	00H	√	√	√
<R>	FFF33H	Operational amplifier control register Note	OAC	R/W	√	√	–	00H	√	√	√
<R>	FFF36H	Analog reference voltage control register	ADVRC	R/W	√	√	–	00H	√	√	√
	FFF37H	Key return mode register	KRM	R/W	√	√	–	00H	–	–	√
	FFF38H	External interrupt rising edge enable register 0	EGP0	R/W	√	√	–	00H	√	√	√
	FFF39H	External interrupt falling edge enable register 0	EGN0	R/W	√	√	–	00H	√	√	√
	FFF3AH	External interrupt rising edge enable register 1	EGP1	R/W	√	√	–	00H	–	√	√
	FFF3BH	External interrupt falling edge enable register 1	EGN1	R/W	√	√	–	00H	–	√	√
	FFF3CH	Input switch control register	ISC	R/W	√	√	–	00H	√	√	√
	FFF3EH	Timer input select register 0	TIS0	R/W	√	√	–	00H	√	√	√
	FFF3FH	Timer input select register 1	TIS1	R/W	√	√	–	00H	√	√	√
	FFF40H	LCD mode register	LCDMD	R/W	√	√	–	00H	√	√	√
	FFF41H	LCD display mode register	LCDM	R/W	√	√	–	00H	√	√	√
	FFF42H	LCD clock control register 0	LCDC0	R/W	√	√	–	00H	√	√	√
	FFF43H	LCD boost level control register	VLCD	R/W	√	√	–	0FH	√	√	√
	FFF44H	Serial data register 02	TXD1/SIO10 / SDR02	R/W	–	√	√	0000H	√	√	√
	FFF45H		–		–	–			√	√	√
	FFF46H	Serial data register 03	RXD1 / SDR03	R/W	–	√	√	0000H	√	√	√
	FFF47H		–		–	–			√	√	√
	FFF48H	Serial data register 10	TXD2/SIO20 / SDR10	R/W	–	√	√	0000H	√	√	√
	FFF49H		–		–	–			√	√	√
	FFF4AH	Serial data register 11	RXD2 / SDR11	R/W	–	√	√	0000H	√	√	√
	FFF4BH		–		–	–			√	√	√
	FFF50H	IICA shift register	IICA	R/W	–	√	–	00H	–	√	√
	FFF51H	IICA status register	IICS	R	√	√	–	00H	–	√	√
	FFF52H	IICA flag register	IICF	R/W	√	√	–	00H	–	√	√
<R>	FFF58H	D/A conversion value setting register 0 Note	DACS0 / DACS	R/W	–	√	–	00H	√	√	√
	FFF59H	D/A conversion value setting register W0 Note	– / W0	R/W	–	–	√	0000H	√	√	√
	FFF5AH	D/A conversion value setting register 1 Note	DACS1 / DACS	R/W	–	√	–	00H	√	√	√
	FFF5BH	D/A conversion value setting register W1 Note	– / W1	R/W	–	–	√	0000H	√	√	√

<R> **Note** Dedicated to μ PD78F150xA.

Figure 4-51. Format of Input Switch Control Register (ISC)

Address: FFF3CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	ISC4	ISC3	ISC2	ISC1	ISC0

ISC4	TI04/SEGxx/P53 schmitt trigger buffer control
0	Disables input
1	Enables input

ISC3	TI02/SEGxx/P52 schmitt trigger buffer control
0	Disables input
1	Enables input

ISC2	RxD3/SEGxx/P50 schmitt trigger buffer control
0	Disables input
1	Enables input

ISC1	Switching channel 7 input of timer array unit
0	Uses the input signal of the TI07 pin as a timer input (normal operation).
1	Input signal of RxD3 pin is used as timer input (wakeup signal detection).

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RxD3 pin as an external interrupt (to measure the pulse widths of the sync break field and sync field).

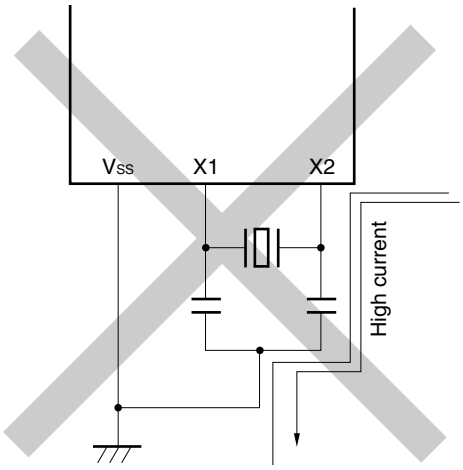
Caution Be sure to clear bits 5 to 7 to "0".

To use the TI04/SEGxx/P53, TI02/SEGxx/P52, and RxD3/SEGxx/P50 pins, set the PF5L and ISCn (n = 2 to 4) bits as follows, according to the function to be used.

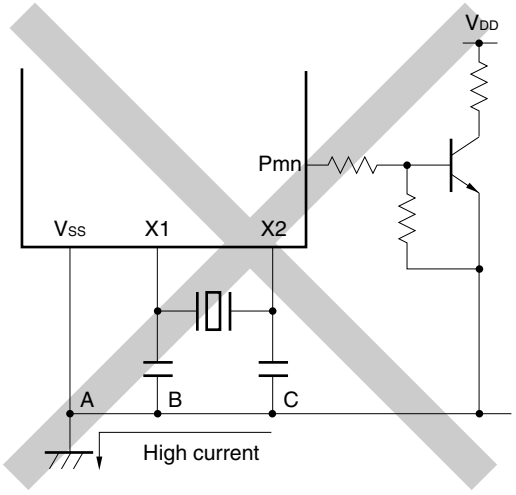
PF5L	ISCn	Pin function
0	0	Port output (default)
0	1	Port input, timer input, or serial data input
1	0	Segment output
1	1	Setting prohibited

Figure 5-12. Examples of Incorrect Resonator Connection (2/2)

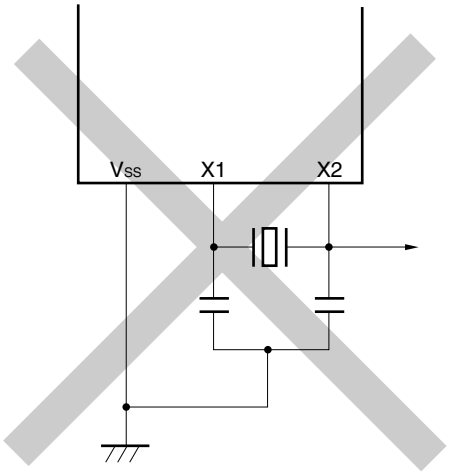
(e) Wiring near high alternating current



(f) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(g) Signals are fetched



Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Caution 2. When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

Table 5-5. Changing CPU Clock (2/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Subsystem clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • HIOSTOP = 0, MCS = 0	XT1 oscillation can be stopped (XTSTOP = 1)
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	20 MHz internal high-speed oscillation clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
20 MHz internal high-speed oscillation clock	Internal high-speed oscillation clock	• SELDSC = 0 (Set when changing the clock.)	20 MHz internal high-speed oscillation clock can be stopped (DSCON = 0)
	X1 clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
	External main system clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
	Subsystem clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–

6.6 Basic Function of Timer Array Unit

6.6.1 Overview of single-operation function and combination operation function

The timer array unit consists of several channels and has a single-operation function that allows each channel to operate independently, and a combination operation function that uses two or more channels in combination.

The single-operation function can be used for any channel, regardless of the operation mode of the other channels.

The combination operation function is realized by combining a master channel (reference timer that mainly counts periods) and a slave channel (timer that operates in accordance with the master channel), and several rules must be observed when using this function.

6.6.2 Basic rules of combination operation function

The basic rules of using the combination operation function are as follows.

(1) Only an even channel (channel 0, 2, 4, etc.) can be set as a master channel.
(2) Any channel, except channel 0, can be set as a slave channel.
(3) The slave channel must be lower than the master channel.
Example: If channel 2 of TAU0 is set as a master channel, channel 3 or those that follow (channels 3, 4, etc. 5) can be set as a slave channel.
If channel 2 of TAU1 is set as a master channel, channel 3 (because TAU1 is provided only with channels up to channel 3) can be set as a slave channel.

(4) Two or more slave channels can be set for one master channel.
(5) When two or more master channels are to be used, slave channels with a master channel between them may not be set.
Example: If channels 0 and 4 of TAU0 are set as master channels, channels 1 to 3 can be set as the slave channels of master channel 0. Channels 5 to 7 cannot be set as the slave channels of master channel 0.

(6) The operating clock for a slave channel in combination with a master channel must be the same as that of the master channel. The CKS bit (bit 15 of the TMRmn register) of the slave channel that operates in combination with the master channel must be the same value as that of the master channel.
(7) A master channel can transmit INTTMmn (interrupt), start software trigger, and count clock to the lower channels.
(8) A slave channel can use the INTTMmn (interrupt), start software trigger, and count clock of the master channel, but it cannot transmit its own INTTMmn (interrupt), start software trigger, and count clock to the lower channel.
(9) A master channel cannot use the INTTMmn (interrupt), start software trigger, and count clock from the higher master channel.
(10) To simultaneously start channels that operate in combination, the TSmn bit of the channels in combination must be set at the same time.
(11) During a counting operation, the TSmn bit of all channels that operate in combination or only the master channel can be set. TSmn of only a slave channel cannot be set.
(12) To stop the channels in combination simultaneously, the TTmn bit of the channels in combination must be set at the same time.

Remark mn: Unit number + Channel number
mn = 00 to 07, 10 to 13

Table 10-6. Setting Functions of ANI9/P151 and ANI10/AM152 Pins

ADPC register	PM15 register	ADS register	ANI9/P151 and ANI10/AM152 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be A/D converted)
		Does not select ANI.	Analog input (not to be A/D converted)
	Output mode	–	Setting prohibited

Remark 78K0R/LF3: ANI9/P151 and ANI10/AM152 are not mounted.
78K0R/LG3, 78K0R/LH3: ANI9/P151, ANI10/AM152

Table 10-7. Setting Functions of ANI15/AVREFM/P157 Pin

ADPC register	PM15 register	ADREF bit	ADS register	ANI15/AVREFM/P157 Pin
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	–	Negative reference voltage input of A/D converter
	Output mode	–	–	Setting prohibited

(4) Serial communication operation setting register mn (SCRmn)

SCRmn is a communication operation setting register of channel n. It is used to set a data transmission/reception mode, phase of data and clock, whether an error signal is to be masked or not, parity bit, start bit, stop bit, and data length.

Rewriting SCRmn is prohibited when the register is in operation (when SEmn = 1).

SCRmn can be set by a 16-bit memory manipulation instruction.

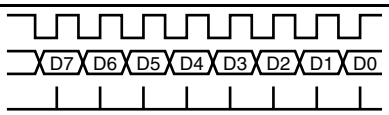
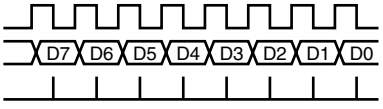
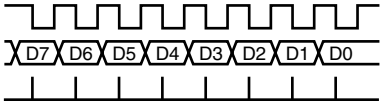
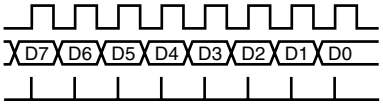
Reset signal generation sets this register to 0087H.

Figure 14-7. Format of Serial Communication Operation Setting Register mn (SCRmn) (1/3)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), F0158H, F0159H (SCR10), F015AH, F015BH (SCR11), F015CH, F015DH (SCR12), F015EH, F015FH (SCR13) — After reset: 0087H — R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	0	DLS mn2	DLS mn1	DLS mn0

TXE mn	RXE mn	Setting of operation mode of channel n
0	0	Does not start communication.
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

DAP mn	CKP mn	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4
Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode and simplified I^2C mode.			

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 20)

15.5.6 Wait

The wait is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCL0 pin to low level notifies the communication partner of the wait state. When wait state has been canceled for both the master and slave devices, the next data transfer can begin.

Figure 15-20. Wait (1/2)

(1) When master device has a nine-clock wait and slave device has an eight-clock wait (master transmits, slave receives, and ACKE = 1)

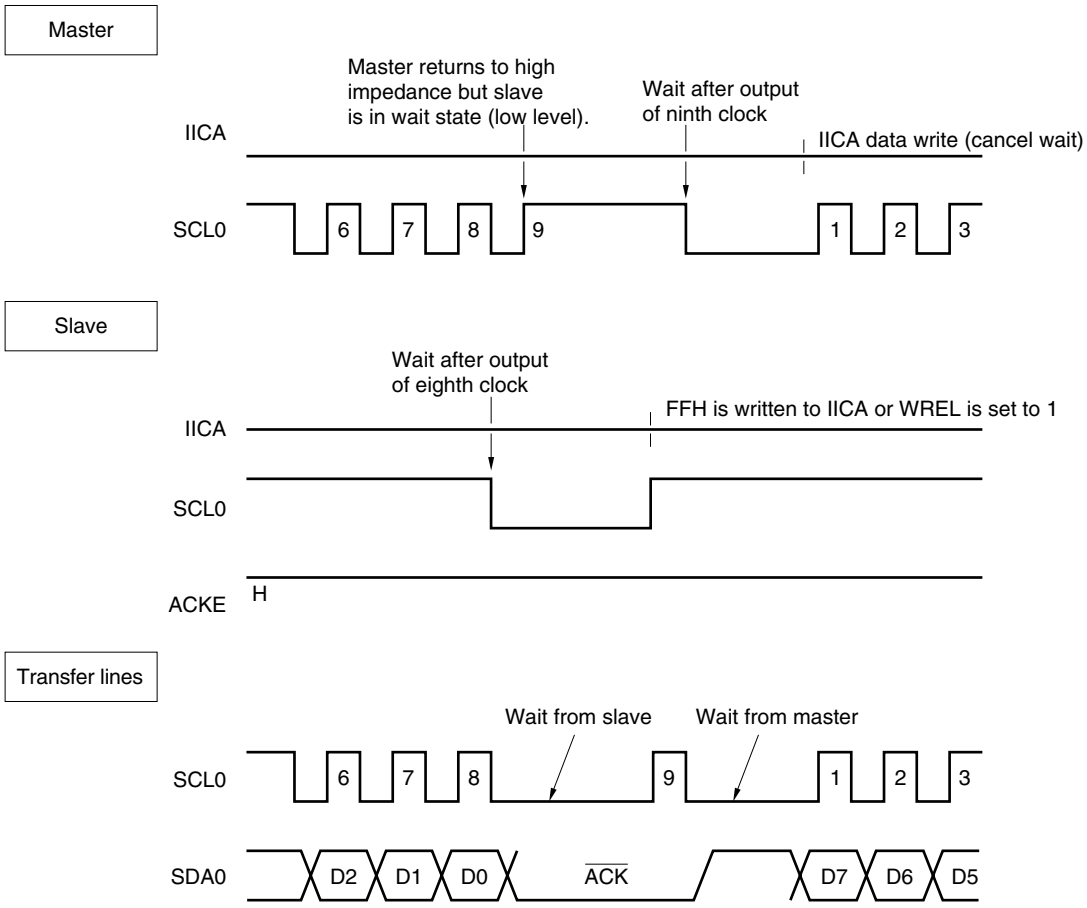
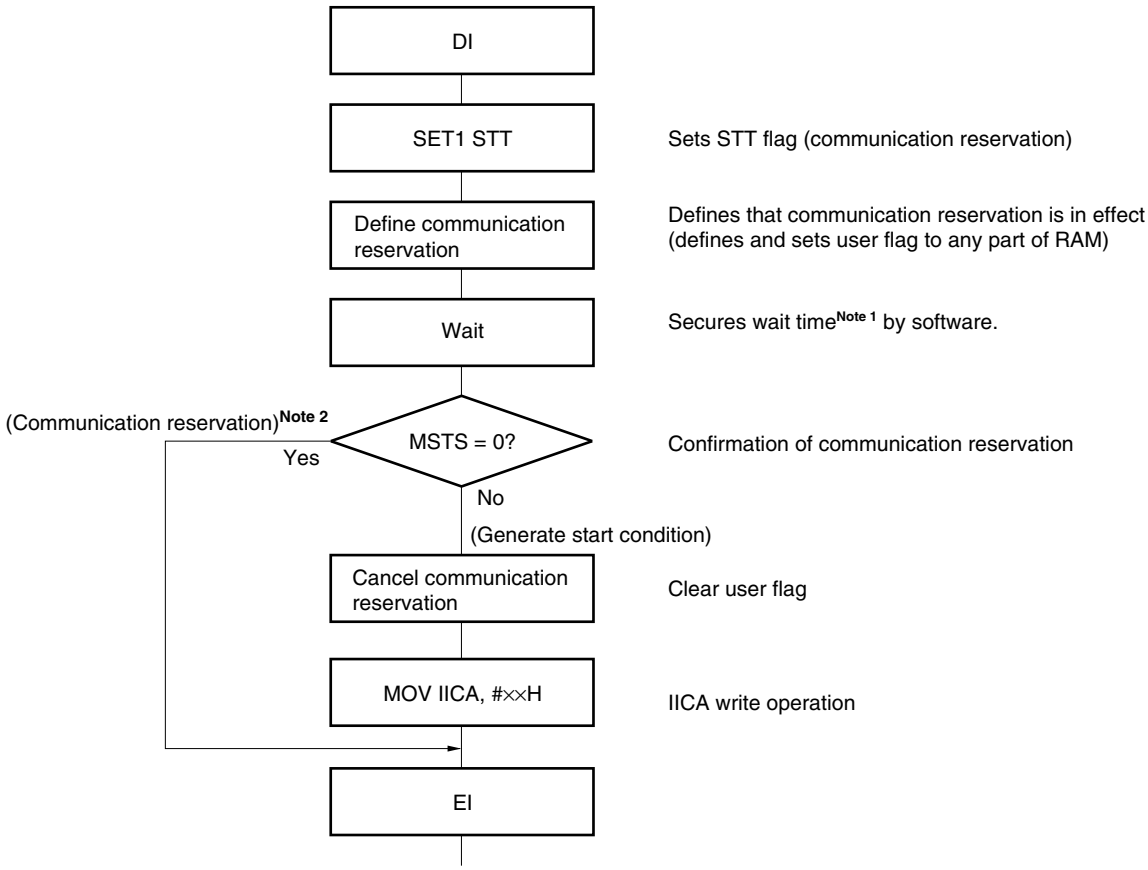


Figure 15-27. Communication Reservation Protocol



Notes 1. The wait time is calculated as follows.
(IICWL setting value + IICWH setting value + 4 clocks) / f_{CLK} + $t_F \times 2$

2. The communication reservation operation executes a write to the IICA shift register (IICA) when a stop condition interrupt request occurs.

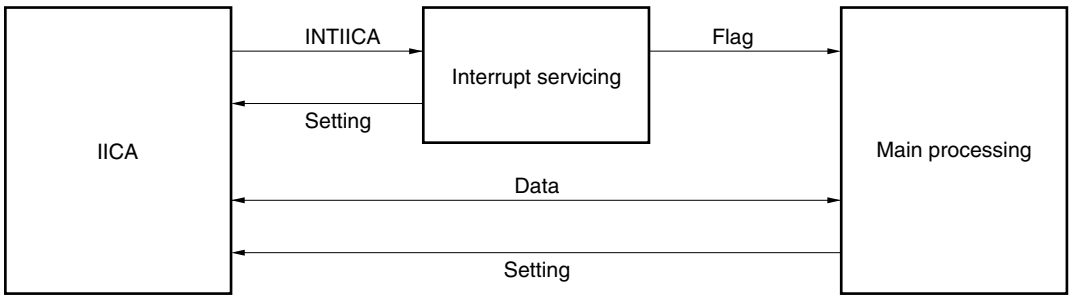
Remark STT: Bit 1 of IICA control register 0 (IICCTL0)
MSTS: Bit 7 of IICA status register (IICS)
IICA: IICA shift register
IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
f_{CLK}: CPU/peripheral hardware clock frequency

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

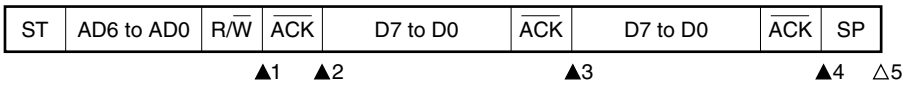
<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIICA interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as TRC.

(ii) When WTIM = 1



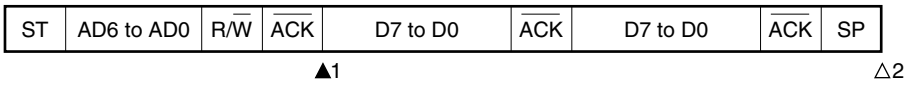
▲1: IICS = 0110×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS bit each time interrupt request signal INTIICA has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data (when WTIM = 1)

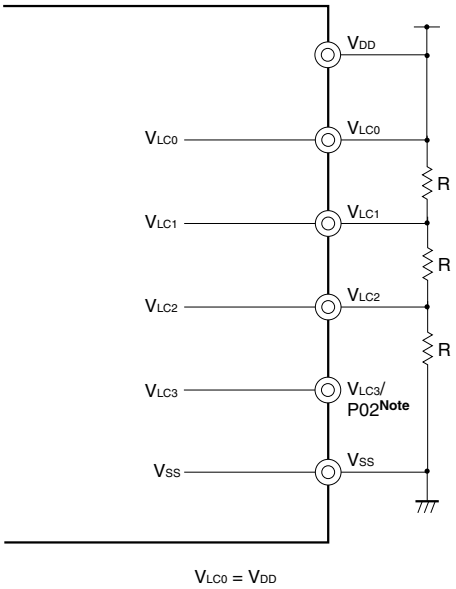


▲1: IICS = 01000110B
△2: IICS = 00000001B

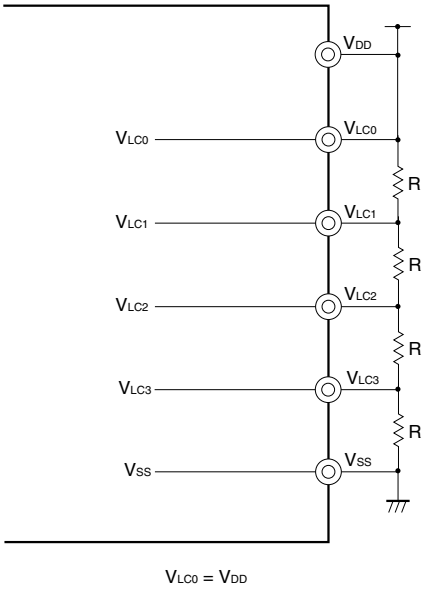
Remark ▲: Always generated
△: Generated only when SPIE = 1

Figure 16-31. Examples of LCD Drive Power Connections (External Resistance Division Method) (2/2)

(c) 1/3 bias method



(d) 1/4 bias method



Note V_{LC3} can be used as port (P02).

Caution To stabilize the potential of the V_{LC0} to V_{LC3} pins, it is recommended to connect a capacitor of about 0.1 μF between each of the pins from V_{LC0} to V_{LC3} and the GND pin as needed.

16.8.2 Internal voltage boosting method

The 78K0R/Lx3 microcontrollers contain an internal voltage boost circuit for generating LCD drive power supplies. The internal voltage boost circuit and external capacitors (0.47 μF±30%) are used to generate an LCD drive voltage. Only 1/3 bias mode or 1/4 bias mode can be set for the internal voltage boost method.

The LCD drive voltage of the internal voltage boost method can supply a constant voltage, regardless of changes in V_{DD}, because it is a power supply separate from the main unit.

In addition, a contrast can be adjusted by using the LCD boost level control register (VLCD).

Table 16-10. LCD Drive Voltages (Internal Voltage Boosting Method)

Bias Method / LCD Drive Voltage Pin	1/3 Bias Method	1/4 Bias Method
V_{LC0}	3 x V_{LC2}	4 x V_{LC3}
V_{LC1}	2 x V_{LC2}	3 x V_{LC3}
V_{LC2}	LCD reference voltage	2 x V_{LC3}
V_{LC3}	–	LCD reference voltage

(3) Multiplication/division data register C (MDCL, MDCH)

The MDCH and MDCL registers store remainder value of the operation result in the division mode. They are not used in the multiplication mode.

MDCH and MDCL can be read by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 17-4. Format of Multiplication/Division Data Register C (MDCH, MDCL)

Address: F00E0H, F00E1H, F00E2H, F00E3H After reset: 0000H, 0000H R

Symbol F00E3H F00E2H

MDCH	MDCH 15	MDCH 14	MDCH 13	MDCH 12	MDCH 11	MDCH 10	MDCH 9	MDCH 8	MDCH 7	MDCH 6	MDCH 5	MDCH 4	MDCH 3	MDCH 2	MDCH 1	MDCH 0

Symbol F00E1H F00E0H

MDCL	MDCL 15	MDCL 14	MDCL 13	MDCL 12	MDCL 11	MDCL 10	MDCL 9	MDCL 8	MDCL 7	MDCL 6	MDCL 5	MDCL 4	MDCL 3	MDCL 2	MDCL 1	MDCL 0

Caution The MDCH and MDCL values read during division operation processing (while the multiplication/division control register (MDUC) is 81H) will not be guaranteed.

Table 17-4. Functions of MDCH and MDCL During Operation Execution

DIVMODE	Operation Mode	Setting	Operation Result
0	Multiplication mode	–	–
1	Division mode	–	MDCH: Remainder (higher 16 bits) MDCL: Remainder (lower 16 bits)

Remark DIVMODE: Bit 7 of the multiplication/division control register (MDUC)

The register configuration differs between when multiplication is executed and when division is executed, as follows.

- Register configuration during multiplication

<Multiplier A> <Multiplier B> <Product>

MDAL (bits 15 to 0) × MDAH (bits 15 to 0) = [MDBH (bits 15 to 0), MDBL (bits 15 to 0)]

- Register configuration during division

<Dividend> <Divisor>

[MDAH (bits 15 to 0), MDAL (bits 15 to 0)] ÷ [MDBH (bits 15 to 0), MDBL (bits 15 to 0)] =

<Quotient> <Remainder>

[MDAH (bits 15 to 0), MDAL (bits 15 to 0)] ··· [MDCH (bits 15 to 0), MDCL (bits 15 to 0)]

Figure 19-10. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (78K0R/LH3) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	SREPR00	CSIPR001 SRPR00	CSIPR000 STPR00	DMAPR01	DMAPR00	SREPR03	SRPR03	STPR03

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	SREPR10	CSIPR101 SRPR10	CSIPR100 STPR10	DMAPR11	DMAPR10	SREPR13	SRPR13	STPR13

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	IICAPR0	SREPR01	SRPR01	CSIPR010 IICPR010 STPR01

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	IICAPR1	SREPR11	SRPR11	CSIPR110 IICPR110 STPR11

CHAPTER 30 INSTRUCTION SET

This chapter lists the instructions in the 78K0R microcontroller instruction set. For details of each operation and operation code, refer to the separate document **78K0R Microcontrollers Instructions User's Manual (U17792E)**.

Remark The shaded parts of the tables in **Table 30-5 Operation List** indicate the operation or instruction format that is newly added for the 78K0R microcontrollers.

30.1 Conventions Used in Operation List

30.1.1 Operand identifiers and specification methods

Operands are described in the "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, !!, $, $!, [ ], and ES: are keywords and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: 16-bit absolute address specification
- !!: 20-bit absolute address specification
- $: 8-bit relative address specification
- $!: 16-bit relative address specification
- [ ]: Indirect address specification
- ES: Extension address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, !!, $, $!, [ ], and ES: symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 30-1. Operand Identifiers and Specification Methods

Identifier	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special-function register symbol (SFR symbol)
sfrp	Special-function register symbols (16-bit manipulatable SFR symbol. Even addresses only[Note])
saddr	FFE20H to FFF1FH Immediate data or labels
saddrp	FFE20H to FF1FH Immediate data or labels (even addresses only[Note])
addr20	00000H to FFFFFH Immediate data or labels
addr16	0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions[Note])
addr5	0080H to 00BFH Immediate data or labels (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note Bit 0 = 0 when an odd address is specified.

30.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

Table 30-2. Symbols in “Operation” Column

Symbol	Function
A	A register; 8-bit accumulator
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
ES	ES register
CS	CS register
AX	AX register pair; 16-bit accumulator
BC	BC register pair
DE	DE register pair
HL	HL register pair
PC	Program counter
SP	Stack pointer
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
RBS	Register bank select flag
IE	Interrupt request enable flag
()	Memory contents indicated by address or register contents in parentheses
X_H, X_L X_S, X_H, X_L	16-bit registers: X_H = higher 8 bits, X_L = lower 8 bits 20-bit registers: X_S = (bits 19 to 16), X_H = (bits 15 to 8), X_L = (bits 7 to 0)
∧	Logical product (AND)
∨	Logical sum (OR)
∀	Exclusive logical sum (exclusive OR)
¯	Inverted data
addr5	16-bit immediate data (even addresses only in 0080H to 00BFH)
addr16	16-bit immediate data
addr20	20-bit immediate data
jdisp8	Signed 8-bit data (displacement value)
jdisp16	Signed 16-bit data (displacement value)

LVI Circuit Characteristics (T_A = –40 to +85°C, $V_{PDR} \le V_{DD} = EV_{DD} \le 5.5$ V, $V_{SS} = EV_{SS} = 0$ V)

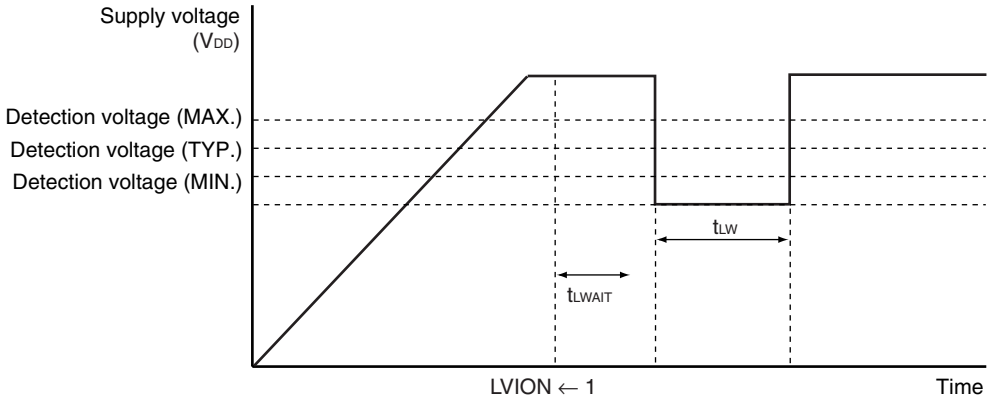
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.12	4.22	4.32	V
		V_{LVI1}		3.97	4.07	4.17	V
		V_{LVI2}		3.82	3.92	4.02	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.35	3.45	3.55	V
		V_{LVI6}		3.20	3.30	3.40	V
		V_{LVI7}		3.05	3.15	3.25	V
		V_{LVI8}		2.89	2.99	3.09	V
		V_{LVI9}		2.74	2.84	2.94	V
		V_{LVI10}		2.58	2.68	2.78	V
		V_{LVI11}		2.43	2.53	2.63	V
		V_{LVI12}		2.28	2.38	2.48	V
		V_{LVI13}		2.12	2.22	2.32	V
		V_{LVI14}		1.97	2.07	2.17	V
		V_{LVI15}		1.81	1.91	2.01	V
	External input pin[Note 1]	V_{EXLVI}	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
	Power supply voltage on power application	V_{PUPLVI}	When LVI default start function enabled is set	1.87	2.07	2.27	V
Minimum pulse width		t_{LW}		200			μs
Detection delay time						200	μs
Operation stabilization wait time[Note 2]		t_{LWAIT}				10	μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

LVI Circuit Timing



(13/14)

Edition	Description	Chapter
4th Edition	Addition of example of calculation of LCD frame frequency to (c) and (d) of **Figure 16-13. Common Signal Waveforms (2/2)**	**CHAPTER 16 LCD CONTROLLER/ DRIVER**
	Change of **Caution** of **Figure 16-31. Examples of LCD Drive Power Connections (External Resistance Division Method)**	
	Change the capacitance value of external capacitors to 0.47 μF±30% in **16.8.2 Internal voltage boosting method** and **16.8.3 Capacitor split method**	
	Addition of **Note** to **Figure 18-4. Format of DMA Mode Control Register n (DMCn) (1/2)**	**CHAPTER 18 DMA CONTROLLER**
	Change of description of **Figure 18-7. Example of Setting for CSI Consecutive Transmission**	
	Addition of **18.5.2 CSI master reception** and **18.5.3 CSI transmission/reception**	
	Change of **18.5.6 Holding DMA transfer pending by DWAITn** and addition of **Caution**	
	Change of **18.5.7 Forced termination by software**	
	Change of **18.6 Cautions on Using DMA Controller**	
	Change value of maskable interrupts of 78K0R/LF3	**CHAPTER 19 INTERRUPT FUNCTIONS**
	Change of **Figure 26-1. Format of User Option Byte (000C0H/010C0H) (1/2)**	**CHAPTER 26 OPTION BYTE**
	Change of **26.4 Setting of Option Byte**	
	Addition of **Figure 27-3. Example of Wiring Adapter for Flash Memory Writing (μPD78F1508A)**	**CHAPTER 27 FLASH MEMORY**
	Addition of **27.9 Creating ROM Code to Place Order for Previously Written Product**	
	Change of Examples 2 in **29.3 BCD Correction Circuit Operation**	**CHAPTER 29 BCD CORRECTION CIRCUIT**
	Change of **Table 30-5. Operation List**	**CHAPTER 30 INSTRUCTION SET**
	Deletion of (TARGET)	**CHAPTER 31 ELECTRICAL SPECIFICATIONS**
	Change of analog output voltage, output current, high, and output current, low in **Absolute Maximum Ratings (T_A = 25°C)**	
	Change of **Internal Oscillator Characteristics**	
	Addition of **Recommended oscillator circuit constants**	
	Change of output voltage, low (V_{OL2}), supply current, and operating current of **DC Characteristics**	
	Change of **Caution** of **(1) Basic operation (3/6)** in **AC Characteristics**	
	Change of **(b) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)** of **(2) Serial interface: Serial array unit (2/18)** and addition of **Note 1**	
	Change of **(c) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)** of **(2) Serial interface: Serial array unit (3/18)**	
	Change of **(d) During communication at same potential (simplified I^2C mode)** of **(2) Serial interface: Serial array unit (5/18)**	
	Change of **(f) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)** of **(2) Serial interface: Serial array unit (11/18)** and addition of **Note 1**	