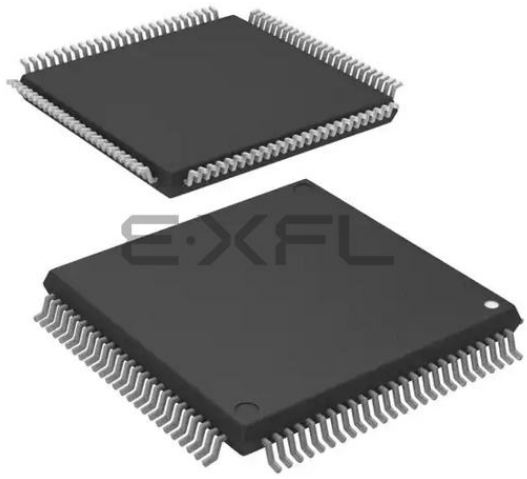
Renesas Electronics America Inc - UPD78F1513AGC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1513agc-ueu-ax

Other Documents

Document Name	Document No.
RENESAS MICROCOMPUTER GENERAL CATALOG	R01CS0001E
SEMICONDUCTOR SELECTION GUIDE − Products and Packages −	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

<R> **Note** See the “Semiconductor Device Mount Manual” website (http://www.renesas.com/prod/package/manual/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

(2) Non-port functions (1/4) : 78K0R/LF3

Function Name	I/O	Function	After Reset	Alternate Function
<R> ANI0	Input	A/D converter analog input	Digital input port	P20/AMP0- Note 1
ANI1				P21/AMP0O Note 1
ANI2				P22/AMP0+ Note 1
ANI3				P23/AMP1- Note 1
ANI4				P24/AMP1O Note 1
ANI5				P25/AMP1+ Note 1
ANI6				P26
ANI15				P157/AV_{REFM} Note 1
<R> AMP0- Note 1	Input	Operational amplifier input (negative side)	Digital input port	P20/ANI0
AMP1- Note 1				P23/ANI3
AMP0+ Note 1	Input	Operational amplifier input (positive side)	Digital input port	P22/ANI2
AMP1+ Note 1				P25/ANI5
AMP0O Note 1	Output	Operational amplifier output	Digital input port	P21/ANI1
AMP1O Note 1				P24/ANI4
AV_{REFM} Note 1	Input	Analog negative reference voltage input	Digital input port	P157/ANI15
AV_{REFP} Note 1		Analog positive reference voltage input	Input	V_{REFOUT} Note 1
AV_{REF} Note 2				–
V_{REFOUT} Note 1	Output	Analog reference voltage output	Input	AV_{REFP} Note 1
ANO0 Note 1	Output	D/A converter analog output	Input port	P110
ANO1 Note 1				P111
SEG0 to SEG3	Output	LCD controller/driver segment signal outputs	Output	COM4 to COM7
SEG4 to SEG10				–
SEG11				P100
SEG12 to SEG19				P147 to P140
SEG20 to SEG22				P92 to P90
SEG23 to SEG26				P57 to P54
SEG27				P53/TI04
SEG28				P52/TI02
SEG29				P51/TxD3
SEG30				P50/RxD3
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output	–
COM4 to COM7				SEG0 to SEG3
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
V_{LC3}			Input port	P02

<R> **Notes 1.** AMPxx, ANOx, AV_{REFP}, AV_{REFM}, and V_{REFOUT} apply to μPD78F150xA only.
2. AV_{REF} applies to μPD78F151xA only.

2.2 Description of Pin Functions

Remark The pins mounted depend on the product. Refer to **1.3 Pin Configuration (Top View)** and **2.1 Pin Function List**.

2.2.1 P00 to P02

P00 to P02 function as an I/O port. This port can also be used for connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

<R>

	78K0R/LF3 (80 pins: μPD78F15x0A, 78F1501A, 78F15x2A)	78K0R/LG3 (100 pins: μPD78F15x3A, 78F1504A, 78F15x5A)	78K0R/LH3 (128 pins: μPD78F15x6A, 78F1507A, 78F15x8A)
P00/CAPH	√		
P01/CAPL	√		
P02/V_{LC3}	√		

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 to P02 function as an I/O port. P00 to P02 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P02 function as connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

(a) CAPH, CAPL

These are the pins for connecting a capacitor for LCD controller/driver.

(b) V_{LC3}

This is the pin for inputting a power supply voltage pin for driving the LCD.

Caution To use P00/CAPH, P01/CAPL, and P02/V_{LC3} as a general-purpose port, set bit 5 (MDSET1) and bit 4 (MDSET0) of LCD mode register (LCDMD) to "0", which is the same as their default status setting.

(4) On-chip debug security ID setting area

A 10-byte area of 000C4H to 000CDH and 010C4H to 010CDH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and 010C4H to 010CDH when the boot swap is used. For details, see **CHAPTER 28 ON-CHIP DEBUG FUNCTION**.

3.1.2 Mirror area

<R> The μPD78F1500A, 78F1503A, 78F01506A, 78F1510A, 78F1513A, and 78F1516A mirror the data flash area of 00000H to 0FFFFH, to F0000H to FFFFFH (the data flash area to be mirrored is set by the processor mode control register (PMC)).

<R> The μPD78F1501A, 78F1502A, 78F1504A, 78F1505A, 78F1507A, 78F1508A, 78F1512A, 78F1515A, and 78F1518A mirror the data flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH (the data flash area to be mirrored is set by the processor mode control register (PMC)).

By reading data from F0000H to FFFFFH, an instruction that does not have the ES registers as an operand can be used, and thus the contents of the data flash can be read with the shorter code. However, the data flash area is not mirrored to the SFR, extended SFR, RAM, and use prohibited areas.

The mirror area can only be read and no instruction can be fetched from this area.

Table 3-5. SFR List (4/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	78K0R/LF3	78K0R/LG3	78K0R/LH3
					1-bit	8-bit	16-bit				
FFF9DH	Real-time counter control register 0	RTCC0		R/W	√	√	–	00H	√	√	√
FFF9EH	Real-time counter control register 1	RTCC1		R/W	√	√	–	00H	√	√	√
FFF9FH	Real-time counter control register 2	RTCC2		R/W	√	√	–	00H	√	√	√
FFFA0H	Clock operation mode control register	CMC		R/W	–	√	–	00H	√	√	√
FFFA1H	Clock operation status control register	CSC		R/W	√	√	–	C0H	√	√	√
FFFA2H	Oscillation stabilization time counter status register	OSTC		R	√	√	–	00H	√	√	√
FFFA3H	Oscillation stabilization time select register	OSTS		R/W	–	√	–	07H	√	√	√
FFFA4H	Clock control register	CKC		R/W	√	√	–	09H	√	√	√
FFFA5H	Clock output select register 0	CKS0		R/W	√	√	–	00H	√	√	√
FFFA6H	Clock output select register 1	CKS1		R/W	√	√	–	00H	√	√	√
FFFA8H	Reset control flag register	RESF		R	–	√	–	Undefined Note 1	√	√	√
FFFA9H	Low-voltage detection register	LVIM		R/W	√	√	–	00H Note 2	√	√	√
FFFAAH	Low-voltage detection level select register	LVIS		R/W	√	√	–	0EH Note 3	√	√	√
FFFABH	Watchdog timer enable register	WDTE		R/W	–	√	–	1A/9A Note 4	√	√	√
FFFB0H	DMA SFR address register 0	DSA0		R/W	–	√	–	00H	√	√	√
FFFB1H	DMA SFR address register 1	DSA1		R/W	–	√	–	00H	√	√	√
FFFB2H	DMA RAM address register 0L	DRA0L	DRA0	R/W	–	√	√	00H	√	√	√
FFFB3H	DMA RAM address register 0H	DRA0H		R/W	–	√		00H	√	√	√
FFFB4H	DMA RAM address register 1L	DRA1L	DRA1	R/W	–	√	√	00H	√	√	√
FFFB5H	DMA RAM address register 1H	DRA1H		R/W	–	√		00H	√	√	√
FFFB6H	DMA byte count register 0L	DBC0L	DBC0	R/W	–	√	√	00H	√	√	√
FFFB7H	DMA byte count register 0H	DBC0H		R/W	–	√		00H	√	√	√
FFFB8H	DMA byte count register 1L	DBC1L	DBC1	R/W	–	√	√	00H	√	√	√
FFFB9H	DMA byte count register 1H	DBC1H		R/W	–	√		00H	√	√	√
FFFBAH	DMA mode control register 0	DMC0		R/W	√	√	–	00H	√	√	√
FFFBBH	DMA mode control register 1	DMC1		R/W	√	√	–	00H	√	√	√
FFFBCH	DMA operation control register 0	DRC0		R/W	√	√	–	00H	√	√	√
FFFBDH	DMA operation control register 1	DRC1		R/W	√	√	–	00H	√	√	√
FFFBEH	Back ground event control register	BECTL		R/W	√	√	–	00H	√	√	√
FFFC0H	–	PFCMD Note 5		–	–	–	–	Undefined	√	√	√
FFFC2H	–	PFS Note 5		–	–	–	–	Undefined	√	√	√
FFFC4H	–	FLPMC Note 5		–	–	–	–	Undefined	√	√	√

Notes 1. The reset value of RESF varies depending on the reset source.

2. The reset value of LVIM varies depending on the reset source and the setting of the option byte.

3. The reset value of LVIS varies depending on the reset source.

4. The reset value of WDTE is determined by the setting of the option byte.

5. Do not directly operate this SFR, because it is to be used in the self programming library.

Table 4-6. Setting Functions of ANI0/AMP0-/P20, ANI2/AMP0+/P22, ANI3/AMP1-/P23, ANI5/AMP1+/P25, and ANI6/AMP2-/P26 Pins

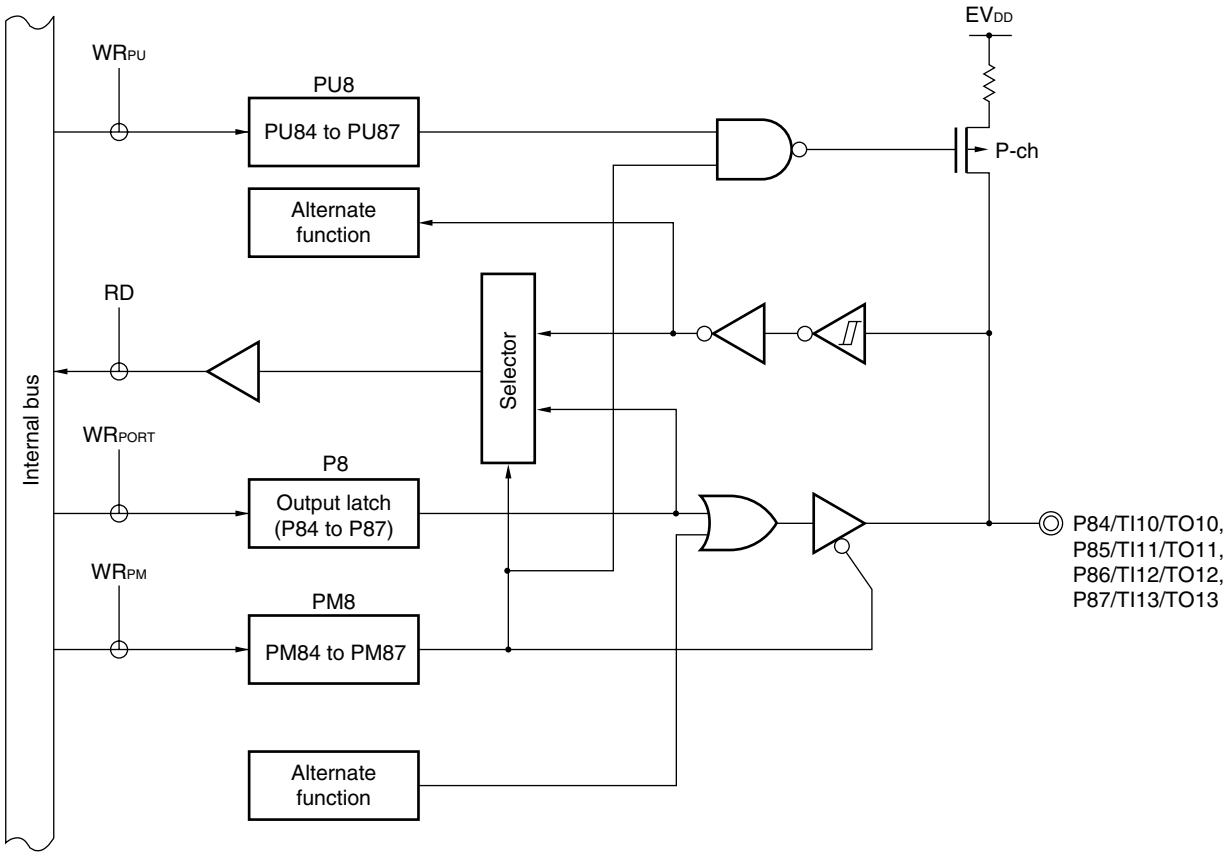
ADPC register	PM2 registers	OAENn bit	ADS register	ANI0/AMP0-/P20, ANI2/AMP0+/P22, ANI3/AMP1-/P23, ANI5/AMP1+/P25, and ANI6/AMP2-/P26 Pins
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	Selects ANI.	Setting prohibited
			Does not select ANI.	Operational amplifier input
	Output mode	–	–	Setting prohibited

Table 4-7. Setting Functions of ANI1/AMP0O/P21, ANI4/AMP1O/P24, and ANI7/AMP2O/P27 Pins

ADPC register	PM2 register	OAENn bit	ADS register	ANI1/AMP0O/P21, ANI4/AMP1O/P24, and ANI7/AMP2O/P27 Pins
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	Selects ANI.	Operational amplifier output (to be converted)
			Does not select ANI.	Operational amplifier output (not to be converted)
	Output mode	–	–	Setting prohibited

Remark 78K0R/LF3: n = 0, 1
78K0R/LG3, 78K0R/LH3: n = 0 to 2

Figure 4-24. Block Diagram of P84 to P87



P8: Port register 8
PU8: Pull-up resistor option register 8
PM8: Port mode register 8
RD: Read signal
WR××: Write signal

Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

3. The microcontroller operates on the 8 MHz internal high-speed oscillation clock if 8 MHz or 20 MHz is selected for the internal high-speed oscillator by using the option byte or on the 1 MHz internal high-speed oscillation clock if 1 MHz is selected.

4. If the internal high-speed oscillator is set to 1 MHz by using the option byte, the 20 MHz internal high-speed oscillation clock cannot be used.

Cautions 1. A voltage stabilization time (about 2.12 to 5.84 ms) is required after the supply voltage reaches 1.61 V (TYP.). If the time for the supply voltage to rise from 1.61 V (TYP.) to 2.07 V (TYP.) is shorter than the voltage stabilization time, reset processing is entered after the voltage stabilization time elapses.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Figure 6-61. Operation Procedure When PWM Function Is Used (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN or TAU1EN bits of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSm register. Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the TMRmn and TMRmp registers of two channels to be used (determines operation mode of channels). An interval (period) value is set to the TDRmn register of the master channel, and a duty factor is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of the TOMn register is set to 1 (combination operation mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmn pin goes into Hi-Z output state. The TOmn default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets TOEmp to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

Remarks 1. 78K0R/LF3:
- m = 0, n = 0, 2, 6, p = n+1, TO00 to TO04, and TO07 pins

2. 78K0R/LG3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins

3. 78K0R/LH3:
- m = 0, n = 0, 2, 4, 6, p = n+1, TO00 to TO07 pins
- m = 1, n = 0, 2, p = n+1, TO10 to TO13 pins

Figure 6-70. Example of Set Contents of Registers
When Multiple PWM Output Function (Slave Channel) Is Used (output two types of PWMs)

(a) Timer mode register mp, mq (TMRmp, TMRmq)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmp	CKSmp			CCSmp	MAS TERmp	STSmp2	STSmp1	STSmp0	CISmp1	CISmp0			MDmp3	MDmp2	MDmp1	MDmp0
	1/0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
TMRmq	CKSmq			CCSmq	MAS TERmq	STSmq2	STSmq1	STSmq0	CISmq1	CISmq0			MDmq3	MDmq2	MDmq1	MDmq0
	1/0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Operation mode of channel p, q
100B: One-count mode

Start trigger during operation
1: Trigger input is valid.

Selection of TImp and TImq pin input edge
00B: Sets 00B because these are not used.

Start trigger selection
100B: Selects INTTMmn of master channel.

Slave/master selection
0: Channel 0 is set as slave channel.

Count clock selection
0: Selects operation clock.

Operation clock selection
0: Selects CKm0 as operation clock of channel p, q.
1: Selects CKm1 as operation clock of channel p, q.
* Make the same setting as master channel.

(b) Timer output register m (TOm)

	Bit q	Bit p
TOm	TOmq	TOmp
	1/0	1/0

0: Outputs 0 from TOmp or TOmq.
1: Outputs 1 from TOmp or TOmq.

(c) Timer output enable register m (TOEm)

	Bit q	Bit p
TOEm	TOEmq	TOEmp
	1/0	1/0

0: Stops the TOmp or TOmq output operation by counting operation.
1: Enables the TOmp or TOmq output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit q	Bit p
TOLm	TOLmq	TOLmp
	1/0	1/0

0: Positive logic output (active-high)
1: Inverted output (active-low)

(e) Timer output mode register m (TOMm)

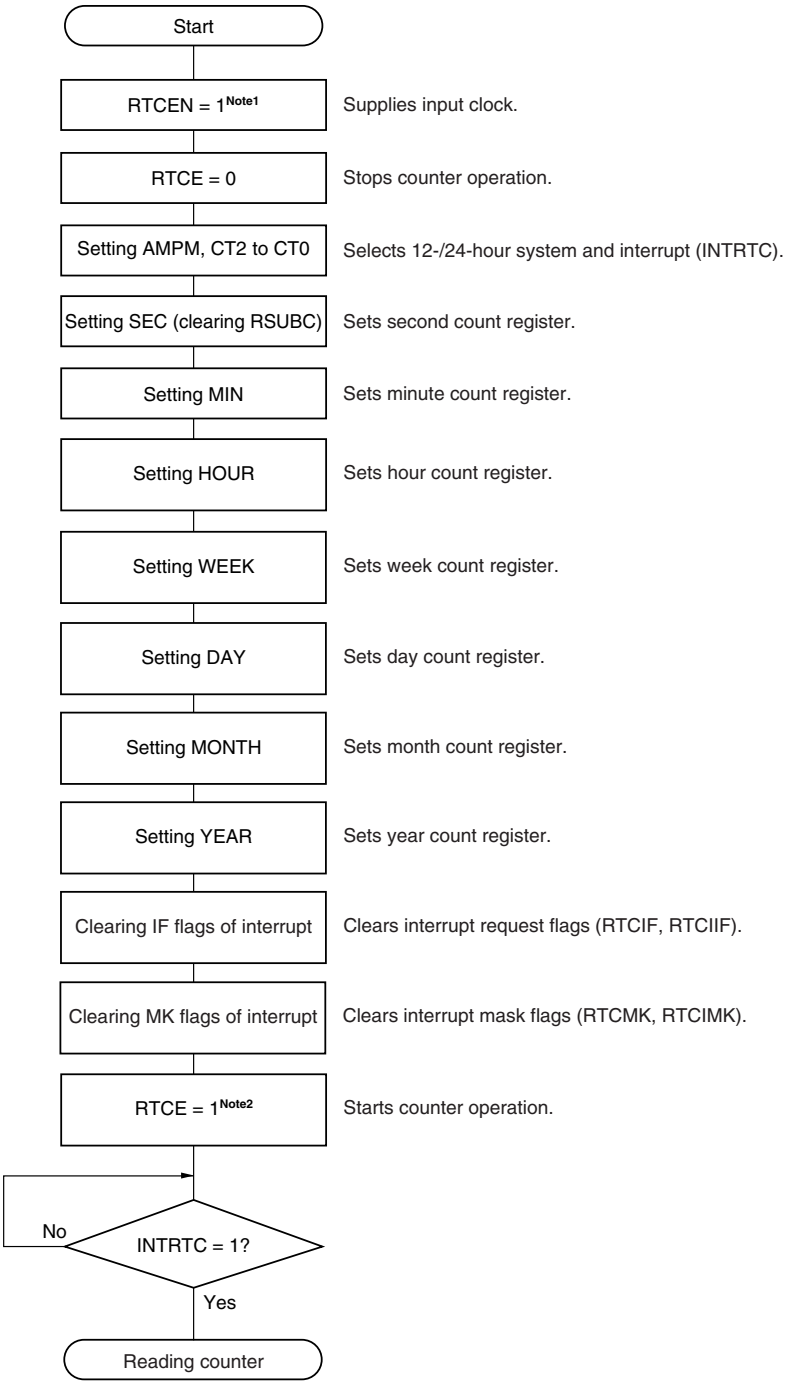
	Bit q	Bit p
TOMm	TOMmq	TOMmp
	1	1

1: Sets the combination operation mode.

7.4 Real-Time Counter Operation

7.4.1 Starting operation of real-time counter

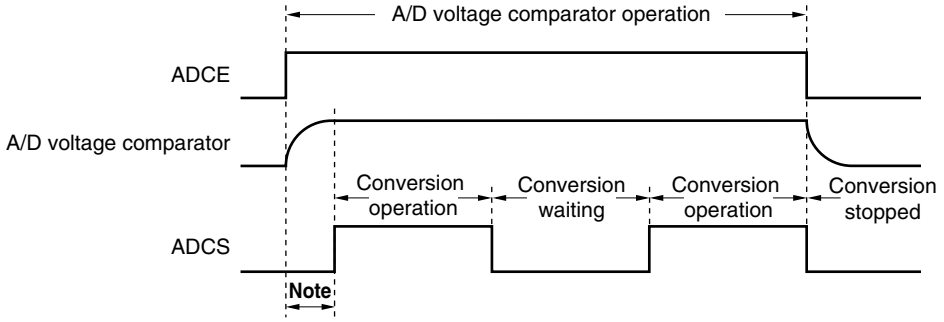
Figure 7-19. Procedure for Starting Operation of Real-Time Counter



Notes 1. First set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

2. Confirm the procedure described in **7.4.2 Shifting to STOP mode after starting operation** when shifting to STOP mode without waiting for INTRTC = 1 after RTCE = 1.

Figure 10-6. Timing Chart When A/D Voltage Comparator Is Used



Note To stabilize the internal circuit, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 μs or longer.

Cautions 1. A/D conversion must be stopped before rewriting bits ADSCM, FR0 to FR2, LV1, and LV0 to values other than the identical data.

2 When using the A/D converter in normal mode 2 (LV1 = 0, LV0 = 1) or low voltage mode (LV1 = 1, LV0 = 0), enable the input gate voltage boost circuit for the A/D converter by using the analog reference voltage control register (ADVRC), and then set ADCE and ADCS to 1. After the voltage boost circuit stabilization time (10 μs) passes after the input gate voltage boost circuit for the A/D converter has been enabled, set ADCS to 1.

14.5.5 Slave reception

Slave reception is that the 78K0R/Lx3 microcontrollers receive data from another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	$\overline{SCK00}$, SI00	$\overline{SCK01}$, SI01	$\overline{SCK10}$, SI10	$\overline{SCK20}$, SI20
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)			
Error detection flag	Overrun error detection flag (OVFmn) only			
Transfer data length	7 or 8 bits			
Transfer rate	Max. f_{MCK}/6 [MHz]Notes 1, 2			
Data phase	Selectable by DAPmn bit • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.			
Clock phase	Selectable by CKPmn bit • CKPmn = 0: Forward • CKPmn = 1: Reverse			
Data direction	MSB or LSB first			

Notes 1. Because the external serial clock input to pins $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, and $\overline{SCK20}$ is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [MHz].

2. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 31 ELECTRICAL SPECIFICATIONS**).

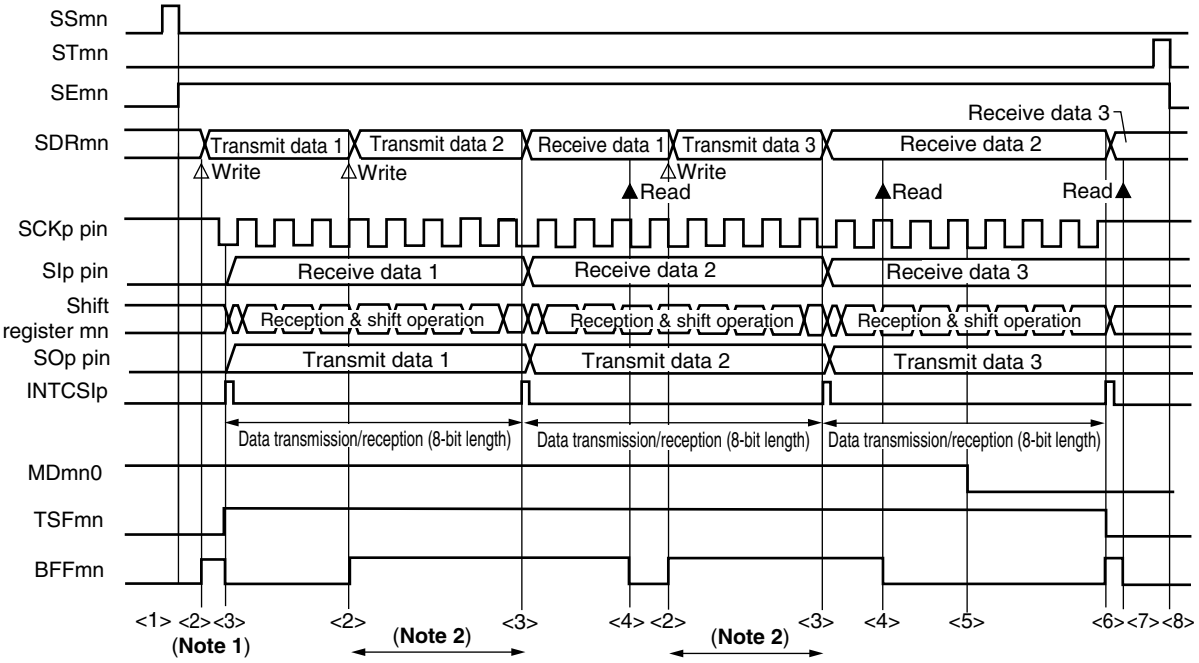
Remarks 1. f_{MCK}: Operation clock (MCK) frequency of target channel

2. For 78K0R/LF3, CSI00 and CSI01 are not mounted.

3. For 78K0R/LG3, CSI01 is not mounted.

(4) Processing flow (in continuous transmission/reception mode)

Figure 14-66. Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Notes 1. When transmit data is written to the SDRmn register while BFFmn = 1, the transmit data is overwritten.

2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

Caution The MDmn0 bit can be rewritten even during operation.
However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-67 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)

14.6.5 Calculating baud rate

(1) Baud rate calculation expression

The baud rate for UART (UART0, UART1, UART2, UART3) communication can be calculated by the following expressions.

(Baud rate) = {Operation clock (MCK) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [bps]

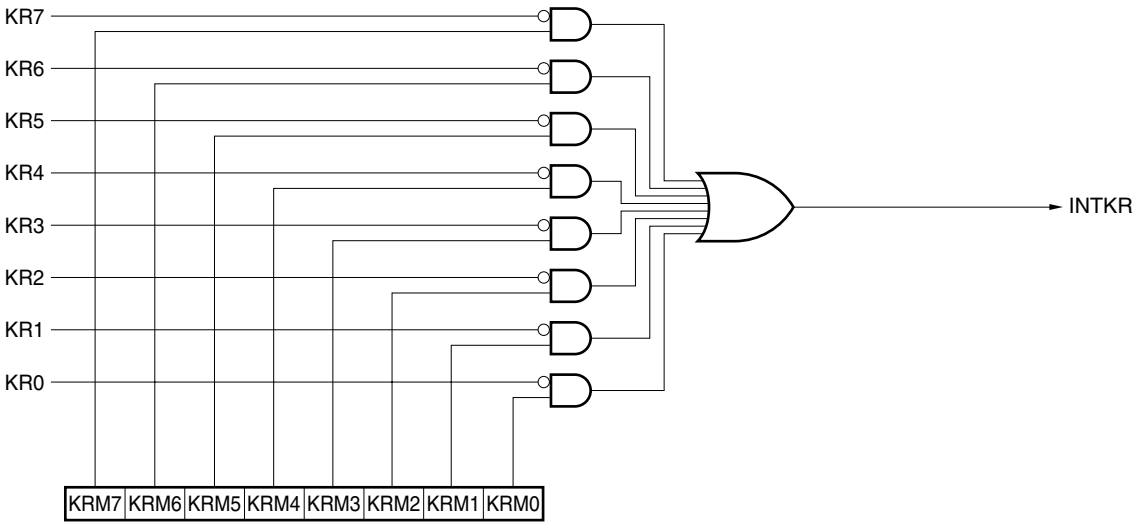
Caution Setting SDRmn [15:9] = (0000000B, 0000001B) is prohibited.

Remarks 1. When UART is used, the value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000010B to 1111111B) and therefore is 2 to 127.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

The operation clock (MCK) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Figure 20-1. Block Diagram of Key Interrupt



20.3 Register Controlling Key Interrupt

(1) Key return mode register (KRM)

This register controls the KRM0 to KRM7 bits using the KR0 to KR7 signals, respectively.

KRM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 20-2. Format of Key Return Mode Register (KRM)

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

Cautions 1. If any of the KRM0 to KRM7 bits used is set to 1, set bits 0 to 7 (PU70 to PU77) of the corresponding pull-up resistor register 7 (PU7) to 1.

2. An interrupt will be generated if the target bit of the KRM register is set while a low level is being input to the key interrupt input pin. To ignore this interrupt, set the KRM register after disabling interrupt servicing by using the interrupt mask flag. Afterward, clear the interrupt request flag and enable interrupt servicing after waiting for the key interrupt input low-level width (250 ns or more).

3. The bits not used in the key interrupt mode can be used as normal ports.

Remark n = 0 to 7

Table 21-1. Operating Statuses in HALT Mode (2/3)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock
			When CPU Is Operating on XT1 Clock (f_{XT})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}	Status before HALT mode was set is retained
		f_X	
		f_{EX}	Operates or stops by external clock input
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Oscillates • WTON = 1 and WDSTBYON = 0: Stops
CPU			Operation stopped
Flash memory			Operation stopped (wait state in low-power consumption mode)
RAM			Status before HALT mode was set is retained at voltage higher than POC detection voltage.
Port (latch)			Status before HALT mode was set is retained
Timer array unit (TAU)			Operable
Real-time counter (RTC)			
Watchdog timer			Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Operates • WTON = 1 and WDSTBYON = 0: Stops
Clock output/buzzer output			Operable
A/D converter			Cannot operate
D/A converter			Operable
Operational amplifier			
Voltage reference			
Serial array unit (SAU)			
Serial interface (IICA)			Cannot operate
LCD controller/driver			Operable
Multiplier/divider			
DMA controller			
Power-on-clear function			
Low-voltage detection function			
External interrupt			
Key interrupt			

Remarks 1. f_{IH}: Internal high-speed oscillation clock, f_{IH20}: 20 MHz internal high-speed oscillation clock
f_X: X1 oscillation clock, f_{EX}: External main system clock
f_{XT}: XT1 oscillation clock, f_{IL}: Internal low-speed oscillation clock

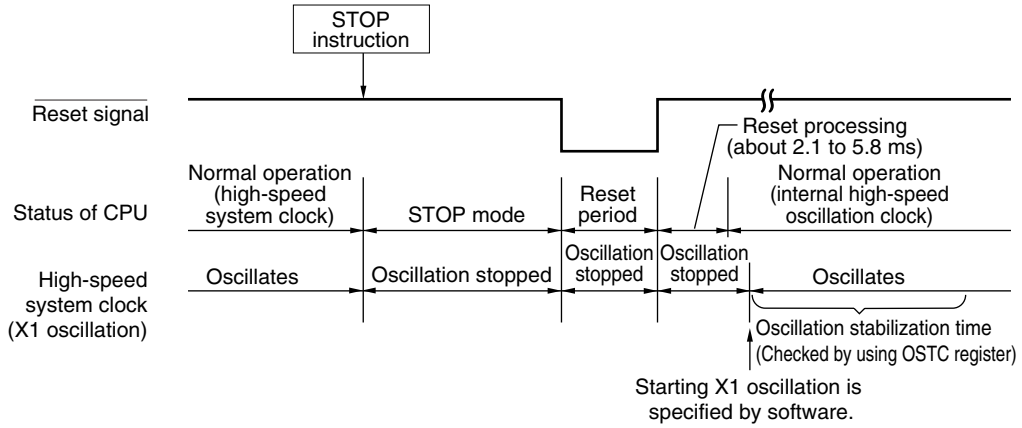
2. The functions mounted depend on the product. Refer to **1.4 Block Diagram** and **1.5 Outline of Functions**.

(b) Release by reset signal generation

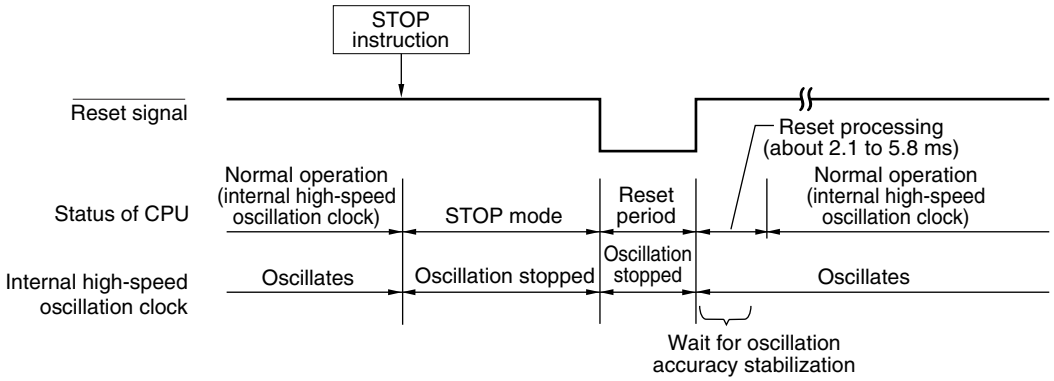
When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 21-7. STOP Mode Release by Reset

(1) When high-speed system clock is used as CPU clock



(2) When internal high-speed oscillation clock is used as CPU clock



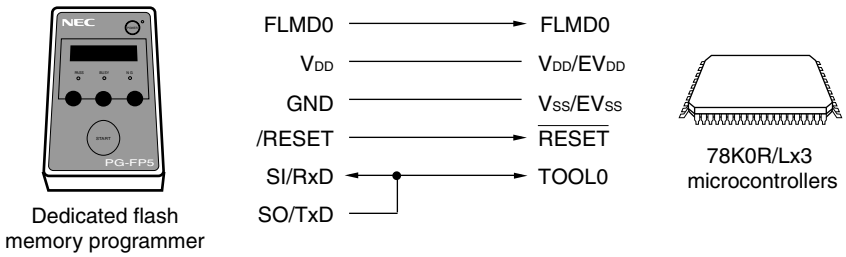
Remark fx: X1 clock oscillation frequency

27.3 Communication Mode

Communication between the dedicated flash memory programmer and the 78K0R/Lx3 microcontrollers is established by serial communication using the TOOL0 pin via a dedicated single-line UART of the 78K0R/Lx3 microcontrollers.

Transfer rate: 115,200 bps to 1,000,000 bps

Figure 27-2. Communication with Dedicated Flash Memory Programmer



When using the FlashPro5 as the dedicated flash memory programmer, the FlashPro5 generates the following signals for the 78K0R/Lx3 microcontrollers. For details, refer to the user's manual for the FlashPro5.

Table 27-1. Pin Connection

FlashPro5			78K0R/Lx3 microcontrollers	Connection
Signal Name	I/O	Pin Function	Pin Name	
FLMD0	Output	Mode signal	FLMD0	◎
V_{DD}	I/O	V_{DD} voltage generation/power monitoring	V_{DD}, EV_{DD}, AV_{DD0}, AV_{DD1}	◎
GND	–	Ground	V_{SS}, EV_{SS}, AV_{SS}	◎
CLK	Output	Clock output	–	×
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎
SI/RxD	Input	Receive signal	TOOL0	◎
SO/TxD	Output	Transmit signal		
SCK	Output	Transfer clock	–	×

Remark ◎: Be sure to connect the pin.
×: The pin does not have to be connected.

DC Characteristics (1/11)

<R> **(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{DD0} ≤ V_{DD}, 1.8 V ≤ AV_{DD1} ≤ V_{DD}, 1.8 V ≤ AV_{DD} ≤ V_{DD}, 1.8 V ≤ EV_{DD1} = V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P02, P10 to P17, P30 to P34, P40, P41, P70 to P77, P80 to P87, P120, P130	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Per pin for P50 to P57, P90 to P97, P100 to P102, P140 to P147	4.0 V ≤ V_{DD} ≤ 5.5 V			–1.6	mA
			2.7 V ≤ V_{DD} < 4.0 V			–0.45	mA
			1.8 V ≤ V_{DD} < 2.7 V			–0.45	mA
		Total of P00 to P02, P10 to P17, P30 to P34, P40, P41, P70 to P77, P80 to P87, P120, P130 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P50 to P57, P90 to P97, P100 to P102, P140 to P147 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–12.8	mA
			2.7 V ≤ V_{DD} < 4.0 V			–3.6	mA
			1.8 V ≤ V_{DD} < 2.7 V			–3.6	mA
		Total of all pins (When duty = 60%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–32.8	mA
			2.7 V ≤ V_{DD} < 4.0 V			–13.6	mA
			1.8 V ≤ V_{DD} < 2.7 V			–8.6	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P152, P157				–0.1	mA
		Per pin for P110, P111				–0.1	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} pin to an output pin.

2. Specification under conditions where the duty factor is 60% or 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
•Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 50% and I_{OH} = –20.0 mA
Total output current of pins = (–20.0 × 0.7)/(50 × 0.01) = –28.0 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10 to P15, P75, P77, P80 and P82 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.