Renesas Electronics America Inc - UPD78F1518AGF-GAT-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1518agf-gat-ax

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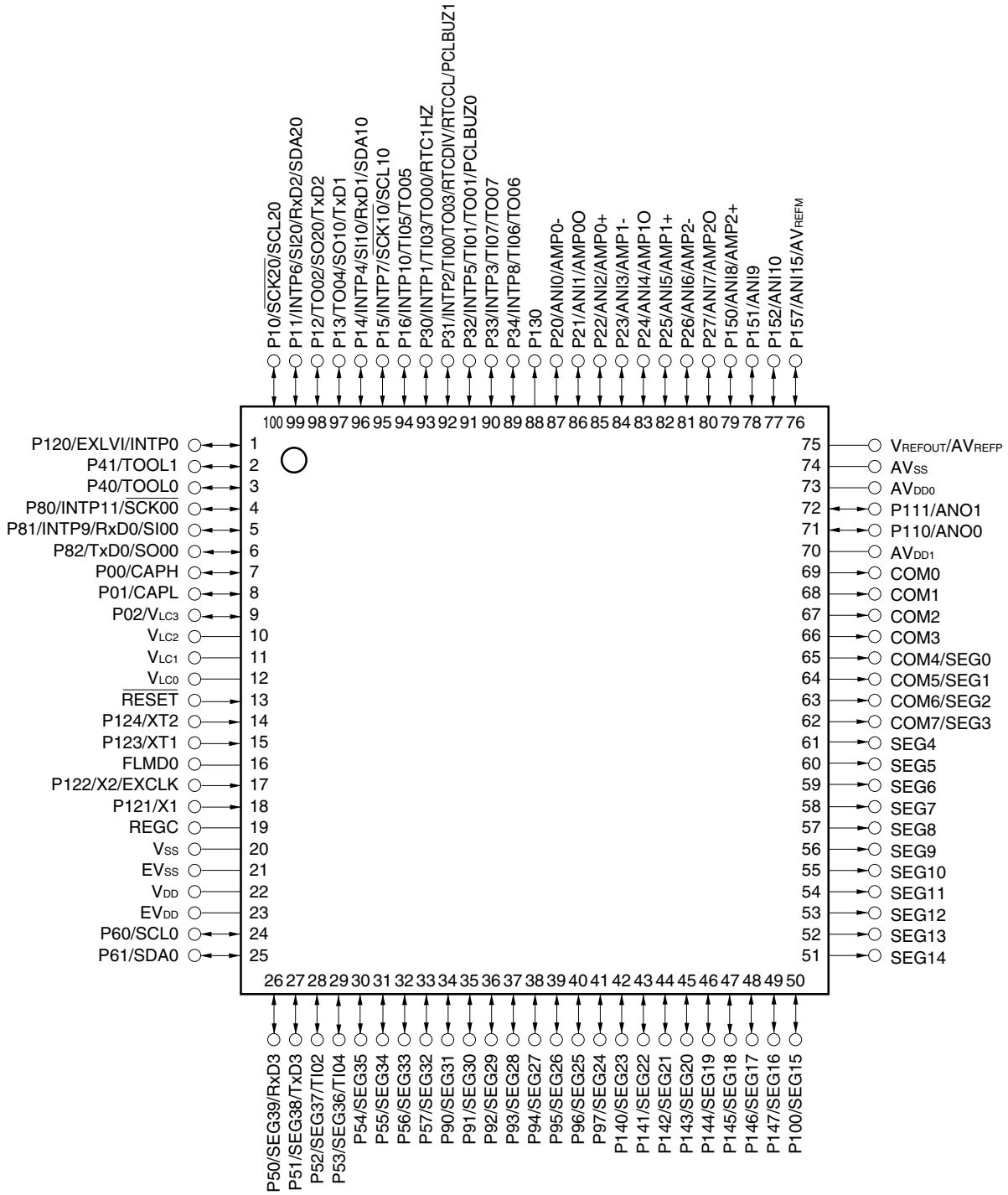
1.3.2 78K0R/LG3

<R> (1) μPD78F150xA

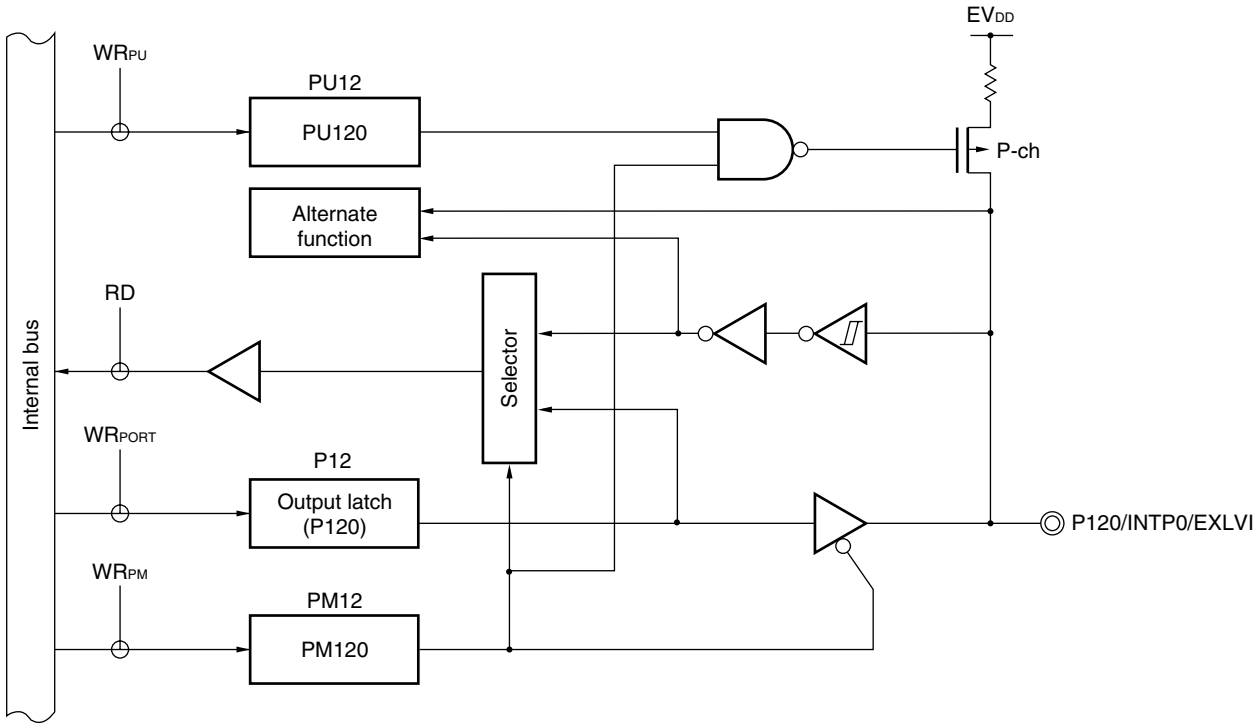
- 100-pin plastic LQFP (fine pitch) (14×14)



Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Figure 4-29. Block Diagram of P120



P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

Caution 1. When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 5-10 and 5-11 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Note that the XT1 oscillator is designed as a low-gain circuit for achieving low-power consumption. Note the following points when designing the XT1 oscillator.

- **The pins and circuit board include parasitic capacitance. Therefore, confirm that there are no problems by performing oscillation evaluation on the circuit board to be actually used.**
- **When low-consumption oscillation or super-low-consumption oscillation is selected, lower power consumption than when selecting normal oscillation can be achieved. However, in this case, the XT1 oscillation margin is reduced, so perform sufficient oscillation evaluation of the resonator to be used for XT1 oscillation before using the resonator.**
- **Keep the wiring length between the XT1 and XT2 pins and resonator as short as possible and parasitic capacitance and wire resistance as small as possible. This is particularly important when super-low-consumption oscillation (AMPHS1 = 1) is selected.**
- **Configure the circuit board by using material with little parasitic capacitance and wire resistance.**
- **Place a ground pattern that has the same potential as V_{SS} (if possible) around the XT1 oscillator.**
- **Do not cross the signal lines between the XT1 and XT2 pins and the resonator with other signal lines. Do not route the signal lines near a signal line through which a high fluctuating current flows.**
- **Moisture absorption by the circuit board and condensation on the board in a highly humid environment may cause the impedance between the XT1 and XT2 pins to drop and disable oscillation. When using the circuit board in such an environment, prevent the circuit board from absorbing moisture by taking measures such as coating the circuit board.**
- **Coat the surface of the circuit board by using material that does not generate capacitance or leakage between the XT1 and XT2 pins.**

Figure 5-12 shows examples of incorrect resonator connection.

6.2 Configuration of Timer Array Unit

The timer array unit includes the following hardware.

Table 6-1. Configuration of Timer Array Unit

Item	Configuration
Timer/counter	Timer counter register mn (TCRmn)
Register	Timer data register mn (TDRmn)
Timer input	TIpq pin, RxD3 pin (for LIN-bus)
Timer output	TOpq pins, output controller
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Timer clock select register m (TPSm) • Timer channel enable status register m (TEm) • Timer channel start register m (TSm) • Timer channel stop register m (TTm) • Timer input select registers 0, 1 (TIS0, TIS1) • Timer output enable register p (TOEp) • Timer output register p (TOp) • Timer output level register p (TOLp) • Timer output mode register p (TOMp)
	<Registers of each channel> • Timer mode register mn (TMRmn) • Timer status register pq (TSRpq) • Input switch control register (ISC) (channel 7 of timer array unit 0 only) • Noise filter enable registers 1, 2 (NFEN1, NFEN2) • Port mode registers 1, 3, 5, 8 (PM1, PM3, PM5, PM8) • Port registers 1, 3, 5, 8 (P1, P3, P5, P8)

Remark mn: Unit number + Channel number, pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 0, pq = 00 to 04, 07
78K0R/LG3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 0, pq = 00 to 07
78K0R/LH3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 0, 1, pq = 00 to 07, 10 to 13

Figures 6-1 and 6-2 show block diagrams.

Figure 6-39. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (1/3)

(1) When CKm0 or CKm1 is selected as count clock

(a) Timer mode register mn (TMRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKSmn			CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0			MDmn3	MDmn2	MDmn1	MDmn0
	1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0

Operation mode of channel n
000B: Interval timer

Setting of operation when counting is started
0: Neither generates INTTMmn nor inverts timer output when counting is started.
1: Generates INTTMmn and inverts timer output when counting is started.

Selection of edge of timer input
00B: Sets 00B because these are not used.

Start trigger selection
000B: Selects only software start.

Slave/master selection
0: Cleared to 0 when independent function is selected.

Count clock selection
0: Selects operation clock.

Operation clock selection
0: Selects CKm0 as operation clock of channel n.
1: Selects CKm1 as operation clock of channel n.

(b) Timer output register p (TOp)

	Bit q
TOp	TOpq
	1/0

0: Outputs 0 from TOpq.
1: Outputs 1 from TOpq.

(c) Timer output enable register p (TOEp)

	Bit q
TOEp	TOEpq
	1/0

0: Stops the TOpq output operation by counting operation.
1: Enables the TOpq output operation by counting operation.

(d) Timer output level register p (TOLp)

	Bit q
TOLp	TOLpq
	0

0: Cleared to 0 when TOMpq = 0 (toggle mode)

(e) Timer output mode register p (TOMp)

	Bit q
TOMp	TOMpq
	0

0: Sets toggle mode.

Remark mn: Unit number + Channel number, pq: Unit number + Channel number (only for channels provided with timer I/O pins)
78K0R/LF3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 04, 07
78K0R/LG3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 07
78K0R/LH3: m = 0, 1, mn = 00 to 07, 10 to 13, pq = 00 to 07, 10 to 13

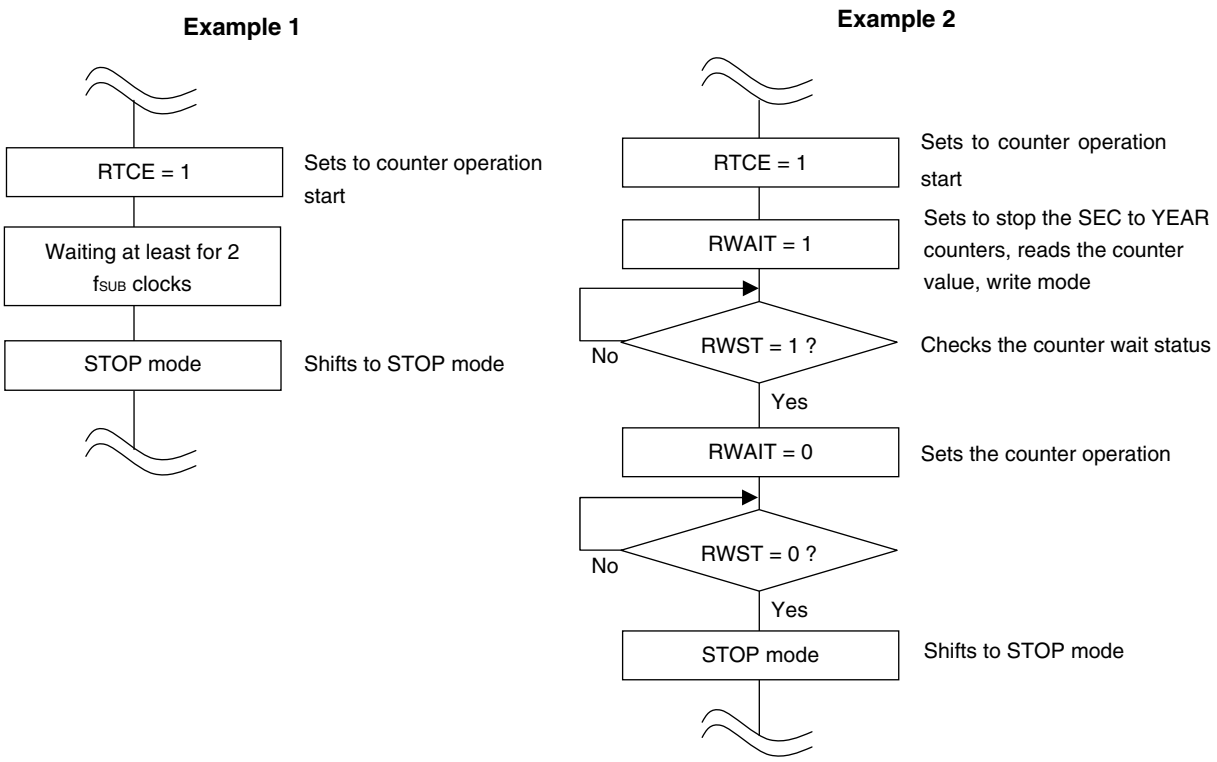
7.4.2 Shifting to STOP mode after starting operation

Perform one of the following processing when shifting to STOP mode immediately after setting RTCE to 1.

However, after setting RTCE to 1, this processing is not required when shifting to STOP mode after the first INTRTC interrupt has occurred.

- Shifting to STOP mode when at least two subsystem clocks (f_{SUB}) (about 62 μs) have elapsed after setting RTCE to 1 (see **Figure 7-20**, **Example 1**).
- Checking by polling RWST to become 1, after setting RTCE to 1 and then setting RWAIT to 1. Afterward, setting RWAIT to 0 and shifting to STOP mode after checking again by polling that RWST has become 0 (see **Figure 7-20**, **Example 2**).

Figure 7-20. Procedure for Shifting to STOP Mode After Setting RTCE to 1



Caution When an operational amplifier is used, AMPn+, AMPn–, and AMPnO pins are used, so the alternative analog input functions cannot be used. The operational amplifier output signals, however, can be used as analog inputs.

Table 12-4. Setting Functions of ANI9/P151 and ANI10/AM152 Pins

ADPC register	PM15 register	ADS register	ANI9/P151 and ANI10/AM152 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	–	Setting prohibited

Remark 78K0R/LF3: ANI9/P151 and ANI10/AM152 are not mounted.
78K0R/LG3, 78K0R/LH3: ANI9/P151, ANI10/AM152

Table 12-5. Setting Functions of ANI15/AV$_{REFM}$/P157 Pin

ADPC register	PM15 register	ADREF bit	ADS register	ANI15/AV$_{REFM}$/P157 Pin
Digital I/O selection	Input mode	0	–	Digital input
		1	–	Setting prohibited
	Output mode	0	–	Digital output
		1	–	Setting prohibited
Analog input selection	Input mode	0	Selects ANI.	Analog input (to be converted)
			Does not select ANI.	Analog input (not to be converted)
		1	–	Negative reference voltage input of A/D converter
	Output mode	–	–	Setting prohibited

14.7.2 Data transmission

Data transmission is an operation to transmit data to the target for transfer (slave) after transmission of an address field. After all data are transmitted to the slave, a stop condition is generated and the bus is released.

Simplified I^2C	IIC10	IIC20
Target channel	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL10, SDA10 Note	SCL20, SDA20 Note
Interrupt	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)	
Error detection flag	Parity error detection flag (PEFmn)	
Transfer data length	8 bits	
Transfer rate	Max. f_{CLK}/4 [MHz] (SDRmn [15:9] = 1 or more) f_{CLK}: System clock frequency However, the following condition must be satisfied in each mode of I^2C. • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)	
Data level	Forward output (default: high level)	
Parity bit	No parity bit	
Stop bit	Appending 1 bit (for ACK reception timing)	
Data direction	MSB first	

Note To perform communication via simplified I^2C, set the data I/O pins (SDA10, SDA20) in the N-ch open-drain output (V_{DD} tolerance) mode (POM14 = 1, POM11 = 1) by using the port output mode register 1 (POM1) (see **4.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM15 = 1, POM10 = 1) also for the clock input/output pins (SCL10, SCL20) (see **4.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

Table 14-9. Relationship between register settings and pins
(Channel 0 of unit 1: CSI20, UART2 transmission, IIC20)

SE10 Note1	MD102	MD101	SOE10	SO10	CKO10	TXE10	RXE10	PM10	P10	PM11 Note2	P11 Note2	PM12	P12	Operation mode	Pin Function		
															$\overline{SCK20}$/SCL20/P10	SI20/SDA20/RxD2/INTP6/P11 Note2	SO20/TxD2/TO02/P12
0	0	0	0	1	1	0	0	× Note3	× Note3	× Note3	× Note3	× Note3	× Note3	Operation stop mode	P10	INTP6/P11	TO02/P12
	0	1														RxD2/INTP6/P11	
	1	0														INTP6/P11	
1	0	0	0	1	1	0	1	1	×	1	×	× Note3	× Note3	Slave CSI20 reception	$\overline{SCK20}$ (input)	SI20	TO02/P12
			1	0/1 Note4	1	1	0	1	×	× Note3	× Note3	0	1	Slave CSI20 transmission	$\overline{SCK20}$ (input)	INTP6/P11	SO20
			1	0/1 Note4	1	1	1	1	×	1	×	0	1	Slave CSI20 transmission/reception	$\overline{SCK20}$ (input)	SI20	SO20
			0	1	0/1 Note4	0	1	0	1	1	×	× Note3	× Note3	Master CSI20 reception	$\overline{SCK20}$ (output)	SI20	TO02/P12
			1	0/1 Note4	0/1 Note4	1	0	0	1	× Note3	× Note3	0	1	Master CSI20 transmission	$\overline{SCK20}$ (output)	INTP6/P11	SO20
			1	0/1 Note4	0/1 Note4	1	1	0	1	1	×	0	1	Master CSI20 transmission/reception	$\overline{SCK20}$ (output)	SI20	SO20
	0	1	1	0/1 Note4	1	1	0	× Note3	× Note3	× Note3	× Note3	0	1	UART2 transmission Note5	P10	RxD2/INTP6/P11	TxD2
0	1	0	0	0/1 Note6	0/1 Note6	0	0	0	1	0	1	× Note3	× Note3	IIC20 start condition	SCL20	SDA20	TO02/P12
						1	0										
						0	1										
1			1	0/1 Note4	0/1 Note4	1	0	0	1	0	1	× Note3	× Note3	IIC20 address field transmission	SCL20	SDA20	TO02/P12
			1	0/1 Note4	0/1 Note4	1	0	0	1	0	1	× Note3	× Note3	IIC20 data transmission	SCL20	SDA20	TO02/P12
			1	0/1 Note4	0/1 Note4	0	1	0	1	0	1	× Note3	× Note3	IIC20 data reception	SCL20	SDA20	TO02/P12
0			0	0/1 Note7	0/1 Note7	0	0	0	1	0	1	× Note3	× Note3	IIC20 stop condition	SCL20	SDA20	TO02/P12
						1	0										
						0	1										

Notes 1. The SE1 register is a read-only status register which is set using the SS1 and ST1 registers.

2. When channel 1 of unit 1 is set to UART2 reception, this pin becomes an RxD2 function pin (refer to **Table 14-10**). In this case, operation stop mode or UART2 transmission must be selected for channel 0 of unit 1.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART2 transmission and reception in a pair, set channel 1 of unit 1 to UART2 reception (refer to **Table 14-10**).

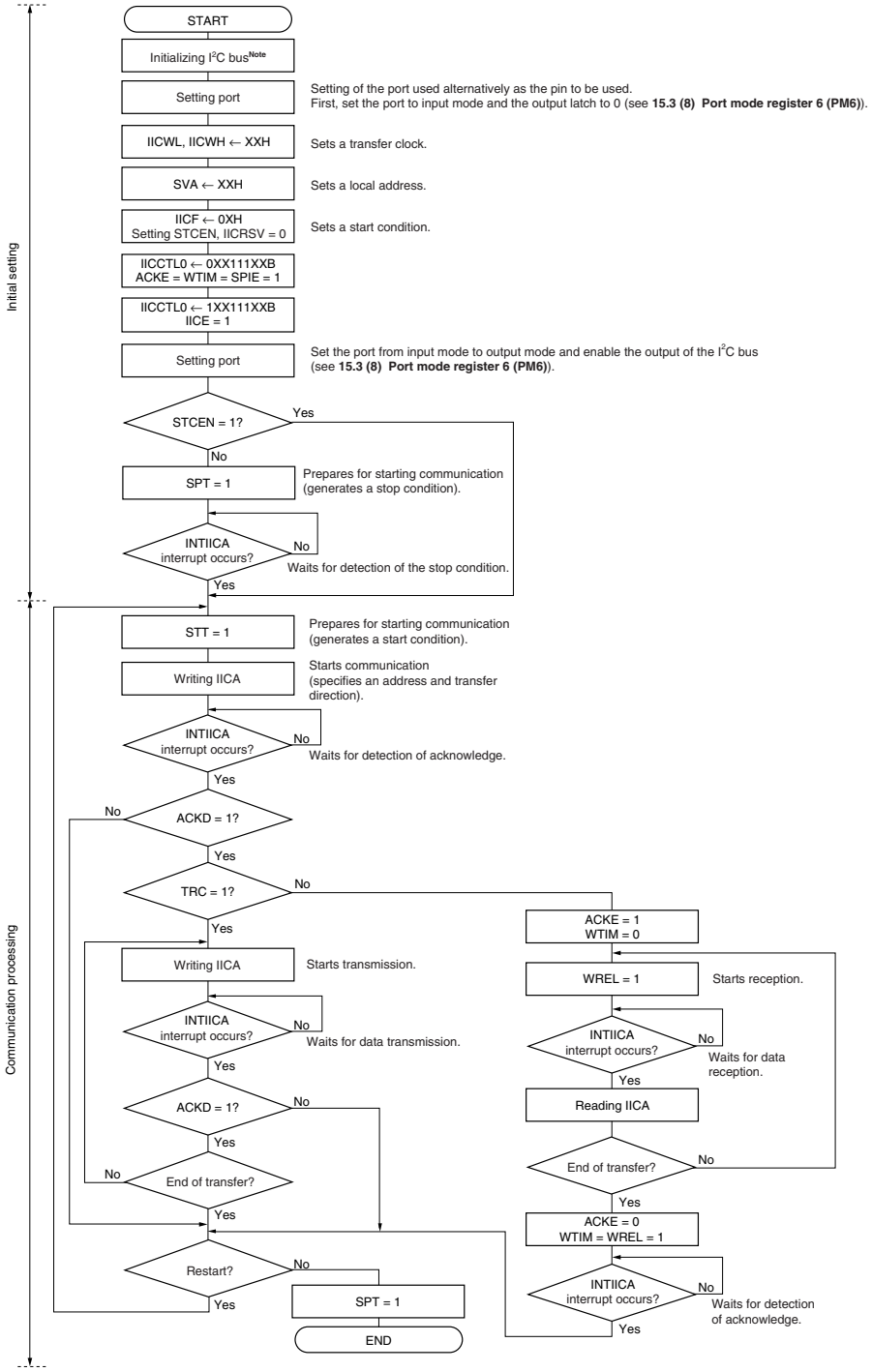
6. Set the CKO10 bit to 1 before a start condition is generated. Clear the SO10 bit from 1 to 0 when the start condition is generated.

7. Set the CKO10 bit to 1 before a stop condition is generated. Clear the SO10 bit from 0 to 1 when the stop condition is generated.

Remark X: Don't care

(1) Master operation in single-master system

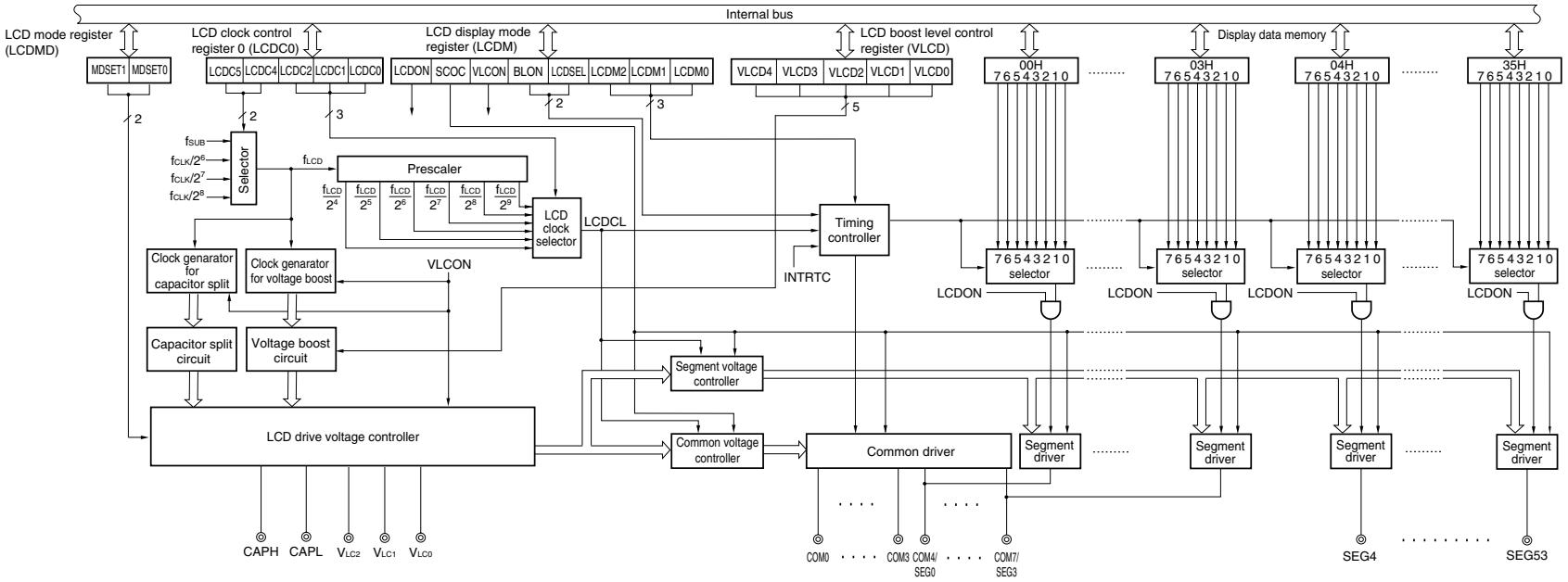
Figure 15-28. Master Operation in Single-Master System



Note Release (SCL0 and SDA0 pins = high level) the I²C bus in conformance with the specifications of the product that is communicating. If EEPROM is outputting a low level to the SDA0 pin, for example, set the SCL0 pin in the output port mode, and output a clock pulse from the output port until the SDA0 pin is constantly at high level.

Remark Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

Figure 16-1. Block Diagram of LCD Controller/Driver



Remark 78K0R/LF3: 31 segment signals (SEG0 to SEG30), 8 common signals (COM0 to COM7)
78K0R/LG3: 40 segment signals (SEG0 to SEG39), 8 common signals (COM0 to COM7)
78K0R/LH3: 54 segment signals (SEG0 to SEG53), 8 common signals (COM0 to COM7)

Cautions 1. Bits 3, 6, and 7 must be set to 0.

2. Set the LCD clock (LCDCL) to no more than 512 Hz when the internal voltage boost method has been set.

Remark f_{CLK}: CPU/Peripheral hardware clock frequency

f_{SUB}: Subsystem clock frequency

(4) LCD boost level control register (VLCD)

This register is used to select the reference voltage that is to be generated when operating the voltage boost circuit (contrast adjustment). The reference voltage can be selected from 20 stages.

VLCD is set using an 8-bit memory manipulation instruction.

Reset signal generation sets VLCD to 0FH.

Figure 16-5. Format of LCD Boost Level Control Register (VLCD)

Address: FFF43H After reset: 0FH R/W

Symbol	7	6	5	4	3	2	1	0
VLCD	0	0	0	VLCD4	VLCD3	VLCD2	VLCD1	VLCD0

VLCD4	VLCD3	VLCD2	VLCD1	VLCD0	Reference voltage selection (contrast adjustment)	V_{LC0} voltage	
						1/3 bias	1/4 bias
0	0	0	0	0	1.75 V	5.25 V	Setting prohibited [Note]
0	0	0	0	1	1.70 V	5.10 V	
0	0	0	1	0	1.65 V	4.95 V	
0	0	0	1	1	1.60 V	4.80 V	
0	0	1	0	0	1.55 V	4.65 V	
0	0	1	0	1	1.50 V	4.50 V	
0	0	1	1	0	1.45 V	4.35 V	
0	0	1	1	1	1.40 V	4.20 V	
0	1	0	0	0	1.35 V	4.05 V	
0	1	0	0	1	1.30 V	3.90 V	5.20 V
0	1	0	1	0	1.25 V	3.75 V	5.00 V
0	1	0	1	1	1.20 V	3.60 V	4.80 V
0	1	1	0	0	1.15 V	3.45 V	4.60 V
0	1	1	0	1	1.10 V	3.30 V	4.40 V
0	1	1	1	0	1.05 V	3.15 V	4.20 V
0	1	1	1	1	1.00 V (default)	3.00 V	4.00 V
1	0	0	0	0	0.95 V	2.85 V	3.80 V
1	0	0	0	1	0.90 V	2.70 V	3.60 V
1	0	0	1	0	0.85 V	2.55 V	3.40 V
1	0	0	1	1	0.80 V	2.40 V	3.20 V
Other than above					Setting prohibited		

Note These settings are prohibited because $V_{LC0} > 5.5$ V.

Figure 19-10. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (78K0R/LH3) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	SREPR00	CSIPR001 SRPR00	CSIPR000 STPR00	DMAPR01	DMAPR00	SREPR03	SRPR03	STPR03

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	SREPR10	CSIPR101 SRPR10	CSIPR100 STPR10	DMAPR11	DMAPR10	SREPR13	SRPR13	STPR13

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	IICAPR0	SREPR01	SRPR01	CSIPR010 IICPR010 STPR01

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	IICAPR1	SREPR11	SRPR11	CSIPR110 IICPR110 STPR11

23.4 Cautions for Power-on-Clear Circuit

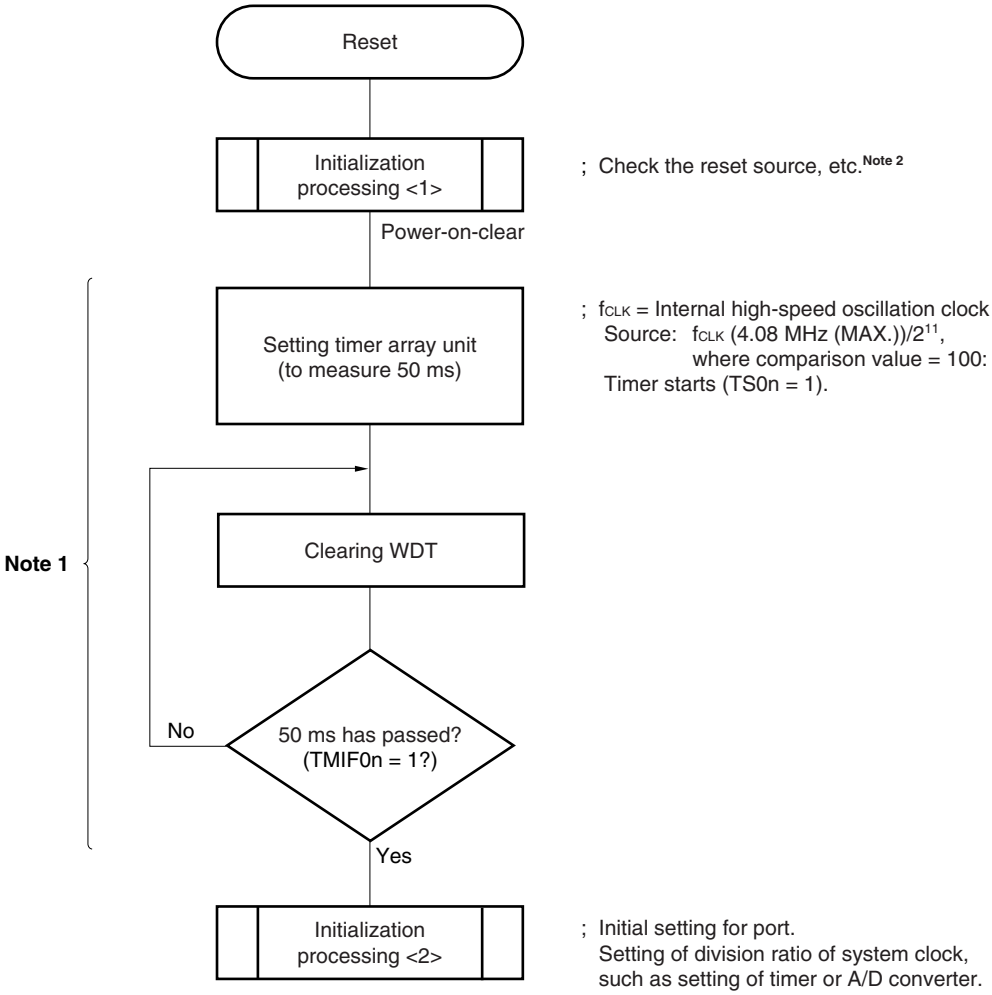
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POR}, V_{PDR}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 23-3. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of POC detection voltage



Notes 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

Remark n = 0 to 7

(2) When detecting level of input voltage from external input pin (EXLVI)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 1 (detects level of input voltage from external input pin (EXLVI)).
    Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <4> Use software to wait for the following periods of time (Total 210 μs).
    - Operation stabilization time (10 μs (MAX.))
    - Minimum pulse width (200 μs (MIN.))
  - <5> Confirm that "input voltage from external input pin (EXLVI) $\geq$ detection voltage (V_{EXLVI} = 1.21 V (TYP.))" when detecting the falling edge of EXLVI, or "input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI} = 1.21 V (TYP.))" when detecting the rising edge of EXLVI, at bit 0 (LVIF) of LVIM.
  - <6> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <7> Release the interrupt mask flag of LVI (LVIMK).
  - <8> Execute the EI instruction (when vector interrupts are used).

  Figure 24-10 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <7> above.

  Caution Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

- When stopping operation
  Be sure to clear (0) LVION by using a 1-bit memory manipulation instruction.

29.3 BCD Correction Circuit Operation

The basic operation of the BCD correction circuit is as follows.

(1) Addition: Calculating the result of adding a BCD code value and another BCD code value by using a BCD code value

<1> The BCD code value to which addition is performed is stored in the A register.

<2> By adding the value of the A register and the second operand (value of one more BCD code to be added) as are in binary, the binary operation result is stored in the A register and the correction value is stored in the BCDADJ register.

<3> Decimal correction is performed by adding in binary the value of the A register (addition result in binary) and the BCDADJ register (correction value), and the correction result is stored in the A register and CY register.

Caution The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Examples 1: 99 + 89 = 188

Instruction	A Register	CY Register	AC Flag	BCDADJ Register
`MOV A, #99H ; <1>`	99H	–	–	–
`ADD A, #89H ; <2>`	22H	1	1	66H
`ADD A, !BCDADJ ; <3>`	88H	1	0	–

Examples 2: 85 + 15 = 100

Instruction	A Register	CY Register	AC Flag	BCDADJ Register
`MOV A, #85H ; <1>`	85H	–	–	–
`ADD A, #15H ; <2>`	9AH	0	0	66H
`ADD A, !BCDADJ ; <3>`	00H	1	1	–

Examples 3: 80 + 80 = 160

Instruction	A Register	CY Register	AC Flag	BCDADJ Register
`MOV A, #80H ; <1>`	80H	–	–	–
`ADD A, #80H ; <2>`	00H	1	0	60H
`ADD A, !BCDADJ ; <3>`	60H	1	0	–

LCD Characteristics (4/4)

(3) Capacitor split method

- **1/3 bias method (T_A = –40 to +85°C, 2.2 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{LC0} voltage	V_{LC0}	C1 to C4 = 0.47 μF[Note 3]		V_{DD}		V
V_{LC1} voltage	V_{LC1}	C1 to C4 = 0.47 μF[Note 3]	2/3 V_{LC0} –0.1	2/3 V_{LC0}	2/3 V_{LC0} +0.1	V
V_{LC2} voltage	V_{LC2}	C1 to C4 = 0.47 μF[Note 3]	1/3 V_{LC0} –0.1	1/3 V_{LC0}	1/3 V_{LC0} +0.1	V
Capacitor split wait time[Note 1]	t_{VAWAIT}		100			ms
LCD output resistor[Note 2] (Common)	R_{ODC}	I_O = ±5 μA			40	kΩ
LCD output resistor[Note 2] (Segment)	R_{OCS}	I_O = ±1 μA			200	kΩ

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. The output resistor is a resistor connected between one of the V_{LC0}, V_{LC1}, V_{LC2} and V_{SS} pins, and either of the SEG and COM pins.

3. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{LC0} and GND
C3: A capacitor connected between V_{LC1} and GND
C4: A capacitor connected between V_{LC2} and GND
C1 = C2 = C3 = C4 = 0.47 pF±30 %

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 5	Soft	Subsystem clock control	XT1/P123, XT2/P124	The XT1/P123 and XT2/P124 pins are in the input port mode after a reset release.	p.237 ☐
	Hard		Subsystem clock	When the subsystem clock is used as the CPU clock, the subsystem clock is also supplied to the peripheral hardware (except the real-time counter, timer array unit (when f_{SUB}/2, f_{SUB}/4, the valid edge of TI0mn input, or the valid edge of INTRTCI is selected as the count clock), clock output/buzzer output, and watchdog timer). At this time, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 31 ELECTRICAL SPECIFICATIONS.	pp.237, 238 ☐
	Soft			The CMC register can be written only once after reset release, by an 8-bit memory manipulation instruction. Therefore, it is necessary to also set the value of the EXCLK and OSCSEL bits at the same time. For EXCLK and OSCSEL bits, see 5.6.1 (1) Example of setting procedure when oscillating the X1 clock or 5.6.1 (2) Example of setting procedure when using the external main system clock.	p.238 ☐
				Be sure to confirm that CLS = 0 when setting XTSTOP to 1. In addition, stop the peripheral hardware if it is operating on the subsystem clock.	p.238 ☐
				The subsystem clock oscillation cannot be stopped using the STOP instruction.	p.238 ☐
		CPU clock status transition	–	Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 31 ELECTRICAL SPECIFICATIONS).	pp.241, 242, 245 ☐
Chapter 6	Soft	Timer array unit	–	Channel 5 of timer array unit 0 of the 78K0R/LF3 can be used only as an interval timer.	p.251 ☐
				Channel 6 of timer array unit 0 of the 78K0R/LF3 can be used only as an interval timer, for PWM output (master channel), and for one-shot pulse output (master channel when software trigger start is selected).	p.251 ☐
				Channels 0 to 3 of timer array unit 1 of the 78K0R/LF3 and 78K0R/LG3 can be used only as interval timers.	p.251 ☐
				Channels 1, 5 to 7 of timer array unit 0 and channels 0 to 3 of timer array unit 1 cannot be used as frequency dividers.	p.251 ☐
			TCRmn: Timer/counter register mn	The count value is not captured to TDRmn even when TCRmn is read.	p.255 ☐
			TDRmn: Timer data register mn	TDRmn does not perform a capture operation even if a capture trigger is input, when it is set to the compare function.	p.260 ☐
			PER0: Peripheral enable register 0	When setting the timer array unit, be sure to set TAUmEN to 1 first. If TAUmEN = 0, writing to a control register of the timer array unit is ignored, and all read values are default values.	p.262 ☐
			TPSm: Timer clock select register m	Be sure to clear bits 15 to 8 to “0”.	p.268 ☐

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Edition	Description	Chapter
3rd Edition	Modification of and addition of **Note** to **Figure 14-98 Timing Chart of Stop Condition Generation**	CHAPTER 14 SERIAL ARRAY UNIT (continuation)
	Addition of **Caution** to **14.7.5 Calculating transfer rate**	
	Modification of **Note 2** in **Table 14-4 Selection of operation clock**	
	Addition of **Caution 3** to **Figure 15-3 Format of IICA Shift Register (IICA)**	CHAPTER 15 SERIAL INTERFACE IICA
	Modification of description in **15.2 (2) Slave address register (SVA)**	
	Modification of description in **Figure 15-4 Format of Slave Address Register (SVA)**	
	Addition of **Note 3** to and modification of **Caution** in **Figure 15-6 Format of IICA Control Register 0 (IICCTL0) (1/4)**	
	Addition of description to **Figure 15-6 Format of IICA Control Register 0 (IICCTL0) (2/4)**	
	Modification of description in **Figure 15-6 Format of IICA Control Register 0 (IICCTL0) (3/4)**	
	Addition of description to **Figure 15-9 Format of IICA Control Register 1 (IICCTL1) (1/2)**	
	Modification of **15.4.2 (1) Setting transfer clock on master side**	
	Modification of **Figure 15-23 Flow When Setting WUP = 0 upon Address Match (Including Extension Code Reception)**	
	Modification of **Figure 15-24 When Operating as Master Device after Releasing STOP Mode other than by INTIICA** and deletion of **Figure 15-25 When Operating as Slave Device after Releasing STOP Mode other than by INTIICA (When Not Required to Operate as Master Device)** in old edition	
	Modification of **15.5.14 (1) When communication reservation function is enabled (bit 0 (IICRSV) of IICA flag register (IICF) = 0)**	
	Modification of **Note 1** in **Figure 15-27 Communication Reservation Protocol**	
	Modification of **Note** in **Figure 15-29 Master Operation in Multi-Master System (2/3)**	
	Modification of **Figure 16-1 Block Diagram of LCD Controller/Driver**	CHAPTER 16 LCD CONTROLLER/DRIVER
	Addition of **Caution 4** to and modification of **Caution 5** in **Figure 16-3 Format of LCD Display Mode Register**	
	Modification of **Figure 16-4 Format of LCD Clock Control Register**	
	Addition of **Caution 5** to and modification of **Figure 16-5 Format of LCD boost level control register (VLCD)**	
	Addition of **<8>** to **16.5 (2) Internal voltage boosting method**	
	Addition of Caution to **Figure 16-31 Examples of LCD Drive Power Connections (External Resistance Division Method)**	
	Modification of description in **19.2 Interrupt Sources and Configuration**	CHAPTER 19 INTERRUPT FUNCTIONS
	Modification of **Table 21-2 Operating Statuses in STOP Mode**	CHAPTER 21 STANDBY FUNCTION
	Modification of **Caution 1**	CHAPTER 22 RESET FUNCTION
	Modification of **Figure 22-1 Block Diagram of Reset Function**	
	Modification of **Table 22-1 Operation Statuses During Reset Period**	
	Modification of **Table 22-2 Hardware Statuses After Reset Acknowledgment**	
	Modification of **22.1 Register for Confirming Reset Source**	
	Modification of and addition of **Caution 2** to **Figure 22-5 Format of Reset Control Flag Register (RESF)**	