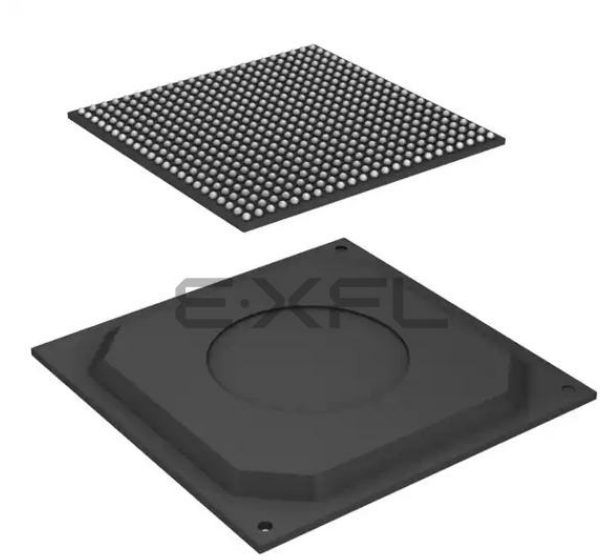

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	200MHz, 800MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, LVDS
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.15V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SNVS, System JTAG, TVDECODE
Package / Case	529-LFBGA
Supplier Device Package	529-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6x4avm08ac

4.1.2.2 17x17 mm NP (VO) and 17x17 mm WP (VN) Package Thermal Resistance

Table 8 displays the 17x17 mm NP (VO) and 17x17 mm WP (VN) package thermal resistance data.

Table 8. 17x17 mm NP (VO) and 17x17 mm WP (VN) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single-layer board (1s)	$R_{\theta JA}$	44.4	°C/W	1,2
Junction to Ambient Natural Convection	Four-layer board (2s2p)	$R_{\theta JA}$	27.4	°C/W	1,2,3
Junction to Ambient (@ 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	35.2	°C/W	1,3
Junction to Ambient (@ 200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	22.5	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	13.2	°C/W	4
Junction to Case	—	$R_{\theta JC}$	8.4	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB}	8.6	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Table 27. LPDDR2 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
Keeper Circuit Resistance	Rkeep	—	110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	μA

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.4.2 DDR3/DDR3L Mode I/O DC Parameters

For details on supported DDR memory configurations, see Section 4.10, "Multi-mode DDR Controller (MMDC). The parameters in Table 28 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 28. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for DSE=001)	0.8*OVDD[1]	—	V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for DSE=001)	0.2*OVDD	V	—
High-level output voltage	VOH	Ioh= -1mA Voh (for all except DSE=001)	0.8*OVDD		V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except DSE=001)	0.2*OVDD	V	—
Input Reference Voltage	Vref	—	0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC	—	Vref[2]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.1	V
Differential Input Logic High	Vih_diff	—	0.2	See Note[3]	V
Differential Input Logic Low	Vil_diff	—	See Note[3]	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

2 Vref – DDR3/DDR3L external reference voltage

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 29 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 29. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

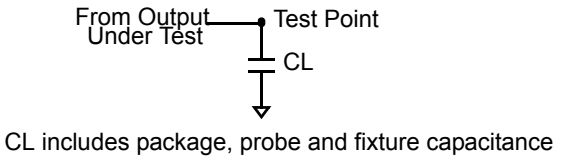

Figure 4. Load Circuit for Output

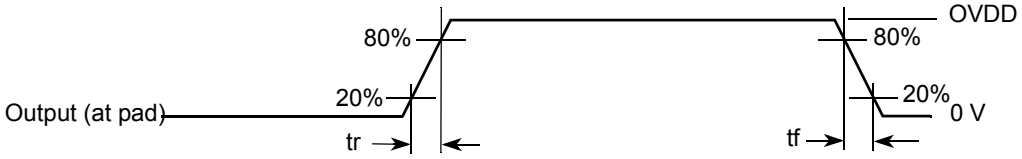

Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 30 and Table 31, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

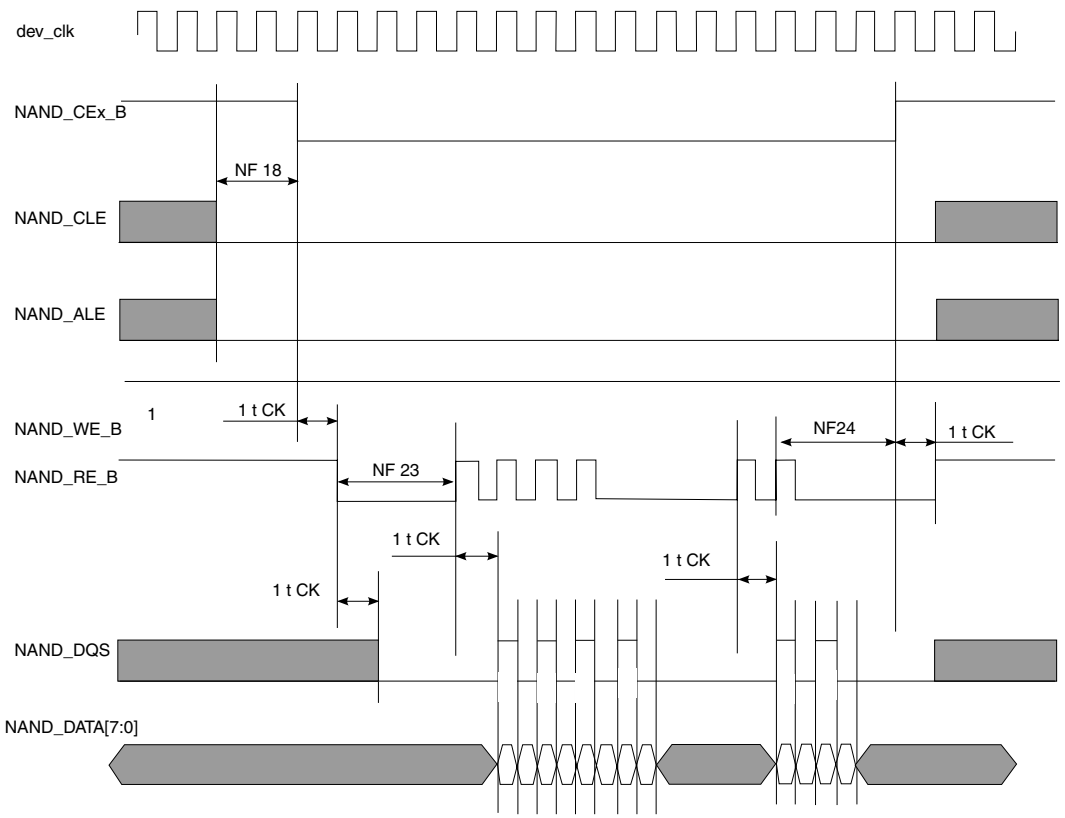

Figure 32. Samsung Toggle Mode Data Read Timing

Table 49. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		—
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		—
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see 2]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

Table 54. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [6][7]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(SCKT pin) = transmit clock
ESAI_RX_CLK(SCKR pin) = receive clock
ESAI_TX_FS(FST pin) = transmit frame sync
ESAI_RX_FS(FSR pin) = receive frame sync
ESAI_TX_HF_CLK(HCKT pin) = transmit high frequency clock
ESAI_RX_HF_CLK(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

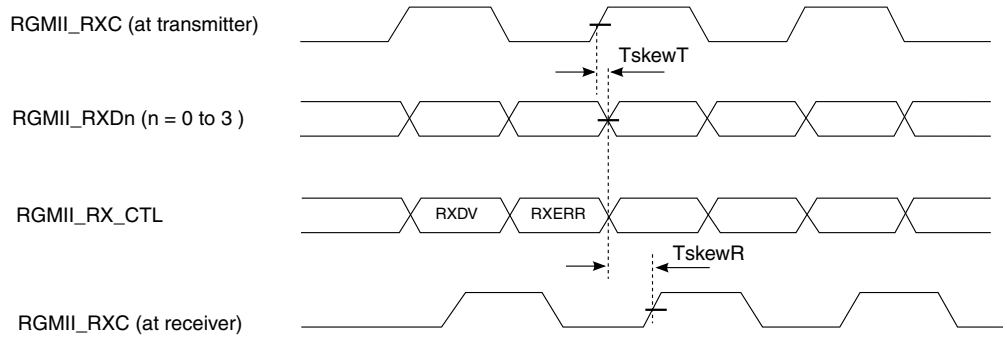

Figure 50. RGMII Receive Signal Timing Diagram Original

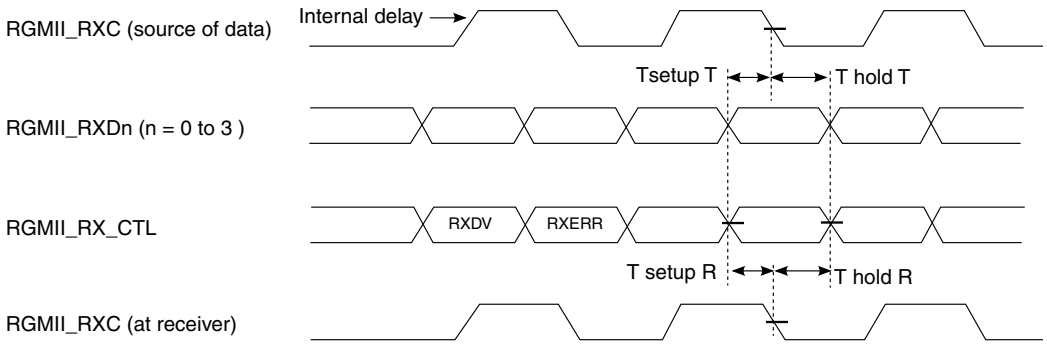

Figure 51. RGMII Receive Signal Timing Diagram with Internal Delay

4.12.7 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM) to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

Table 67. LCDIF Display Interface Signal Mapping (continued)

Pin Name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	X
LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	X
LCD_D23	X	X	X	G[7]	X
LCD_D22	X	X	X	G[6]	X
LCD_D21	X	X	X	R[5]	X
LCD_D20	X	X	X	R[4]	X
LCD_D19	X	X	X	R[3]	X
LCD_D18	X	X	X	R[2]	X
LCD_D17	X	X	R[5]	R[1]	X
LCD_D16	X	X	R[4]	R[0]	X
LCD_D15 / VSYNC*	X	R[4]	R[3]	G[7]	X
LCD_D14 / HSYNC**	X	R[3]	R[2]	G[6]	X
LCD_D13 / LCD_DOTCLK**	X	R[2]	R[1]	G[5]	X
LCD_D12 / ENABLE**	X	R[1]	R[0]	G[4]	X
LCD_D11	X	R[0]	G[5]	G[3]	X
LCD_D10	X	G[5]	G[4]	G[2]	X
LCD_D9	X	G[4]	G[3]	G[1]	X
LCD_D8	X	G[3]	G[2]	G[0]	X
LCD_D7	R[2]	G[2]	G[1]	B[7]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	B[6]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	X
LCD_BUSY / LCD_VSYNC	LCD_BUSY (OR optional LCD_VSYNC)	LCD_BUSY (OR optional LCD_VSYNC)	LCD_BUSY (OR optional LCD_VSYNC)	LCD_BUSY (OR optional LCD_VSYNC)	X

Table 70. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit	Comment
Bus Hold from MLB_CLK low	t_{mdzh}	4	—	ns	—
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}		10	ns	—

1 The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

2 MLB_CLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 71; unless otherwise noted.

Table 71. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK Operating Frequency[1]	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	1	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	1	ns	V_{IH} TO V_{IL}
MLB_CLK low time	t_{mckl}	6.1	—	ns	[2]
MLB_CLK high time	t_{mckh}	9.3	—	ns	—
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcfdz}	0	t_{mckl}	ns	[3]
Bus Hold from MLB_CLK low	t_{mdzh}	2	—	ns	—
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}	—	7	ns	—

1 The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

2 MLB_CLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 82. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

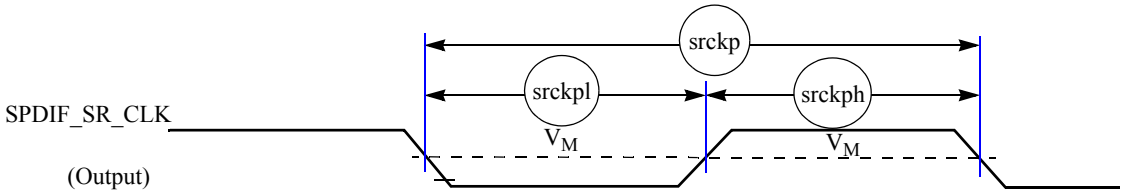

Figure 68. SPDIF_SR_CLK Timing Diagram

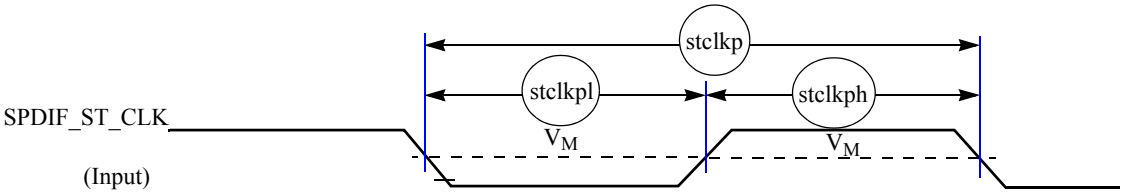

Figure 69. SPDIF_ST_CLK Timing Diagram

Table 105. SD/MMC Boot through USDHC1 (continued)

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)	SDMMC MFG Mode
NAND_DATA02	usdhc1.DATA6	Alt 1	—	—	Yes	—	—
NAND_DATA03	usdhc1.DATA7	Alt 1	—	—	Yes	—	—
NAND_WP_B	GPIO4_15	Alt 5	—	—	—	Yes	—
NAND_READY_B	usdhc1.VSELECT	Alt 1	—	—	—	Yes	—

Table 106. SD/MMC Boot through USDHC2

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)
SD2_CLK	usdhc2.CLK	Alt 0	Yes	—	—	—
SD2_CMD	usdhc2.CMD	Alt 0	Yes	—	—	—
SD2_DATA0	usdhc2.DATA0	Alt 0	Yes	—	—	—
SD2_DATA1	usdhc2.DATA1	Alt 0	—	Yes	Yes	—
SD2_DATA2	usdhc2.DATA2	Alt 0	—	Yes	Yes	—
SD2_DATA3	usdhc2.DATA3	Alt 0	Yes	—	—	—
NAND_DATA04	usdhc2.DATA4	Alt 1	—	—	Yes	—
NAND_DATA05	usdhc2.DATA5	Alt 1	—	—	Yes	—
NAND_DATA06	usdhc2.DATA6	Alt 1	—	—	Yes	—
NAND_DATA07	usdhc2.DATA7	Alt 1	—	—	Yes	—
NAND_RE_B	GPIO4_IO12	Alt 5	—	—	—	Yes
NAND_CE0_B	usdhc2.VSELECT	Alt 1	—	—	—	Yes

Table 107. SD/MMC Boot through USDHC3

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)
SD3_CLK	usdhc3.CLK	Alt 0	Yes	—	—	—
SD3_CMD	usdhc3.CMD	Alt 0	Yes	—	—	—
SD3_DATA0	usdhc3.DATA0	Alt 0	Yes	—	—	—
SD3_DATA1	usdhc3.DATA1	Alt 0	—	Yes	Yes	—
SD3_DATA2	usdhc3.DATA2	Alt 0	—	Yes	Yes	—

6.3.2 19x19 mm Supplies Contact Assignments and Functional Contact Assignments

Table 112 shows supplies contact assignments for the 19x19 mm package.

Table 112. 19x19 mm Supplies Contact Assignments

Supply Rail Name	19x19 Ball(s) Position(s)	Remark
ADC_VREFH	AA16	ADC high reference voltage
ADC_VREFL	U16	ADC low reference voltage
DRAM_VREF	M3	DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM.
DRAM_ZQPAD	C4	DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss.
GPANAIO	V18	Analog output for NXP use only. This output must always be left unconnected.
NGND_KEL0	R16	Connect to Vss
NVCC_CSI	P18	Supply input for the CSI interface
NVCC_DRAM	F5, G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5, V5	Supply input for the DDR I/O interface
NVCC_DRAM_2P5	M6	Supply input for the DDR interface
NVCC_ENET	F6	Supply input for the ENET interfaces
NVCC_GPIO	G15	Supply input for the GPIO interface
NVCC_HIGH	U12	3.3 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_JTAG	U11	Supply input for the JTAG interface
NVCC_KEY	G16	Supply input for the Key Pad Port (KPP) interface
NVCC_LCD1	G17	Supply input for the LCD interface
NVCC_LOW	V11	1.8 V Supply input for the dual-voltage IOs on the SD3 interface
NVCC_LVDS	T18	Supply input for the LVDS interface
NVCC_NAND	U8	Supply input for the Raw NAND flash memories interface
NVCC_PLL	Y23	Supply input for the PLLs
NVCC_QSPI	G14	Supply input for the QSPI interface
NVCC_RGMII1	F8	Supply input for the RGMII1 interface
NVCC_RGMII2	G9	Supply input for the RGMII2 interface
NVCC_SD1	G12	Supply input for the SD1 interface
NVCC_SD2	G11	Supply input for the SD2 interface
NVCC_SD4	U10	Supply input for the SD4 interface
NVCC_USB_H	AA6	Supply input for the USB HSIC interface
PCIE_REXT	M21	PCIe impedance calibration resistor. Connect PCIE_REXT to an external 200 ohm 1% resistor to Vss.
PCIE_VP	L18	Supply input for the PCIe PHY
PCIE_VPH	R18	Supply input for the PCIe PHY

Table 112. 19x19 mm Supplies Contact Assignments (continued)

Supply Rail Name	19x19 Ball(s) Position(s)	Remark
PCIE_VPTX	M18	Supply input for the PCIe PHY
RSVD	E5	Reserved. Do not connect.
USB_OTG1_VBUS	W20	VBUS input for USB_OTG1
USB_OTG2_VBUS	Y18	VBUS input for USB_OTG2
Reserved	K21	Reserved. Leave unconnected.
Reserved	L21	Reserved. Connect to ground through a 10 kΩ resistor.
Reserved	N18	Reserved. Connect to ground through a 10 kΩ resistor.
VDD_ARM_CAP	C18, J12, J13, J14, J15, J16, K16, L16, M16	Supply voltage output from internal LDO_ARM. Requires external capacitor(s).
VDD_ARM_IN	K12, K13, K14, K15, J21, L15, M15	Supply voltage input for internal LDO_ARM.
VDD_HIGH_CAP	U17, U18	Supply voltage output from internal LDO_2P5. Requires external capacitor(s).
VDD_HIGH_IN	U14, U15	Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS.
VDD_SNVS_CAP	Y22	Supply voltage output from internal LDO_SNVS. Requires external capacitor(s).
VDD_SNVS_IN	V15	Supply voltage input to the SNVS voltage domain
VDD_SOC_CAP	J7, J8, J9, J10, J11, K7, L7, M7, N7, N16, P7, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, Y10, AA10	Supply voltage output from internal LDO_SOC. Requires external capacitor(s).
VDD_SOC_IN	C9, K8, K9, K10, K11, L8, M8, N8, N15, P8, P9, P10, P11, P12, P13, P14, P15	Supply voltage input to internal LDO_SOC and LDO_PCIE
VDD_USB_CAP	AA17	Supply voltage output from internal LDO_USB. Requires external capacitor(s).
VDDA_ADC_3P3	U13	Supply voltage input to the ADC. This supply must be provided even if the ADC is not used.
VSS	A1, A6, A23, B3, B6, C2, C3, C5, D7, D9, D11, D13, D15, D17, D19, F2, F3, F20, G6, G7, G8, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, J2, J3, J6, J17, J20, K6, K17, L2, L3, L6, L9, L10, L11, L12, L13, L14, L17, M9, M10, M11, M12, M13, M14, M17, M20, M22, M23, N2, N3, N6, N9, N10, N11, N12, N13, N14, N17, P6, P17, R2, R3, R6, R17, R20, R21, R22, R23, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, U6, U7, U20, U21, V2, V3, V8, V9, W19, W21, W22, W23, Y7, Y11, Y13, Y15, Y17, Y20, AA2, AA3, AA5, AA18, AA20, AB3, AB6, AB19, AB21, AB23, AC1, AC6, AC19, AC21, AC23	Ground

Table 113. 19x19 mm Functional Contact Assignments (continued)

Ball Name	19x19 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
SD4_DATA7	AB11	NVCC_SD4	GPIO	ALT5	GPIO6_IO21	Input	Keeper
SD4_RESET_B	Y9	NVCC_SD4	GPIO	ALT5	GPIO6_IO22	Input	Keeper
SNVS_PMIC_ON_REQ[1]	W16	VDD_SNVS_IN	GPIO	—	SNVS_PMIC_ON_REQ	Output	100 kΩ pull-up
SNVS_TAMPER	V14	VDD_SNVS_IN	GPIO	—	SNVS_TAMPER	Input	100 kΩ pull-down
TEST_MODE	Y16	VDD_SNVS_IN	—	—	TEST_MODE	Input	100 kΩ pull-down
USB_H_DATA	Y5	NVCC_USB_H	GPIO	ALT5	GPIO7_IO10	Input	100 kΩ pull-down
USB_H_STROBE	Y6	NVCC_USB_H	GPIO	ALT5	GPIO7_IO11	Input	100 kΩ pull-down
USB_OTG1_CHD_B	V19	VDD_USB_CAP	—	—	USB_OTG1_CHD_B	—	—
USB_OTG1_DN	Y21	VDD_USB_CAP	—	—	USB_OTG1_DN	—	—
USB_OTG1_DP	AA21	VDD_USB_CAP	—	—	USB_OTG1_DP	—	—
USB_OTG2_DN	Y19	VDD_USB_CAP	—	—	USB_OTG2_DN	—	—
USB_OTG2_DP	AA19	VDD_USB_CAP	—	—	USB_OTG2_DP	—	—
Reserved	L23	—	—	—	—	—	—
Reserved	L22	—	—	—	—	—	—
Reserved	K23	—	—	—	—	—	—
Reserved	K22	—	—	—	—	—	—
XTALI	AB22	NVCC_PLL	—	—	XTALI	—	—
XTALO	AC22	NVCC_PLL	—	—	XTALO	—	—

[1] On silicon revisions prior to 1.2, the SNVS_PMIC_ON_REQ may briefly go low and then return high during POR. SNVS_PMIC_ON_REQ should be high during POR. An external 100k pull-up is required.

Table 114. 19x19 mm, 0.8 mm Pitch, 23x23 Ball Map (continued)

	H	J	K	L	M	N	P
1	DRAM_SDQS1_P	DRAM_DATA08	DRAM_DATA12	DRAM_DATA09	DRAM_SDCLK0_N	DRAM_DATA05	DRAM_DATA04
2	DRAM_SDQS1_N	VSS	DRAM_DATA10	VSS	DRAM_SDCLK0_P	VSS	DRAM_DATA07
3	DRAM_ADDR03	VSS	DRAM_SDWE_B	VSS	DRAM_VREF	VSS	DRAM_ADDR09
4	DRAM_SDBA0	DRAM_CS0_B	DRAM_CAS_B	DRAM_RAS_B	DRAM_SDBA2	DRAM_ADDR00	DRAM_ADDR13
5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
6	VSS	VSS	VSS	VSS	NVCC_DRAM_2P5	VSS	VSS
7	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN
9	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
10	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
11	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
12	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
13	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
14	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
15	VSS	VDD_ARM_CAP	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_SOC_IN	VDD_SOC_IN
16	VSS	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_SOC_CAP	VDD_SOC_CAP
17	VSS	VSS	VSS	VSS	VSS	VSS	VSS
18	LCD1_DATA11	LCD1_DATA06	LCD1_DATA04	PCIE_VP	PCIE_VPTX	RSVD	NVCC_CSI
19	LCD1_DATA10	LCD1_DATA05	LCD1_DATA03	CSI_DATA07	CSI_DATA06	CSI_DATA04	CSI_DATA02
20	LCD1_DATA09	VSS	LCD1_DATA02	CSI_HSYNC	VSS	CSI_DATA05	CSI_DATA01
21	LCD1_CLK	VDD_ARM_IN	RSVD	RSVD	PCIE_REXT	CSI_DATA03	CSI_DATA00
22	LCD1_DATA08	LCD1_DATA01	RSVD	RSVD	VSS	PCIE_RX_N	PCIE_TX_N
23	LCD1_DATA07	LCD1_DATA00	RSVD	RSVD	VSS	PCIE_RX_P	PCIE_TX_P
	H	J	K	L	M	N	P

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

Ball Name	17x17 NP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
DRAM_DATA12	J1	NVCC_DRAM	DDR	—	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	F1	NVCC_DRAM	DDR	—	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	E2	NVCC_DRAM	DDR	—	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	E1	NVCC_DRAM	DDR	—	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DATA16	V1	NVCC_DRAM	DDR	—	DRAM_DATA16	Input	100 kΩ pull-up
DRAM_DATA17	W4	NVCC_DRAM	DDR	—	DRAM_DATA17	Input	100 kΩ pull-up
DRAM_DATA18	Y4	NVCC_DRAM	DDR	—	DRAM_DATA18	Input	100 kΩ pull-up
DRAM_DATA19	U2	NVCC_DRAM	DDR	—	DRAM_DATA19	Input	100 kΩ pull-up
DRAM_DATA20	W3	NVCC_DRAM	DDR	—	DRAM_DATA20	Input	100 kΩ pull-up
DRAM_DATA21	Y2	NVCC_DRAM	DDR	—	DRAM_DATA21	Input	100 kΩ pull-up
DRAM_DATA22	U1	NVCC_DRAM	DDR	—	DRAM_DATA22	Input	100 kΩ pull-up
DRAM_DATA23	V2	NVCC_DRAM	DDR	—	DRAM_DATA23	Input	100 kΩ pull-up
DRAM_DATA24	A2	NVCC_DRAM	DDR	—	DRAM_DATA24	Input	100 kΩ pull-up
DRAM_DATA25	D1	NVCC_DRAM	DDR	—	DRAM_DATA25	Input	100 kΩ pull-up
DRAM_DATA26	C1	NVCC_DRAM	DDR	—	DRAM_DATA26	Input	100 kΩ pull-up
DRAM_DATA27	D2	NVCC_DRAM	DDR	—	DRAM_DATA27	Input	100 kΩ pull-up
DRAM_DATA28	C2	NVCC_DRAM	DDR	—	DRAM_DATA28	Input	100 kΩ pull-up
DRAM_DATA29	B3	NVCC_DRAM	DDR	—	DRAM_DATA29	Input	100 kΩ pull-up
DRAM_DATA30	B4	NVCC_DRAM	DDR	—	DRAM_DATA30	Input	100 kΩ pull-up

Table 119. 17x17 mm WP (with PCIe) Supplies Contact Assignments (continued)

Supply Rail Name	17x17 WP [with PCIe] Ball(s) Position(s)	Remark
USB_OTG1_VBUS	T16	VBUS input for USB_OTG1
USB_OTG2_VBUS	T15	VBUS input for USB_OTG2
VDD_ARM_CAP	C16, D16, H10, H11, H12, H13, J13, K13, L13	Supply voltage output from internal LDO_ARM. Requires external capacitor(s).
VDD_ARM_IN	H18, J10, J11, J12, K12, L12	Supply voltage input for internal LDO_ARM.
VDD_HIGH_CAP	V17, V18	Supply voltage output from internal LDO_2P5. Requires external capacitor(s).
VDD_HIGH_IN	U17, U18	Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS.
VDD_SNVS_CAP	V16	Supply voltage output from internal LDO_SNVS. Requires external capacitor(s).
VDD_SNVS_IN	T18	Supply voltage input to the SNVS voltage domain
VDD_SOC_CAP	H8, H9, J8, K8, L8, M8, M13, N8, N9, N10, N11, N12, V8	Supply voltage output from internal LDO_SOC. Requires external capacitor(s).
VDD_SOC_IN	C7, C8, J9, K9, L9, M9, M10, M11, M12	Supply voltage input to internal LDO_SOC and LDO_PCIE
VDD_USB_CAP	V15	Supply voltage output from internal LDO_USB. Requires external capacitor(s).
VDDA_ADC_3P3	R13	Supply voltage input to the ADC. This supply must be provided even if the ADC is not used.
VSS	A1, A20, C3, C4, C18, D6, D9, D12, D15, E3, F3, F5, F17, G7, G8, G9, G10, G11, G12, G13, G14, H3, H7, H14, J7, J14, J17, K3, K10, K11, K14, L3, L7, L10, L11, L14, M7, M14, M17, N3, N7, N13, N19, N20, P7, P8, P9, P10, P11, P12, R3, R5, R17, T3, T19, T20, U6, U9, U12, U15, V3, V4, W16, W18, Y1, Y16, Y18, Y20	Ground

Table 120 shows an alpha-sorted list of functional contact assignments for the 17x17 mm WP (with PCIe) package.

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments

Ball Name	17x17 WP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
ADC1_IN0	Y14	VDDA_ADC_3P3	—	—	ADC1_IN0	Input	—
ADC1_IN1	W14	VDDA_ADC_3P3	—	—	ADC1_IN1	Input	—

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

Ball Name	17x17 WP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
DRAM_DATA15	E1	NVCC_DRAM	DDR	—	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DATA16	V1	NVCC_DRAM	DDR	—	DRAM_DATA16	Input	100 kΩ pull-up
DRAM_DATA17	W4	NVCC_DRAM	DDR	—	DRAM_DATA17	Input	100 kΩ pull-up
DRAM_DATA18	Y4	NVCC_DRAM	DDR	—	DRAM_DATA18	Input	100 kΩ pull-up
DRAM_DATA19	U2	NVCC_DRAM	DDR	—	DRAM_DATA19	Input	100 kΩ pull-up
DRAM_DATA20	W3	NVCC_DRAM	DDR	—	DRAM_DATA20	Input	100 kΩ pull-up
DRAM_DATA21	Y2	NVCC_DRAM	DDR	—	DRAM_DATA21	Input	100 kΩ pull-up
DRAM_DATA22	U1	NVCC_DRAM	DDR	—	DRAM_DATA22	Input	100 kΩ pull-up
DRAM_DATA23	V2	NVCC_DRAM	DDR	—	DRAM_DATA23	Input	100 kΩ pull-up
DRAM_DATA24	A2	NVCC_DRAM	DDR	—	DRAM_DATA24	Input	100 kΩ pull-up
DRAM_DATA25	D1	NVCC_DRAM	DDR	—	DRAM_DATA25	Input	100 kΩ pull-up
DRAM_DATA26	C1	NVCC_DRAM	DDR	—	DRAM_DATA26	Input	100 kΩ pull-up
DRAM_DATA27	D2	NVCC_DRAM	DDR	—	DRAM_DATA27	Input	100 kΩ pull-up
DRAM_DATA28	C2	NVCC_DRAM	DDR	—	DRAM_DATA28	Input	100 kΩ pull-up
DRAM_DATA29	B3	NVCC_DRAM	DDR	—	DRAM_DATA29	Input	100 kΩ pull-up
DRAM_DATA30	B4	NVCC_DRAM	DDR	—	DRAM_DATA30	Input	100 kΩ pull-up
DRAM_DATA31	A4	NVCC_DRAM	DDR	—	DRAM_DATA31	Input	100 kΩ pull-up
DRAM_DQM0	N2	NVCC_DRAM	DDR	—	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	G2	NVCC_DRAM	DDR	—	DRAM_DQM1	Output	100 kΩ pull-up

Table 123. 14 x 14 Functional Contact Assignments

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
ADC1_IN0	N14	VDDA_ADC_3P3	—	—	ADC1_IN0	Input	—
ADC1_IN1	T15	VDDA_ADC_3P3	—	—	ADC1_IN1	Input	—
ADC1_IN2	W14	VDDA_ADC_3P3	—	—	ADC1_IN2	Input	—
ADC1_IN3	P13	VDDA_ADC_3P3	—	—	ADC1_IN3	Input	—
ADC2_IN0	W15	VDDA_ADC_3P3	—	—	ADC2_IN0	Input	—
ADC2_IN1	R14	VDDA_ADC_3P3	—	—	ADC2_IN1	Input	—
ADC2_IN2	N15	VDDA_ADC_3P3	—	—	ADC2_IN2	Input	—
ADC2_IN3	R15	VDDA_ADC_3P3	—	—	ADC2_IN3	Input	—
BOOT_MODE0	Y16	VDD_SNVS_IN	GPIO	—	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	W16	VDD_SNVS_IN	GPIO	—	BOOT_MODE1	Input	100 kΩ pull-down
CCM_CLK1_N	P20	VDD_HIGH_CAP	—	—	CCM_CLK1_N	—	—
CCM_CLK1_P	P19	VDD_HIGH_CAP	—	—	CCM_CLK1_P	—	—
CCM_CLK2	V16	VDD_HIGH_CAP	—	—	CCM_CLK2	—	—
CCM_PMIC_STBY_REQ	N16	VDD_SNVS_IN	GPIO	—	CCM_PMIC_STBY_REQ	Output	0
DRAM_ADDR00	N5	NVCC_DRAM	DDR	—	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	P5	NVCC_DRAM	DDR	—	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	M4	NVCC_DRAM	DDR	—	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	K5	NVCC_DRAM	DDR	—	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	H5	NVCC_DRAM	DDR	—	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	F4	NVCC_DRAM	DDR	—	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	N4	NVCC_DRAM	DDR	—	DRAM_ADDR06	Output	100 kΩ pull-up
DRAM_ADDR07	G5	NVCC_DRAM	DDR	—	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J4	NVCC_DRAM	DDR	—	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	L2	NVCC_DRAM	DDR	—	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	H4	NVCC_DRAM	DDR	—	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	M3	NVCC_DRAM	DDR	—	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	M5	NVCC_DRAM	DDR	—	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	J3	NVCC_DRAM	DDR	—	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	R1	NVCC_DRAM	DDR	—	DRAM_ADDR14	Output	100 kΩ pull-up

Table 125. i.MX 6SoloX Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	7/2015	*(continued from previous page)* • Updated Table 45, "EIM Asynchronous Timing Parameters Relative to Chip Select," on page 60. Elaborated to show results of calculations. No specification change. • In Table 64, “DDR3/DDR3L Read Cycle,” on page 93, updated minimum value for DDR26 • Added note regarding ECSPIx_MOSI to Figure 36, "ECSPI Master Mode Timing Diagram," on page 74 • Added note regarding ECSPIx_MISO to Figure 37, "ECSPI Slave Mode Timing Diagram," on page 75 • Updated Figure 42, "SDR50/SDR104 Timing," on page 82 • In Table 68, "LVDS Display Bridge (LDB) Electrical Specification," on page 93: – Corrected units for V_{OH} values from ‘mV’ to ‘V’ – Corrected units for V_{OL} values from ‘mV’ to ‘V’ • In Section 4.12.21, “USB PHY Parameters,” in list of amendments to Rev. 2 of the The USB PHY meets the electrical compliance requirements defined in revision 2.0 of the *USB On-The-Go and Embedded Host Supplement to the USB 2.0 Specification,* added “Portable device only” under “Battery Charging Specification” • Added Table 111, "Signals with Different States During Reset and After Reset," on page 132 • In Table 113, "19x19 mm Functional Contact Assignments," on page 138, corrected GPIO signal names • In Table 116, "17x17 mm NP (no PCIe) Supplies Contact Assignments," on page 157, added ball L9 to the VDD_SOC_CAP row • In Table 123, "14 x 14 Functional Contact Assignments," on page 191, corrected power group for SD2 ball names to ‘NVCC_SD1_SD2’
0	2/2015	• Initial public release

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