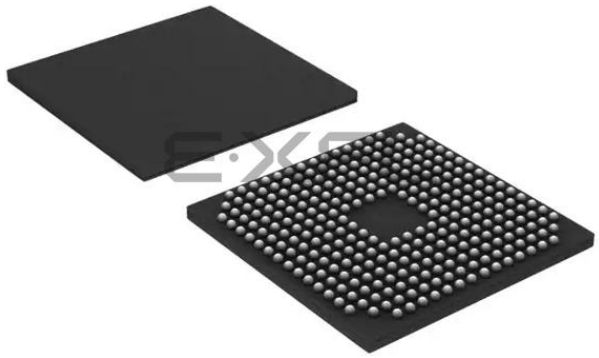

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3220fet296-01-5

- Multi-layer AHB system that provides a separate bus for each AHB master, including both an instruction and data bus for the CPU, two data busses for the DMA controller, and another bus for the USB controller, one for the LCD, and a final one for the Ethernet MAC. There are no arbitration delays in the system unless two masters attempt to access the same slave at the same time.
- External memory controller for DDR and SDR SDRAM as well as for static devices.
- Two NAND flash controllers: One for single-level NAND flash devices and the other for multi-level NAND flash devices.
- Master Interrupt Controller (MIC) and two Slave Interrupt Controllers (SIC), supporting 74 interrupt sources.
- Eight channel General Purpose DMA (GPDMA) controller on the AHB that can be used with the SD card port, the high-speed UARTs, I^2S-bus interfaces, and SPI interfaces, as well as memory-to-memory transfers.
- Serial interfaces:
  - 10/100 Ethernet MAC with dedicated DMA Controller.
  - USB interface supporting either device, host (OHCI compliant), or On-The-Go (OTG) with an integral DMA controller and dedicated PLL to generate the required 48 MHz USB clock.
  - Four standard UARTs with fractional baud rate generation and 64 byte FIFOs. One of the standard UARTs supports IrDA.
  - Three additional high-speed UARTs intended for on-board communications that support baud rates up to 921 600 when using a 13 MHz main oscillator. All high-speed UARTs provide 64 byte FIFOs.
  - Two SPI controllers.
  - Two SSP controllers.
  - Two I^2C-bus interfaces with standard open-drain pins. The I^2C-bus interfaces support single master, slave, and multi-master I^2C-bus configurations.
  - Two I^2S-bus interfaces, each with separate input and output channels. Each channel can be operated independently on three pins, or both input and output channels can be used with only four pins and a shared clock.
- Additional peripherals:
  - LCD controller supporting both STN and TFT panels, with dedicated DMA controller. Programmable display resolution up to 1024×768.
  - Secure Digital (SD) memory card interface, which conforms to the *SD Memory Card Specification Version 1.01*.
  - General Purpose (GP) input, output, and I/O pins. Includes 12 GP input pins, 24 GP output pins, and 51 GP I/O pins.
  - 10-bit, 400 kHz Analog-to-Digital Converter (ADC) with input multiplexing from three pins. Optionally, the ADC can operate as a touch screen controller.
  - Real-Time Clock (RTC) with separate power pin and dedicated 32 kHz oscillator. NXP implemented the RTC in an independent on-chip power domain so it can remain active while the rest of the chip is not powered. The RTC also includes a 32-byte scratch pad memory.
  - 32-bit general purpose high-speed timer with a 16-bit pre-scaler. This timer includes one external capture input pin and a capture connection to the RTC clock. Interrupts may be generated using three match registers.

5. Block diagram

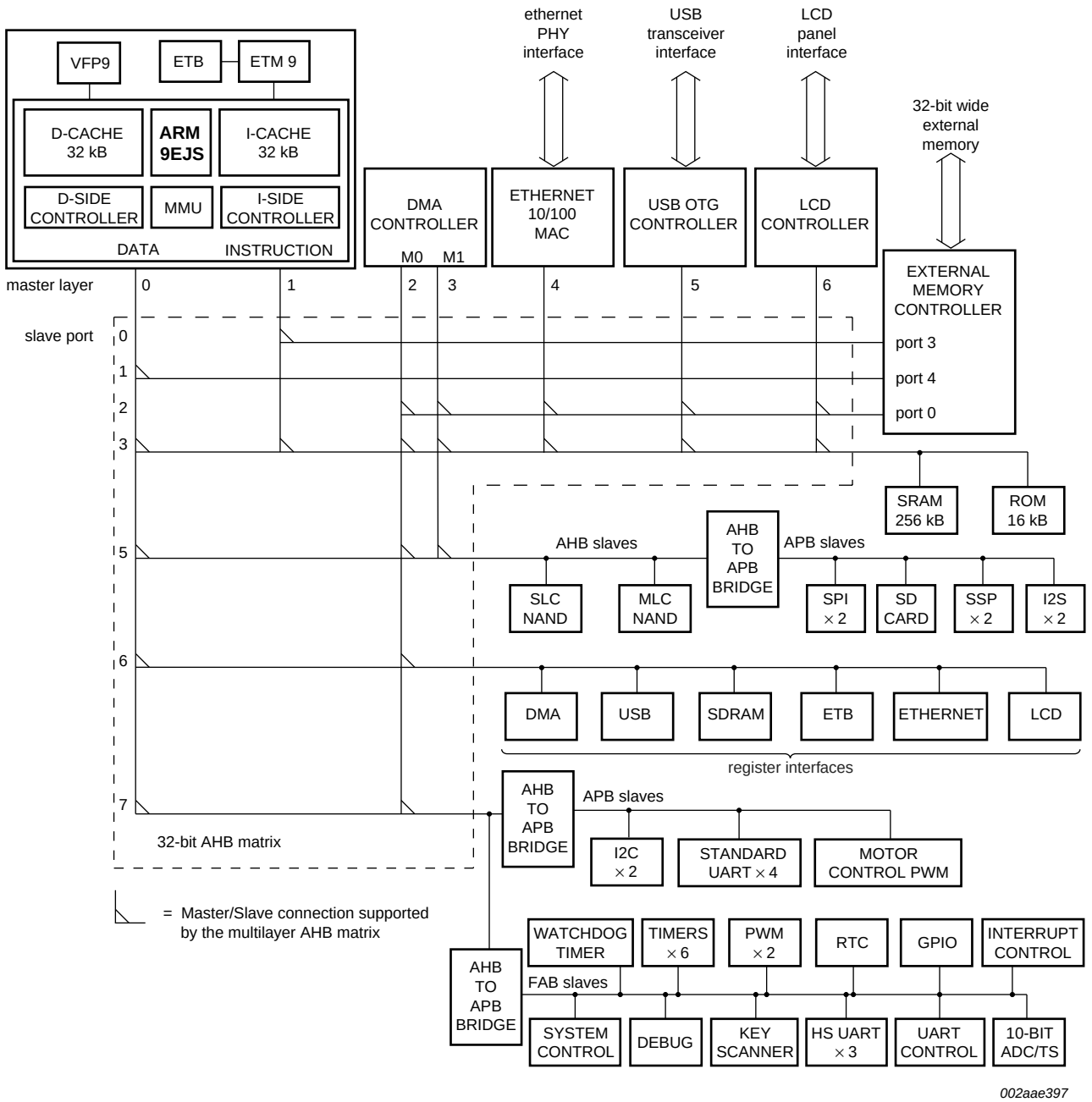


Fig 1. Block diagram of LPC3220/30/40/50

7. Functional description

7.1 CPU and subsystems

7.1.1 CPU

NXP created the LPC3220/30/40/50 using an ARM926EJ-S CPU core that includes a Harvard architecture and a 5-stage pipeline. To this ARM core, NXP implemented a 32 kB instruction cache, a 32 kB data cache and a Vector Floating Point coprocessor. The ARM926EJ-S core also has an integral Memory Management Unit (MMU) to provide the virtual memory capabilities required to support the multi-programming demands of modern operating systems. The basic ARM926EJ-S core V5TE instruction set includes DSP instruction extensions for native Jazelle Java Byte-code execution in hardware. The LPC3220/30/40/50 operates at CPU frequencies up to 266 MHz.

7.1.2 Vector Floating Point (VFP) coprocessor

The LPC3220/30/40/50 includes a VFP co-processor providing full support for single-precision and double-precision add, subtract, multiply, divide, and multiply-accumulate operations at CPU clock speeds. It is compliant with the IEEE 754 standard for binary Floating-Point Arithmetic. This hardware floating point capability makes the microcontroller suitable for advanced motor control and DSP applications. The VFP has 3 separate pipelines for floating-point MAC operations, divide or square root operations, and Load/Store operations. These pipelines operate in parallel and can complete execution out of order. All single-precision instructions execute in one cycle, except the divide and square root instructions. All double-precision multiply and multiply-accumulate instructions take two cycles. The VFP also provides format conversions between floating-point and integer word formats.

7.1.3 Emulation and debugging

The LPC3220/30/40/50 supports emulation and debugging via a dedicated JTAG serial port. An Embedded Trace Buffer allows tracing program execution. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

7.1.3.1 Embedded ICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an Embedded ICE protocol converter. The Embedded ICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel (DCC) function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or entering the debug state.

7.2.1 APB

Many peripheral functions are accessed by on-chip APBs that are attached to the higher speed AHB. The APB performs reads and writes to peripheral registers in three peripheral clocks.

7.2.2 FAB

Some peripherals are placed on a special bus called FAB that allows faster CPU access to those peripheral functions. A write access to FAB peripherals takes a single AHB clock and a read access to FAB peripherals takes two AHB clocks.

7.3 Physical memory map

The physical memory map incorporates several distinct regions, as shown in Figure 3. When an application is running, the CPU interrupt vectors are re-mapped to allow them to reside in on-chip SRAM (IRAM).

packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU. The Ethernet DMA can access off-chip memory via the EMC, as well as the IRAM. The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.6.2.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching. Wake-on-LAN power management support allows system wake-up using the receive filters or a magic frame detection filter.
- Physical interface
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.6.3 USB interface

The LPC3220/30/40/50 supports USB in either device, host, or OTG configuration.

7.6.3.1 USB device controller

The USB device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error

- Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices under software control. HNP is partially implemented in hardware.
- Provides programmable timers required for HNP and SRP.
- Supports slave mode operation through AHB slave interface.
- Supports the OTG ATX from NXP (ISP 1302) or any external CEA-2011OTG specification compliant ATX.

7.6.4 LCD controller

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode.

An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.6.4.1 Features

- AHB bus master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 k color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32 bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock or from a clock input pin.

7.7 System functions

To enhance the performance of the LPC3220/30/40/50 incorporates the following system functions, an Interrupt Controller (INTC), a watchdog timer, a millisecond timer, and several power control features. These functions are described in the following sections

7.7.1 Interrupt controller

The interrupt controller is comprised of three basic interrupt controller blocks, supporting a total of 73 interrupt sources. Each interrupt source can be individually enabled/disabled and configured for high or low level triggering, or rising or falling edge triggering. Each interrupt may also be steered to either the FIQ or IRQ input of the ARM9. Raw interrupt status and masked interrupt status registers allow versatile condition evaluation. In addition to peripheral functions, each of the six general purpose input/output pins and 12 of the 22 general purpose input pins are connected directly to the interrupt controller.

7.7.2 Watchdog timer

The watchdog timer block is clocked by the main peripheral clock, which clocks a 32-bit counter. A match register is compared to the Timer. When configured for watchdog functionality, a match drives the match output low. The match output is gated with an enable signal that gives the opportunity to generate two type of reset signal: one that only resets chip internally, and another that goes through a programmable pulse generator before it goes to the external pin $\overline{\text{RESOUT}}$ and to the internal chip reset.

7.7.2.1 Features

- Programmable 32-bit timer.
- Internally resets the device if not periodically reloaded.
- Flag to indicate that a watchdog reset has occurred.
- Programmable watchdog pulse output on $\overline{\text{RESOUT}}$ pin.
- Can be used as a standard timer if watchdog is not used.
- Pause control to stop counting when core is in debug state.

7.7.3 Millisecond timer

The millisecond timer is clocked by 32 kHz RTC clock, so a prescaler is not needed to obtain a lower count rate.

The millisecond timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and the cause the Timer/Counter either continue to run, stop, or be reset.

7.7.3.1 Features

- 32-bit Timer/Counter, running from the 32 kHz RTC clock.
- Counter or Timer operation.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

output to be used directly. The maximum PLL output frequency supported by the CPU is 266 MHz. The only output frequency supported by the USB PLL is 48 MHz, and the clock has strict requirements for nominal frequency (500 ppm) and jitter (500 ps).

7.7.4.4 Power control modes

The LPC3220/30/40/50 supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: Run mode, Direct Run mode, and Stop mode.

Run mode is the normal operating mode for applications that require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. In Run mode, the CPU can run at up to 266 MHz and the AHB bus can run at up to 133 MHz.

Direct Run mode allows reducing the CPU and AHB bus rates in order to save power. Direct Run mode can also be the normal operating mode for applications that do not require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. Direct Run mode is the default mode following chip reset.

Stop mode causes all CPU and AHB operation to cease, and stops clocks to peripherals other than the USB block.

7.7.4.5 Reset

Reset is accomplished by an active LOW signal on the $\overline{\text{RESET}}$ input pin. A reset pulse with a minimum width of 10 main oscillator clocks after the oscillator is stable is required to guarantee a valid chip reset. At power-up, 10 milliseconds should be allowed for the oscillator to start up and stabilize after V_{DD} reaches operational voltage. An internal reset with a minimum duration of 10 clock pulses will also be applied if the watchdog timer generates an internal device reset.

The $\overline{\text{RESET}}$ pin is located in the RTC power domain. This means that the RTC power must be present for an external reset to have any effect. The RTC power domain nominally runs from 1.2 V, but the $\overline{\text{RESET}}$ pin can be driven as high as 1.95 V.

7.8 Communication peripheral interfaces

In addition to the Ethernet MAC and USB interfaces there are many more serial communication peripheral interfaces available on the LPC3220/30/40/50. Here is a list of the serial communication interfaces:

- Seven UARTs; four standard UARTs and three high-speed UARTs
- Two SPI serial I/O controllers
- Two SSP serial I/O controllers
- Two I^2C serial I/O controllers
- Two I^2S audio controllers

A short functional description of each of these peripherals is provided in the following sections.

7.8.1 UARTs

The LPC3220/30/40/50 contains seven UARTs. Four are standard UARTs, and three are high-speed UARTs.

7.8.1.1 Standard UARTs

The four standard UARTs are compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16, 32, 48, and 60 Bytes.
- Transmitter FIFO trigger points at 0, 4, 8, and 16 Bytes.
- Register locations conform to the “550” industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

7.8.1.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock for on-board communication in low noise conditions. This is accomplished by changing the over sampling from 16× to 14× and altering the rate generation logic.

Features

- Each high-speed UART has 64-byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1, 4, 8, 16, 32, and 48 B.
- Transmitter FIFO trigger points at 0, 4, and 8 B.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- The three high speed UARTs only support (8N1) 8-bit data word length, 1-stop bit, no parity, and no flow control as a the communications protocol.
- Each UART includes an internal loopback mode.

7.8.2 SPI serial I/O controller

The LPC3220/30/40/50 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

7.9.2 Keyboard scanner

The keyboard scanner function can automatically scan a keyboard of up to 64 keys in an 8×8 matrix. In operation, the keyboard scanner's internal state machine will normally be in an idle state, with all KEY_ROWn pins set high, waiting for a change in the column inputs to indicate that one or more keys have been pressed.

When a keypress is detected, the matrix is scanned by setting one output pin high at a time and reading the column inputs. After de-bouncing, the keypad state is stored and an interrupt is generated. The keypad is then continuously scanned waiting for 'extra key pressed' or 'key released'. Any new keypad state is scanned and stored into the matrix registers followed by a new interrupt request to the interrupt controller. It is possible to detect and separate up to 64 multiple keys pressed.

7.9.2.1 Features

- Supports up to 64 keys in 8×8 matrix.
- Programmable de-bounce period.
- A key press can wake up the CPU from Stop mode.

7.9.3 Touch screen controller and 10-bit ADC

The LPC3220/30/40/50 microcontrollers includes Touch Screen Controller (TSC) hardware, which automatically measures and determines the X and Y coordinates where a touch screen is pressed. In addition, the TSC can measure an analog input signal on the AUX_IN pin.

Optionally, the TSC can operate as an Analog-to-Digital Converter (ADC). The ADC supports three channels and uses 10-bit successive approximation to produce results with a resolution of 10 bits in 11 clock cycles.

The analog portion of the ADC has its own power supply to enhance the low noise characteristics of the converter. This voltage is only supplied internally when the core has voltage. However, the ADC block is not affected by any difference in ramp-up time for VDD_AD and VDD_CORE voltage supplies.

7.9.3.1 Features

- Measurement range of 0 V to VDD_AD (nominally 3.3 V).
- Low-noise ADC.
- 10-bit resolution.
- Three input channels.
- Uses 32 kHz RTC clock or peripheral clock.

7.9.4 Real-Time Clock (RTC) and battery RAM

The RTC runs at 32768 Hz using a very low power oscillator. The RTC counts seconds and can generate alarm interrupts that can wake up the device from Stop mode. The RTC clock can also clock the 397x PLL, the Millisecond Timer, the ADC, the Keyboard Scanner and the PWMs. The RTC up-counter value represents a number of seconds elapsed since second 0, which is an application determined time. The RTC counter will reach maximum value after about 136 years. The RTC down-counter is initiated with all ones.

Two 32-bit match registers are readable and writable by the processor. A match will result in an interrupt provided that the interrupt is enabled. The ONSW output pin can also be triggered by a match event and cause an external power supply to turn on all of the operating voltages, as a way to startup after power has been removed.

The RTC block is implemented in a separate voltage domain. The block is supplied via a separate supply pin from a battery or other power source.

The RTC block also contains 32 words (128 bytes) of very low voltage SRAM. This SRAM is able to hold its contents down to the minimum RTC operating voltage.

7.9.4.1 Features

- Measures the passage of time in seconds.
- 32-bit up and down seconds counters.
- Ultra-low power design to support battery powered systems.
- Dedicated 32 kHz oscillator.
- An output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC.
- Two 32-bit match registers with interrupt option.
- 32 words (128 bytes) of very low voltage SRAM.
- The RTC and battery RAM power have an independent power domain and dedicated supply pins, which can be powered from a battery or power supply.

Remark: The LPC3220/30/40/50 will run at voltages down to 0.9 V at frequencies below 14 MHz. However, the ARM core cannot access the RTC registers and battery RAM when the core supply voltage is at 0.9 V and the RTC supply is at 1.2 V.

7.9.5 Enhanced 32-bit timers/external event counters

The LPC3220/30/40/50 includes six 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.9.5.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit pre-scaler.
- Counter or Timer operation.
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - continuous operation with optional interrupt generation on match
  - stop timer on match with optional interrupt generation
  - reset timer on match with optional interrupt generation
- Up to four external outputs corresponding to match registers, with the following capabilities:

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Notes	Min	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)		[2]	−0.5	+1.4	V
$V_{DD(EMC)}$	external memory controller supply voltage		[3]	−0.5	+4.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		[4]	−0.5	+4.6	V
$V_{DD(IO)}$	input/output supply voltage		[5]	−0.5	+4.6	V
V_{IA}	analog input voltage			−0.5	+4.6	V
V_I	input voltage	1.8 V pins	[6]	−0.5	+2.4	V
		3.3 V pins	[6]	−0.5	+4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
T_{stg}	storage temperature			−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	max. junction temp 125 °C max. ambient temp 85 °C	[7]	-	1.12	W
V_{ESD}	electrostatic discharge voltage	HBM	[8]	-	2500	V
		CDM	[9]	-	1000	V

[1] The following applies to Table 7:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core, PLL, oscillator, and RTC supplies; applies to pins VDD_CORE, VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, VDD_PLLUSB, VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[3] I/O pad supply; applies to domains VDD_EMC.

[4] Applies to VDD_AD pins.

[5] Applies to pins in the following domains VDD_IOA, VDD_IOB, VDD_IOC, and VDD_IOD.

[6] Including voltage on outputs in 3-state mode.

[7] Based on package heat transfer, not device power consumption. Calculated package thermal resistance ($Theta_{JA}$): 35.766 °C/W (with JEDEC Test Board and 0 m/s airflow, ±15 % accuracy).

[8] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[9] Charge device model per AEC-Q100-011.

10. Static characteristics

Table 8. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)	core supply voltage for full performance; 266 MHz (see Figure 4); VDD_CORE supply domain	[2]	1.31	1.35	1.39	V
		core supply voltage for normal performance; 208 MHz (see Figure 4); VDD_CORE supply domain	[2]	1.1	1.2	1.39	V
		core supply voltage for reduced power; up to 14 MHz CPU; VDD_CORE supply domain	[2]	0.9	-	1.39	V
		RTC supply voltage; VDD_RTC supply domain	[3]	0.9	-	1.39	V
		PLL and oscillator supply voltage	[4]	1.1	1.2	1.39	V
$V_{DD(EMC)}$	external memory controller supply voltage	in 1.8 V range	[5]	1.7	1.8	1.95	V
		in 2.5 V range	[6]	2.3	2.5	2.7	V
		in 3.3 V range	[7]	2.7	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage	VDD_IOA, VDD_IOB, and VDD_IOD supply domain in 1.8 V range		1.7	1.8	1.95	V
		in 3.3 V range		2.7	3.3	3.6	V
		VDD_IOC supply domain in 1.8 V range		1.7	1.8	1.95	V
		in 3.3 V range		2.3	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	applies to pins in VDD_AD power domain		2.7	3.3	3.6	V

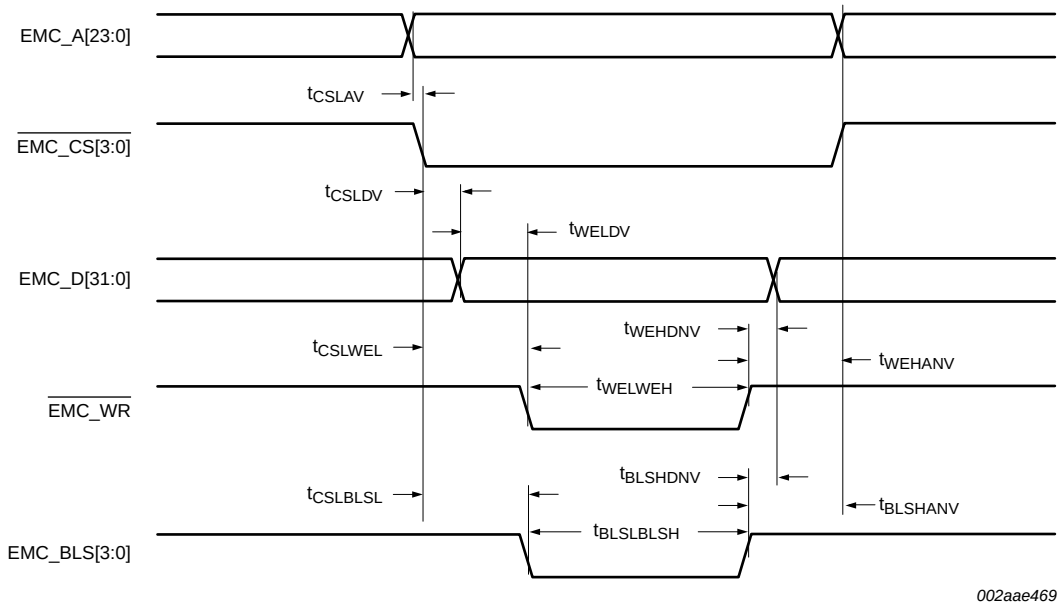


Fig 8. External memory write access

11.4 DDR SDRAM controller

Table 14. EMC DDR SDRAM memory interface dynamic characteristics[1]

C_L = 25 pF, T_{amb} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typical	Max	Unit
f_{oper}	operating frequency			-	104	133	MHz
t_{CK}	clock cycle time			7.5	9.6	-	ns
t_{CL}	CK LOW-level width			-	$0.5 \times t_{CK}$	-	ns
t_{CH}	CK HIGH-level width			-	$0.5 \times t_{CK}$	-	ns
$t_{d(V)ctrl}$	control valid delay time		[2][3]	-	(CMD_DLY × 0.25) + 1.5	-	ns
$t_{h(ctrl)}$	control hold time		[2][3]	-	(CMD_DLY × 0.25) − 1.5	-	ns
$t_{d(AV)}$	address valid delay time		[2]	-	(CMD_DLY × 0.25) + 1.5	-	ns
$t_{h(A)}$	address hold time		[2]	-	(CMD_DLY × 0.25) − 1.5	-	ns
$t_{su(Q)}$	data output set-up time	EMC_D[31:0] and EMC_DQM[3:0] to EMC_DQS[1:0] out	[5]	$0.08 \times t_{CK}$	$0.15 \times t_{CK}$	$0.25 \times t_{CK}$	ns
$t_{h(Q)}$	data output hold time	EMC_D[31:0] and EMC_DQM[3:0] to EMC_DQS[1:0] out	[5]	$0.25 \times t_{CK}$	$0.35 \times t_{CK}$	$0.42 \times t_{CK}$	ns
t_{DQSH}	DQS HIGH time	for WRITE command		-	$0.5 \times t_{CK}$	-	ns
t_{DQSL}	DQS LOW time	for WRITE command		-	$0.5 \times t_{CK}$	-	ns
t_{DQSS}	WRITE command to first DQS latching transition time	for DQS out		-	t_{CK} + 0.7	-	ns
t_{DSS}	DQS falling edge to CK set-up time	for DQS in		-	$0.5 \times t_{CK}$	-	ns
t_{DSH}	DQS falling edge hold time from CK	for DQS in		-	$0.5 \times t_{CK}$	-	ns
$t_{d(DQS)}$	DQS delay time	for DQS in	[4]	-	DQS_DELAY	-	ns
$t_{su(D)}$	data input set-up time			-	0.3	-	ns
$t_{h(D)}$	data input hold time			-	0.5	-	ns

[1] All values valid for EMC pads set to fast slew rate at 1.8 V unless otherwise specified (see SDRAMCLK_CTRL register in the *LPC32x0 User manual*).

[2] CMD_DLY = COMMAND_DELAY bit field in SDRAMCLK_CTRL[18:14] register, see *External Memory Controller (EMC) chapter in LPC32x0 User manual*.

[3] Applies to signals EMC_DQM[3:0], $\overline{\text{EMC\_DYCS}}$[1:0], $\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_WR}}$, EMC_CKE[1:0].

[4] DQS_DELAY, see *LPC32x0 User manual, External Memory Controller Chapter, Section 8 DDR DQS delay calibration* for details on configuring this value.

[5] Test conditions for measurements: T_{amb} = −40 °C to +85 °C; operating frequency range f_{oper} = 52 MHz to 133 MHz; EMC_DQM[3:0] and EMC_D[31:0] driving 2 inches of 50 Ω characteristic impedance trace with 10 pF capacitive load; no external source series termination resistors used. EMC pads set to fast slew rate at 1.8 V or 2.5 V (see SDRAMCLK_CTRL register in the *LPC32x0 User manual*).

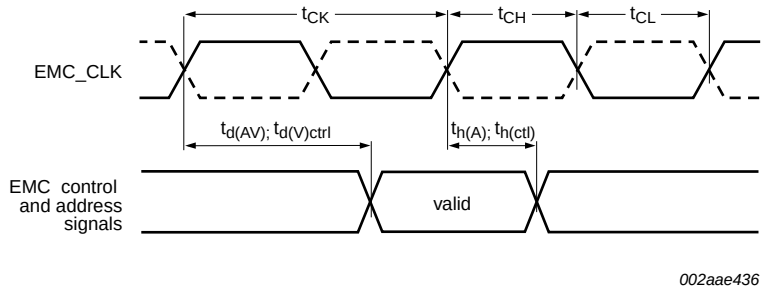


Fig 10. DDR control timing parameters

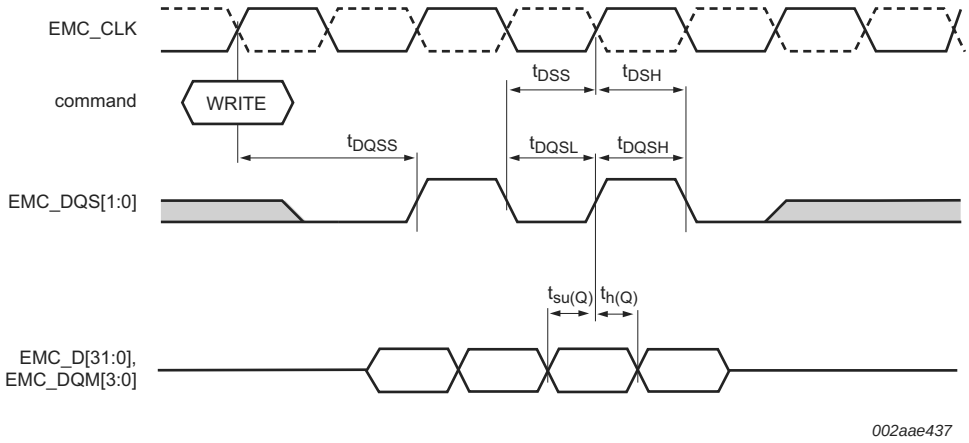
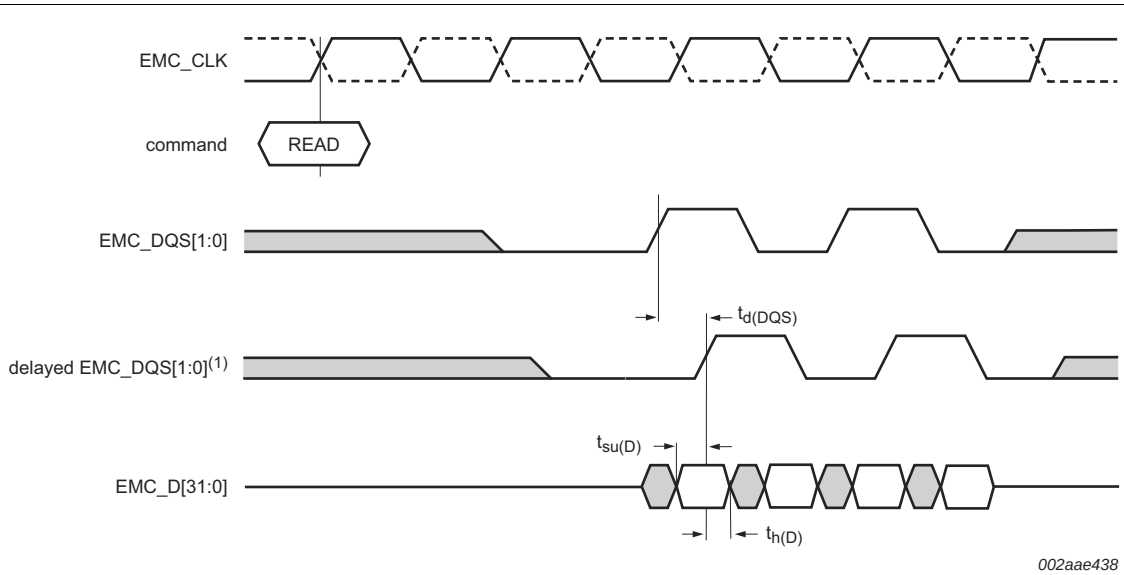


Fig 11. DDR write timing parameters



(1) The delay of the EMC_DQS[1:0] signal is determined by the DQS_DELAY settings. See *LPC32x0 User manual, External Memory Controller Chapter, section DDR DQS delay calibration* for details on configuring this value.

Fig 12. DDR read timing parameters

Table 18. Dynamic characteristics of SLC NAND flash memory controller *…continued*
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WH}	$\overline{WE}$ HIGH hold time	write	[1][6][7]	-	$T_{HCLK} \times (Wsu + Wh)$	-	ns
t_{WHR}	$\overline{WE}$ HIGH to $\overline{RE}$ LOW time	write	[1][7][9]	-	$(T_{HCLK} \times Wh) + (2 \times T_{HCLK} \times Wb)$	-	ns
t_{WP}	$\overline{WE}$ pulse width	write	[1][8]	-	$T_{HCLK} \times Ww$	-	ns
t_{REHRBL}	$\overline{RE}$ HIGH to R/$\overline{B}$ LOW time	write	[1][3][5]	-	$(T_{HCLK} \times Rh) + (2 \times T_{HCLK} \times Rb)$	-	ns

[1] T_{HCLK} = 1/HCLK

[2] Rsu = bit field R_SETUP[3:0] in register SLC_TAC[3:0] for reads

[3] Rh = bit field R_HOLD[3:0] in register SLC_TAC[7:4] for reads

[4] Rw = bit field R_WIDTH[3:0] in register SLC_TAC[11:8] for reads

[5] Rb = bit field R_RDY[3:0] in register SLC_TAC[15:12] for reads

[6] Wsu = bit field W_SETUP[3:0] in register SLC_TAC[19:16] for writes

[7] Wh = bit field W_HOLD[3:0] in register SLC_TAC[23:20] for writes

[8] Ww = bit field W_WIDTH[3:0] in register SLC_TAC[27:24] for writes

[9] Wb = bit field W_RDY[3:0] in register SLC_TAC[31:28] for writes

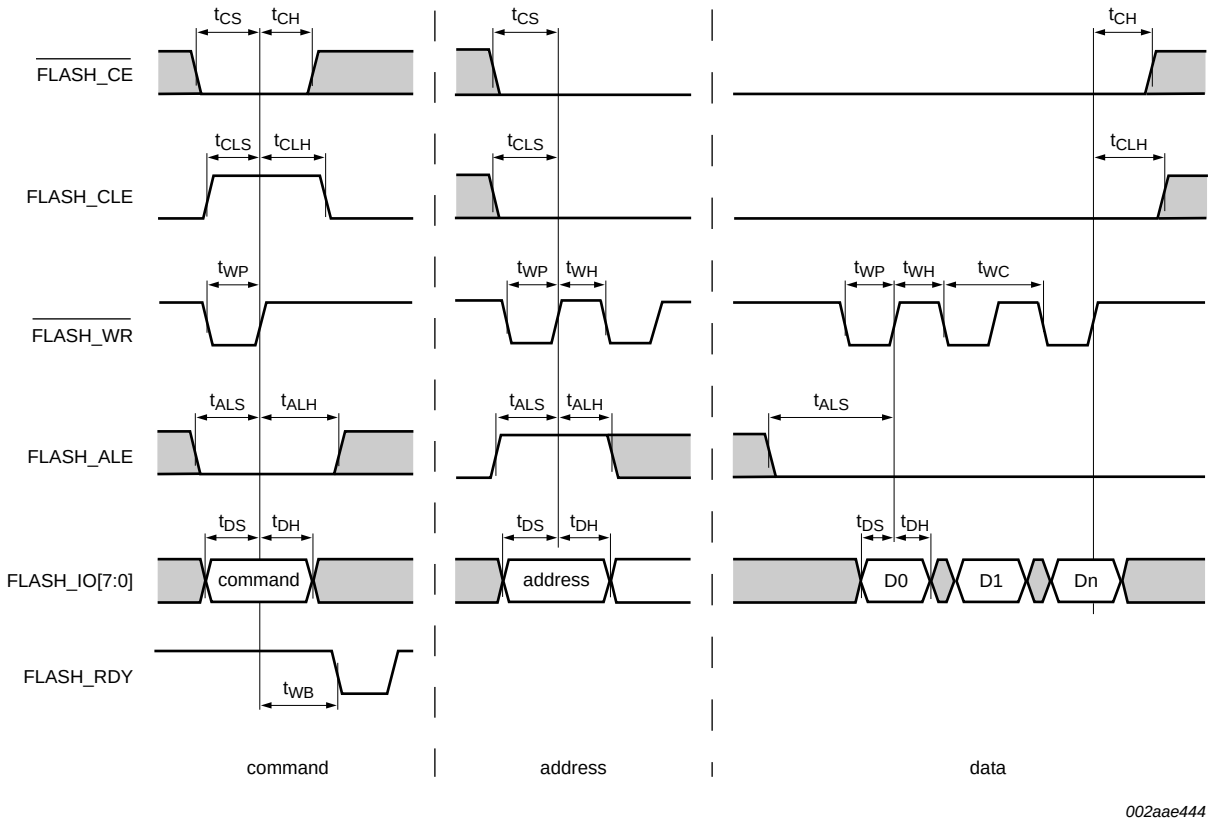
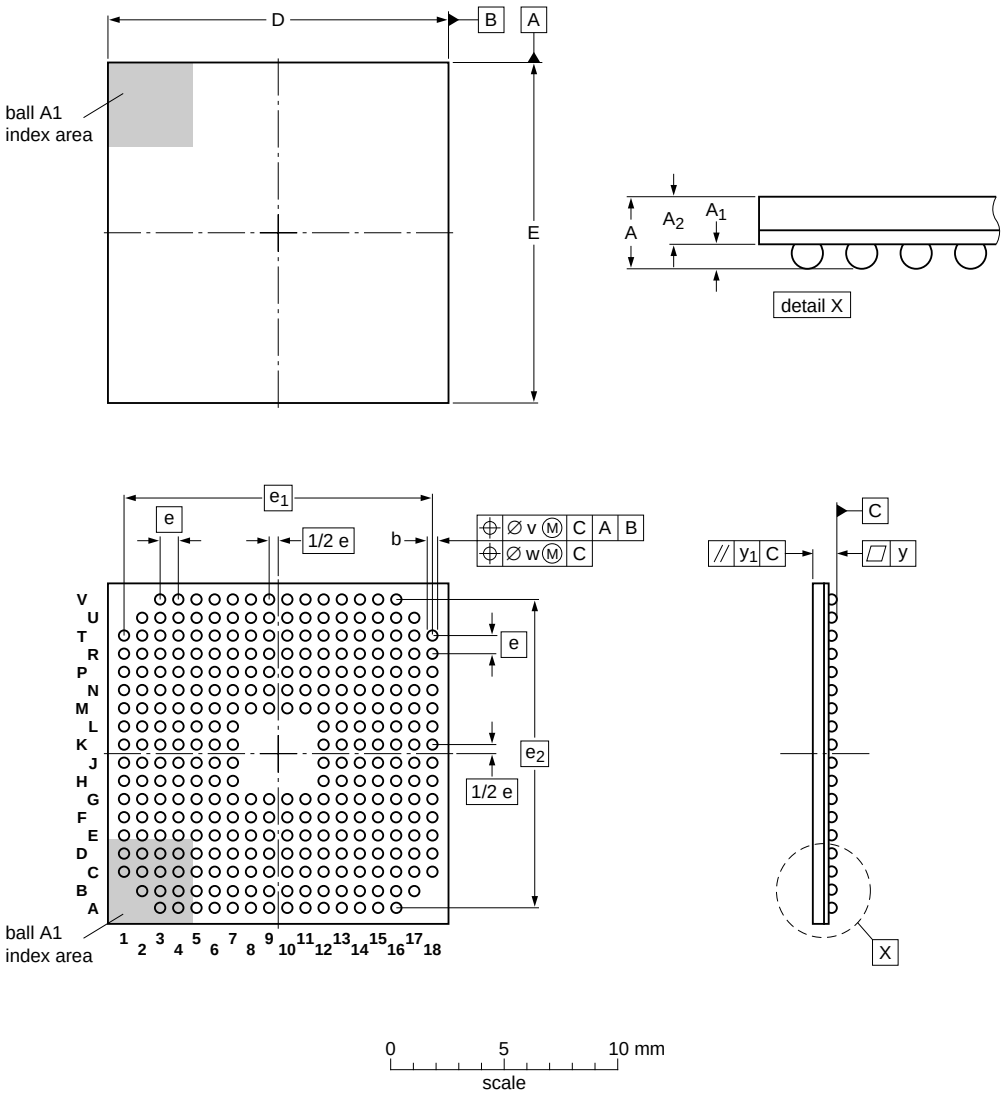


Fig 17. MLC NAND flash memory write timing (writing to NAND flash)

13. Package outline

TFBGA296: plastic thin fine-pitch ball grid array package; 296 balls **SOT1048-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.80 0.65	0.5 0.4	15.1 14.9	15.1 14.9	0.8	13.6	13.6	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1048-1		MO-216				~~07-10-19~~ 07-11-02

Fig 25. Package outline SOT1048-1 (TFBGA296)

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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