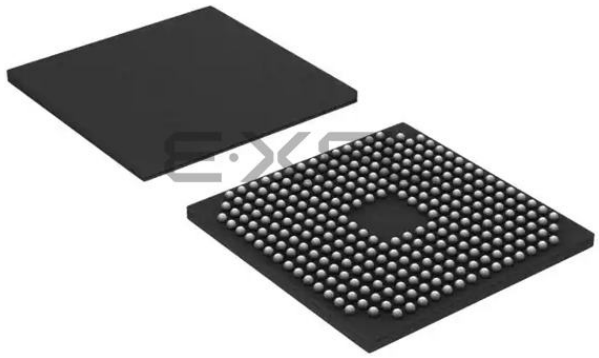

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3220fet296-551

- Six enhanced timer/counters which are architecturally identical except for the peripheral base address. Two capture inputs and two match outputs are pinned out to four timers. Timer 1 brings out a third match output, timers 2 and 3 bring out all four match outputs, timer 4 has one match output, and timer 5 has no inputs or outputs.
- 32-bit millisecond timer driven from the RTC clock. This timer can generate interrupts using two match registers.
- WatchDog timer clocked by the peripheral clock.
- Two single-output PWM blocks.
- Motor control PWM.
- Keyboard scanner function allows automatic scanning of an up to 8 × 8 key matrix.
- Up to 18 external interrupts.

- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation Trace Buffer (ETB) with 2048 × 24 bit RAM allows trace via JTAG.
- Stop mode saves power while allowing many peripheral functions to restart CPU activity.
- On-chip crystal oscillator.
- An on-chip PLL allows CPU operation up to the maximum CPU rate without the requirement for a high frequency crystal. Another PLL allows operation from the 32 kHz RTC clock rather than the external crystal.
- Boundary scan for simplified board testing.
- User-accessible unique serial ID number for each chip.
- TFBGA296 package with a 15 mm × 15 mm × 0.7 mm body.

3. Applications

- Consumer
- Medical
- Industrial
- Network control

6. Pinning information

6.1 Pinning

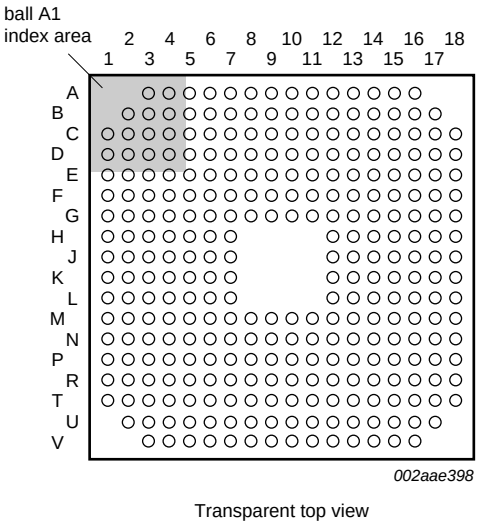


Fig 2. Pin configuration for SOT1048-1 (TFBGA296)

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A					
				A3	I2C2_SCL
A4	I2S1TX_CLK/MAT3[0]	A5	I2C1_SCL	A6	MS_BS/MAT2[1]
A7	MS_DIO1/MAT0[1]	A8	MS_DIO0/MAT0[0]	A9	SPI2_DATIO/MOSI1/LCDVD[20][1]
A10	SPI2_DATIN/MISO1/ LCDVD[21][1]/GPI_27	A11	GPIO_1	A12	GPIO_0
A13	GPO_21/U4_TX/LCDVD[3][1]	A14	GPO_15/MCOA1/LCDFP[1]	A15	GPO_7/LCDVD[2][1]
A16	GPO_6/LCDVD[18][1]				
Row B					
		B2	GPO_20	B3	GPO_5
B4	I2S1TX_WS/CAP3[0]	B5	P0[0]/I2S1RX_CLK	B6	I2C1_SDA
B7	MS_SCLK/MAT2[0]	B8	MS_DIO2/MAT0[2]	B9	SPI1_DATIO/MOSI0/MCI2
B10	SPI2_CLK/SCK1/LCDVD[23][1]	B11	GPIO_4/SSEL1/LCDVD[22][1]	B12	GPO_12/MCOA2/LCDLE[1]
B13	GPO_13/MCOB1/LCDDCLK[1]	B14	GPO_2/MAT1[0]/LCDVD[0][1]	B15	GPI_19/U4_RX
B16	GPI_8/KEY_COL6/ SPI2_BUSY/ENET_RX_DV[2]	B17	n.c.		
Row C					
C1	$\overline{\text{FLASH\_RD}}$	C2	GPO_19	C3	GPO_0/TST_CLK1
C4	$\overline{\text{USB\_ATX\_INT}}$	C5	USB_SE0_VM/U5_TX	C6	TST_CLK2
C7	GPI_6/HSTIM_CAP/ ENET_RXD2[2]	C8	MS_DIO3/MAT0[3]	C9	SPI1_CLK/SCK0

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Power supply domain	Type	Description
ADIN0/TS_YM	U15	VDD_AD	analog in	ADC input 0/touch screen Y minus
ADIN1/TS_XM	T14	VDD_AD	analog in	ADC input 0/touch screen X minus
ADIN2/TS_AUX_IN	V16	VDD_AD	analog in	ADC input 2/touch screen AUX input
DBGEN	G14	VDD_IOD	I: PD	Device test input LOW = JTAG in-circuit debug available; normal operation. HIGH = I/O cell boundary scan test; for board assembly BSDL test.
EMC_A[0]/P1[0]	L3	VDD_EMC	I/O	EMC address bit 0
			I/O	Port 1 GPIO bit 0
EMC_A[1]/P1[1]	L4	VDD_EMC	I/O	EMC address bit 1
			I/O	Port 1 GPIO bit 1
EMC_A[2]/P1[2]	M1	VDD_EMC	I/O	EMC address bit 2
			I/O	Port 1 GPIO bit 2
EMC_A[3]/P1[3]	M2	VDD_EMC	I/O	EMC address bit 3
			I/O	Port 1 GPIO bit 3
EMC_A[4]/P1[4]	M3	VDD_EMC	I/O	EMC address bit 4
			I/O	Port 1 GPIO bit 4
EMC_A[5]/P1[5]	N1	VDD_EMC	I/O	EMC address bit 5
			I/O	Port 1 GPIO bit 5
EMC_A[6]/P1[6]	N2	VDD_EMC	I/O	EMC address bit 6
			I/O	Port 1 GPIO bit 6
EMC_A[7/P1[7]	N3	VDD_EMC	I/O	EMC address bit 7
			I/O	Port 1 GPIO bit 7
EMC_A[8]/P1[8]	M4	VDD_EMC	I/O	EMC address bit 8
			I/O	Port 1 GPIO bit 8
EMC_A[9]/P1[9]	P1	VDD_EMC	I/O	EMC address bit 9
			I/O	Port 1 GPIO bit 9
EMC_A[10]/P1[10]	P2	VDD_EMC	I/O	EMC address bit 10
			I/O	Port 1 GPIO bit 10
EMC_A[11]/P1[11]	P3	VDD_EMC	I/O	EMC address bit 11
			I/O	Port 1 GPIO bit 11
EMC_A[12]/P1[12]	N4	VDD_EMC	I/O	EMC address bit 12
			I/O	Port 1 GPIO bit 12
EMC_A[13]/P1[13]	R1	VDD_EMC	I/O	EMC address bit 13
			I/O	Port 1 GPIO bit 13
EMC_A[14]/P1[14]	R2	VDD_EMC	I/O	EMC address bit 14
			I/O	Port 1 GPIO bit 14

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
P0[1]/ I2S1RX_WS	D7	VDD_IOB	I/O	Port 0 GPIO bit 1
			I/O	I^2S1 receive word select
P0[2]/ I2S0RX_SDA/ LCDVD[4]	M17	VDD_IOA	I/O	Port 0 GPIO bit 2
			I/O	I^2S0 receive data
			I/O	LCD data bit 4 (LPC3230 and LPC3250 only)
P0[3]/ I2S0RX_CLK/ LCDVD[5]	M18	VDD_IOA	I/O	Port 0 GPIO bit 3
			I/O	I^2S0 receive clock
			I/O	LCD data bit 5 (LPC3230 and LPC3250 only)
P0[4]/ I2S0RX_WS/ LCDVD[6]	L15	VDD_IOA	I/O	Port 0 GPIO bit 4
			I/O	I^2S0 receive word select
			I/O	LCD data bit 6 (LPC3230 and LPC3250 only)
P0[5]/ I2S0TX_SDA/ LCDVD[7]	L16	VDD_IOA	I/O	Port 0 GPIO bit 5
			I/O	I^2S0 transmit data
			I/O	LCD data bit 7 (LPC3230 and LPC3250 only)
P0[6]/ I2S0TX_CLK/ LCDVD[12]	L17	VDD_IOA	I/O	Port 0 GPIO bit 6
			I/O	I^2S0 transmit clock
			I/O	LCD data bit 12 (LPC3230 and LPC3250 only)
P0[7]/ I2S0TX_WS/ LCDVD[13]	L18	VDD_IOA	I/O	Port 0 GPIO bit 7
			I/O	I^2S0 transmit word select
			I/O	LCD data bit 13 (LPC3230 and LPC3250 only)
PLL397_LOOP	R14	VDD_PLL397	analog filter	PLL397 loop filter (for external components)
PWM_OUT1/ LCDVD[16]	D14	VDD_IOD	O	PWM1 out
			O	LCD data bit 16 (LPC3230 and LPC3250 only)
PWM_OUT2/INTSTAT/ LCDVD[19]	D15	VDD_IOD	O	PWM2 output/internal interrupt status[1]
			O	LCD data bit 19 (LPC3230 and LPC3250 only)
$\overline{\text{RESET}}$	M14	VDD_RTC	I	Reset input, active LOW
$\overline{\text{RESOUT}}$	G4	VDD_IOC	O	Reset out. Reflects external and WDT reset
RTCX_IN	P16	VDD_RTC	analog in	RTC oscillator input
RTCX_OUT	P17	VDD_RTC	analog out	RTC oscillator output
SPI1_CLK/ SCK0	C9	VDD_IOD	O	SPI1 clock out
			O	SSP0 clock out
SPI1_DATIN/ MISO0/ GPI_25/ MCI1	C10	VDD_IOD	I/O	SPI1 data in
			I/O	SSP0 MISO
			I/O	General purpose input bit 25
			I	Motor control channel 1 input
SPI1_DATIO/ MOSI0/ MCI2	B9	VDD_IOD	I/O	SPI1 data out (and optional input)
			I/O	SSP0 MOSI
			I	Motor control channel 2 input

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
SPI2_CLK/ SCK1/ LCDVD[23]	B10	VDD_IOD	I/O	SPI2 clock out
			I/O	SSP1 clock out
			I/O	LCD data bit 23 (LPC3230 and LPC3250 only)
SPI2_DATIO/ MOSI1/ LCDVD[20]	A9	VDD_IOD	I/O	SPI2 data out (and optional input)
			I/O	SSP1 MOSI
			I/O	LCD data bit 20 (LPC3230 and LPC3250 only)
SPI2_DATIN/ MISO1/ LCDVD[21]/ GPI_27	A10	VDD_IOD	I/O	SPI2 data in
			I/O	SSP1 MISO
			I/O	LCD data 21 (LPC3230 and LPC3250 only)
			I/O	General purpose input bit 27
SYSCLKEN/ LCDVD[15]	G17	VDD_IOD	I/O T	Clock request out for external clock source
			I/O T	LCD data bit 15 (LPC3230 and LPC3250 only)
SYSX_IN	T17	VDD_OSC	analog in	System clock oscillator input
SYSX_OUT	R15	VDD_OSC	analog out	System clock oscillator output
TS_XP	R13	VDD_AD	I/O	Touchscreen X output
TS_YP	U16	VDD_AD	I/O	Touchscreen Y output
TST_CLK2	C6	VDD_IOB	O	Test clock 2 out
U1_RX/CAP1[0]/ GPI_15	K15	VDD_IOA	I/O	HS UART 1 receive
			I/O	Timer 1 capture input 0
			I/O	General purpose input bit 15
U1_TX	K16	VDD_IOA	O	HS UART 1 transmit
U2_HCTS/ U3_CTS/GPI_16	J18	VDD_IOA	I/O	HS UART 2 Clear to Send input
			I	UART 3 Clear to Send
			I/O	General purpose input bit 16
U2_RX/ U3_DSR/GPI_17	K18	VDD_IOA	I/O	HS UART 2 receive
			I/O	UART 3 data set ready
			I/O	General purpose input bit 17
U2_TX/U3_DTR	K17	VDD_IOA	O	HS UART 2 transmit
			O	UART 3 data terminal ready out
U3_RX/ GPI_18	J14	VDD_IOD	I/O	UART 3 receive
			I/O	General purpose input bit 18
U3_TX	J17	VDD_IOD	O	UART 3 transmit
U5_RX/ GPI_20	F18	VDD_IOD	I/O	UART 5 receive
			I	General purpose input bit 20
U5_TX	H15	VDD_IOD	O	UART 5 transmit
U6_IRRX/ GPI_21	F17	VDD_IOD	I/O	UART 6 receive (with IrDA)
			I	General purpose input bit 21
U6_IRTX	G16	VDD_IOD	O	UART 6 transmit (with IrDA)

7.1.3.2 Embedded trace buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer (ETB) of 2048 × 24 bits captures the trace information under software debugger control. Data from the ETB is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

7.2 AHB matrix

The LPC3220/30/40/50 has a multi-layer AHB matrix for inter-block communication. AHB is an ARM defined high-speed bus, which is part of the ARM bus architecture. AHB is a high-bandwidth low-latency bus that supports multi-master arbitration and a bus grant/request mechanism. For systems that have only one (CPU), or two (CPU and DMA) bus masters a simple AHB works well. However, if a system requires multiple bus masters and the CPU needs access to external memory, a single AHB bus can cause a bottleneck.

To increase performance, the LPC3220/30/40/50 uses an expanded AHB architecture known as Multi-layer AHB. A Multi-layer AHB replaces the request/grant and arbitration mechanism used in a simple AHB with an interconnect matrix that moves arbitration out toward the slave devices. Thus, if a CPU and a DMA controller want access to the same memory, the interconnect matrix arbitrates between the two when granting access to the memory. This advanced architecture allows simultaneous access by bus masters to different resources with an increase in arbitration complexity. In this architectural implementation, removing guaranteed central arbitration and allowing more than one bus master to be active at the same time provides better overall microcontroller performance.

In the LPC3220/30/40/50, the multi-Layer AHB system has a separate bus for each of seven AHB Masters:

- CPU data bus
- CPU instruction bus
- General purpose DMA Master 0
- General purpose DMA Master 1
- Ethernet controller
- USB controller
- LCD controller

There are no arbitration delays unless two masters attempt to access the same slave at the same time.

7.4 Internal memory

7.4.1 On-chip ROM

The built-in 16 kB ROM contains a program which runs a boot procedure to load code from one of four external sources, UART 5, SSP0 (SPI mode), EMC Static CS0 memory, or NAND FLASH.

After reset, execution always begins from the internal ROM. The bootstrap software first reads the $\overline{\text{SERVICE}}$ input (GPI_1). If $\overline{\text{SERVICE}}$ is LOW, the bootstrap starts a service boot and can download a program over serial link UART 5 to IRAM and transfer execution to the downloaded code.

If the $\overline{\text{SERVICE}}$ pin is HIGH, the bootstrap routine jumps to normal boot. The normal boot process first tests SPI memory for boot information if present it uploads the boot code and transfers execution to the uploaded software. If the SPI is not present or no software is loaded, the bootloader will test the EMC Static CS0 memory for the presence of boot code and if present boots from static memory, If this test fails the boot loader will test external NAND flash for boot code and boot if code is present.

The boot loader consumes no user memory space because it is in ROM.

7.4.2 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8, 16, or 32 bit memory. The LPC3220/30/40/50 provides 256 kB of internal SRAM.

7.5 External memory interfaces

The LPC3220/30/40/50 includes three external memory interfaces, NAND Flash controllers, Secure Digital Memory Controller, and an external memory controller for SDRAM, DDR SDRAM, and Static Memory devices.

7.5.1 NAND flash controllers

The LPC3220/30/40/50 includes two NAND flash controllers, one for multi-level cell NAND flash devices and one for single-level cell NAND flash devices. The two NAND flash controllers use the same pins to interface to external NAND flash devices, so only one interface is active at a time.

7.5.1.1 Multi-Level Cell (MLC) NAND flash controller

The MLC NAND flash controller interfaces to either multi-level or single-level NAND flash devices. An external NAND flash device is used to allow the bootloader to automatically load a portion of the application code into internal SRAM for execution following reset.

The MLC NAND flash controller supports small (528 byte) and large (2114 byte) pages. Programmable NAND timing parameters allow support for a variety of NAND flash devices. A built-in Reed-Solomon encoder/decoder provides error detection and correction capability. A 528 byte data buffer reduces the need for CPU supervision during loading. The MLC NAND flash controller also provides DMA support.

7.5.1.2 Single-Level Cell (SLC) NAND flash controller

The SLC NAND flash controller interfaces to single-level NAND flash devices. DMA page transfers are supported, including a 20-byte DMA read and write FIFO. Hardware support for ECC (Error Checking and Correction) is included for the main data area. Software can correct a single bit error.

7.5.2 SD card controller

The SD interface allows access to external SD memory cards. The SD card interface conforms to the *SD Memory Card Specification Version 1.01*.

7.5.2.1 Features

- 1-bit and 4-bit data line interface support.
- DMA is supported through the system DMA controller.
- Provides all functions specific to the SD memory card. These include the clock generation unit, power management control, command and data transfer.

7.5.3 External memory controller

The LPC3220/30/40/50 includes a memory controller that supports data bus SDRAM, DDR SDRAM, and static memory devices. The memory controller provides an interface between the system bus and external (off-chip) memory devices.

The controller supports 16-bit and 32-bit wide SDR SDRAM devices of 64 Mbit, 128 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit sizes, as well as 16-bit wide data bus DDR SDRAM devices of 64 Mbit, 128 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit sizes. Two dynamic memory chip selects are supplied, supporting two groups of SDRAM:

- DYCS0 in the address range 0x8000 0000 to 0x9FFF FFFF
- DYCS1 in the address range 0xA000 0000 to 0xBFFF FFFF

The memory controller also supports 8-bit, 16-bit, and 32-bit wide asynchronous static memory devices, including RAM, ROM, and flash, with or without asynchronous page mode. Four static memory chip selects are supplied for SRAM devices:

- CS0 in the address range 0xE000 0000 to 0xE0FF FFFF
- CS1 in the address range 0xE100 0000 to 0xE1FF FFFF
- CS2 in the address range 0xE200 0000 to 0xE2FF FFFF
- CS3 in the address range 0xE300 0000 to 0xE3FF FFFF

The SDRAM controller uses three data ports to allow simultaneous requests from multiple on-chip AHB bus masters and has the following features.

- Dynamic memory interface supports SDRAM, DDR-SDRAM, and low-power variants.
- Read and write buffers to reduce latency and improve performance.
- Static memory features include
  - asynchronous page mode read
  - programmable wait states
  - bus turnaround cycles
  - output enable and write enable delays

  - extended wait
- Power-saving modes dynamically control EMC_CKE[1:0] and EMC_CLK.
- Dynamic memory self-refresh mode supported by software.
- Controller supports 2 k, 4 k, and 8 k row address synchronous memory parts. That is, typical 512 MB, 256 MB, 128 MB, and 16 MB parts, with 8, 16, or 32 data bits per device.
- Two reset domains enable dynamic memory contents to be preserved over a soft reset.
- This controller does not support synchronous static memory devices (burst mode devices).

7.6 AHB master peripherals

The LPC3220/30/40/50 implements four AHB master peripherals, which include a General Purpose Direct Memory Access (GPDMA) controller, a 10/100 Ethernet Media Access Controller (MAC), a Universal Serial Bus (USB) controller, and an LCD controller. Each of these four peripherals contain an integral DMA controller optimized to support the performance demands of the peripheral.

7.6.1 General Purpose DMA (GPDMA) controller

The GPDMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the same AHB master, or one area by each master. The DMA controller supports the following peripheral device transfers.

- Secure Digital (SD) Memory interface
- High-speed UARTs
- I^2S0 and I^2S1 ports
- SPI1 and SPI2 interfaces
- SSP0 and SSP1 interfaces
- Memory

The DMA controls eight DMA channels with hardware prioritization. The DMA controller interfaces to the system via two AHB bus masters, each with a full 32-bit data bus width. DMA operations may be set up for 8-bit, 16-bit, and 32-bit data widths, and can be either big-endian or little-endian. Incrementing or non-incrementing addressing for source and destination are supported, as well as programmable DMA burst size. Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.

7.6.2 Ethernet MAC

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive

7.7 System functions

To enhance the performance of the LPC3220/30/40/50 incorporates the following system functions, an Interrupt Controller (INTC), a watchdog timer, a millisecond timer, and several power control features. These functions are described in the following sections

7.7.1 Interrupt controller

The interrupt controller is comprised of three basic interrupt controller blocks, supporting a total of 73 interrupt sources. Each interrupt source can be individually enabled/disabled and configured for high or low level triggering, or rising or falling edge triggering. Each interrupt may also be steered to either the FIQ or IRQ input of the ARM9. Raw interrupt status and masked interrupt status registers allow versatile condition evaluation. In addition to peripheral functions, each of the six general purpose input/output pins and 12 of the 22 general purpose input pins are connected directly to the interrupt controller.

7.7.2 Watchdog timer

The watchdog timer block is clocked by the main peripheral clock, which clocks a 32-bit counter. A match register is compared to the Timer. When configured for watchdog functionality, a match drives the match output low. The match output is gated with an enable signal that gives the opportunity to generate two type of reset signal: one that only resets chip internally, and another that goes through a programmable pulse generator before it goes to the external pin $\overline{\text{RESOUT}}$ and to the internal chip reset.

7.7.2.1 Features

- Programmable 32-bit timer.
- Internally resets the device if not periodically reloaded.
- Flag to indicate that a watchdog reset has occurred.
- Programmable watchdog pulse output on $\overline{\text{RESOUT}}$ pin.
- Can be used as a standard timer if watchdog is not used.
- Pause control to stop counting when core is in debug state.

7.7.3 Millisecond timer

The millisecond timer is clocked by 32 kHz RTC clock, so a prescaler is not needed to obtain a lower count rate.

The millisecond timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and the cause the Timer/Counter either continue to run, stop, or be reset.

7.7.3.1 Features

- 32-bit Timer/Counter, running from the 32 kHz RTC clock.
- Counter or Timer operation.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master. The SPI implementation on the LPC3220/30/40/50 does not support operation as a slave.

7.8.2.1 Features

- Supports slaves compatible with SPI modes 0 to 3.
- Half duplex synchronous transfers.
- DMA support for data transmit and receive.
- 1-bit to 16-bit word length.
- Choice of LSB or MSB first data transmission.
- 64 × 16-bit input or output FIFO.
- Bit rates up to 52 Mbit/s.
- Busy input function.
- DMA time out interrupt to allow detection of end of reception when using DMA.
- Timed interrupt to facilitate emptying the FIFO at the end of a transmission.
- SPI clock and data pins may be used as general purpose pins if the SPI is not used.
- Slave selects can be supported using GPO or GPIO pins

7.8.3 SSP serial I/O controller

The LPC3220/30/40/50 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.8.3.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of $\frac{1}{2}$ (Master mode) and $\frac{1}{2}$ (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.8.4 I^2C-bus serial I/O controller

There are two I^2C-bus interfaces in the LPC32x0 family of controllers. These I^2C blocks can be configured as a master, multi-master or slave supporting up to 400 kHz. The I^2C blocks also support 7 or 10 bit addressing. Each has a four word FIFO for both transmit and receive. An interrupt signal is available from each block.

There is a separate slave transmit FIFO. The slave transmit FIFO (TXS) and its level are only available when the controller is configured as a Master/Slave device and is operating in a multi-master environment. Separate TX FIFOs are needed in a multi-master because a controller might have a message queued for transmission when an external master addresses it to be come a slave-transmitter, a second source of data is needed.

Note that the I^2C clock must be enabled in the I2CCLK_CTRL register before using the I^2C. The I^2C clock can be disabled between communications, if used as a single master I^2C-bus interface, software has full control of when I^2C communication is taking place on the bus.

7.8.4.1 Features

- The two I^2C-bus blocks are standard I^2C-bus compliant interfaces that may be used in Single-master, Multi-master or Slave modes.
- Programmable clock to allow adjustment of I^2C-bus transfer rates.
- Bidirectional data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

7.8.5 I^2S-bus audio controller

The I^2S-bus provides a standard communication interface for digital audio applications The I^2S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. Each I^2S connection can act as a master or a slave. The master connection determines the frequency of the clock line and all other slaves are driven by this clock source. The two I^2S-bus interfaces on the LPC3220/30/40/50 provides a separate transmit and receive channel, providing a total of two transmit channels and two receive channels. Each I^2S channel supports monaural or stereo formatted data.

7.8.5.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- Supports standard sampling frequencies (8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz).
- Word select period can be configured in master mode (separately for I^2S input and output).
- Two eight-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop, and mute options separately for I^2S input and I^2S output.

7.9 Other peripherals

In addition to the communication peripherals there are many general purpose peripherals available in the LPC3220/30/40/50. Here is a list of the general purpose peripherals.

- GPI/O
- Keyboard scanner
- Touch screen controller and 10-bit Analog-to-Digital-Converter
- Real-time clock
- High-speed timer
- Four general purpose 32-bit timer/external event counters
- Two simple PWMs
- One motor control PWM

A short functional description of each of these peripherals is provided in the following sections.

7.9.1 General purpose parallel I/O

Some device pins that are not dedicated to a specific peripheral function have been designed to be general purpose inputs, outputs, or input/outputs. Also, some pins may be configured either as a specific peripheral function or a general purpose input, output, or input/output. A total of 51 pins can potentially be used as general purpose input/outputs, 24 as general purpose outputs, and 22 as general purpose inputs.

GPIO pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of GPIO and GPO outputs controlled by that register simultaneously. The value of the output register for standard GPIOs and GPO pins may be read back, as well as the current actual state of the port pins.

In addition to GPIO pins on port 0, port 1, and port 2, there are 22 GPI, 24 GPO, and six GPIO pins. When the SDRAM bus is configured for 16 data bits, 13 of the remaining SDRAM data pins may be used as GPIOs.

7.9.1.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- A single register selects direction for pins that support both input and output modes.
- Direction control of individual bits.
- For input/output pins, both the programmed output state and the actual pin state can be read.
- There are a total of 12 general purpose inputs, 24 general purpose outputs, and six general purpose input/outputs.
- Additionally, 13 SDRAM data lines may be used as GPIOs if a 16-bit SDRAM interface is used (rather than a 32-bit interface).

- set LOW on match
- set HIGH on match
- toggle on match
- do nothing on match

7.9.6 High-speed timer

The high-speed timer block is clocked by the main peripheral clock. The clock is first divided down in a 16-bit programmable pre-scale counter which clocks a 32-bit timer/counter.

The high-speed timer includes three match registers that are compared to the timer/counter value. A match can generate an interrupt and cause the timer/counter to either continue to run, stop, or be reset. The high-speed timer also includes two capture registers that can take a snapshot of the timer/counter value when an input signal transitions. A capture event may also generate an interrupt.

7.9.6.1 Features

- 32-bit timer/counter with programmable 16-bit pre-scaler.
- Counter or timer operation.
- Two 32-bit capture registers.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

7.9.7 Pulse Width Modulators (PWMs)

The LPC3220/30/40/50 provides two simple PWMs. They are clocked separately by either the main peripheral clock or the 32 kHz RTC clock. Both PWMs have a duty cycle programmable in 255 steps.

7.9.7.1 Features

- Clocked by the main peripheral clock or the 32 kHz RTC clock.
- Programmable 4-bit pre-scaler.
- Duty cycle programmable in 255 steps.
- Output frequency up to 50 kHz when using a 13 MHz peripheral clock.

7.9.8 Motor control pulse width modulator

The Motor Control PWM (MCPWM) provides a set of features for three-phase AC and DC motor control applications in a single peripheral. The MCPWM can also be configured for use in other generalized timing, counting, capture, and compare applications.

7.9.8.1 Features

- 32-bit timer
- 32-bit period register

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Notes	Min	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)		[2]	−0.5	+1.4	V
$V_{DD(EMC)}$	external memory controller supply voltage		[3]	−0.5	+4.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		[4]	−0.5	+4.6	V
$V_{DD(IO)}$	input/output supply voltage		[5]	−0.5	+4.6	V
V_{IA}	analog input voltage			−0.5	+4.6	V
V_I	input voltage	1.8 V pins	[6]	−0.5	+2.4	V
		3.3 V pins	[6]	−0.5	+4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
T_{stg}	storage temperature			−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	max. junction temp 125 °C max. ambient temp 85 °C	[7]	-	1.12	W
V_{ESD}	electrostatic discharge voltage	HBM	[8]	-	2500	V
		CDM	[9]	-	1000	V

[1] The following applies to Table 7:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core, PLL, oscillator, and RTC supplies; applies to pins VDD_CORE, VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, VDD_PLLUSB, VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[3] I/O pad supply; applies to domains VDD_EMC.

[4] Applies to VDD_AD pins.

[5] Applies to pins in the following domains VDD_IOA, VDD_IOB, VDD_IOC, and VDD_IOD.

[6] Including voltage on outputs in 3-state mode.

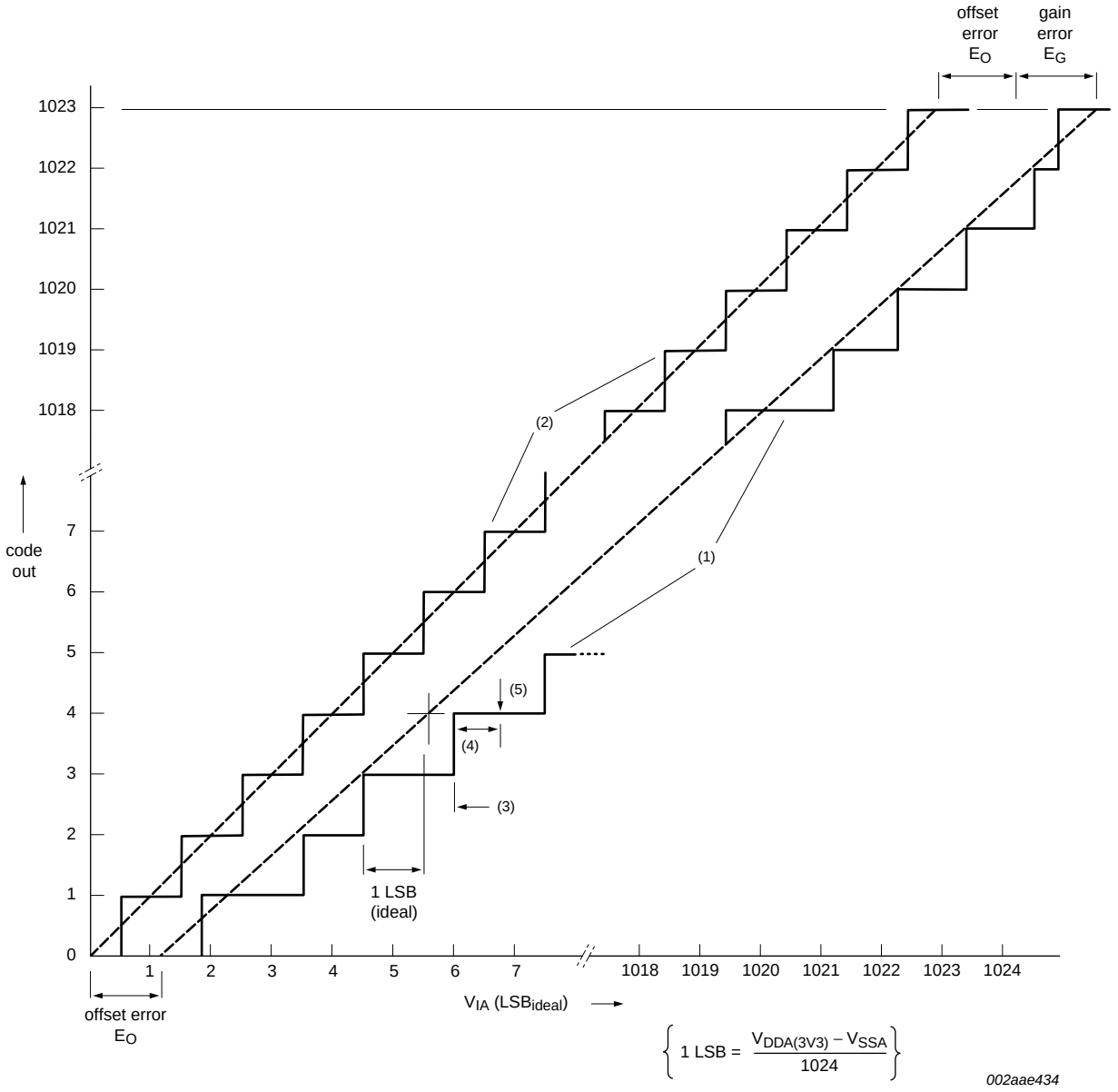
[7] Based on package heat transfer, not device power consumption. Calculated package thermal resistance ($Theta_{JA}$): 35.766 °C/W (with JEDEC Test Board and 0 m/s airflow, ±15 % accuracy).

[8] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[9] Charge device model per AEC-Q100-011.

Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
C_i	input capacitance	Excluding bonding pad capacitance		-	-	1.6	pF
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
		3.3 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
I_{OL}	LOW-level output current	$V_{DD(IO)}$ = 1.8 V; V_{OL} = 0.4 V	[10][14]	3	-	-	mA
		$V_{DD(IO)}$ = 3.3 V; V_{OL} = 0.4 V		3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = $V_{DD(IO)}$; no pull-up/down	[10]	-	-	10	μA
I_{OLS}	LOW-level short-circuit output current	$V_{DD(IO)}$ = 1.8 V; V_{OL} = $V_{DD(IO)}$	[10][15]	-	-	40	mA
		$V_{DD(IO)}$ = 3.3 V; V_{OL} = $V_{DD(IO)}$		-	-	40	mA
ONSW pin							
V_O	output voltage		[10][11][12][13]	0	-	$V_{DD(1V2)}$	V
V_{OH}	HIGH-level output voltage	1.2 V outputs; I_{OH} = −1 mA	[14]	$V_{DD(1V2)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.2 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(1V2)}$ − 0.4 V	[10][14]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[10][14]	3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = $V_{DD(1V2)}$; no pull-up/down	[10]	-	-	1.5	μA
I_{OHS}	HIGH-level short-circuit output current	$V_{DD(1V2)}$ = 1.8 V; V_{OH} = 0 V	[15]	-	-	−135	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = $V_{DD(1V2)}$	[10][15]	-	-	135	mA
Z_o	output impedance	$V_{DD(1V2)}$ = 1.2 V		40	-	60	Ω
Oscillator input/output pins							
$V_{i(xtal)}$	crystal input voltage	on pins RTCX_IN and SYSX_IN		−0.5	-	+1.3	V
$V_{o(xtal)}$	crystal output voltage	on pins RTCX_OUT and SYSX_OUT		−0.5	-	+1.3	V
$\overline{\text{RESET}}$ pin							
V_I	input voltage		[10][12]	0	-	1.95	V
V_{IH}	HIGH-level input voltage	1.2 V inputs		0.7 × $V_{DD(1V2)}$	-	-	V
V_{IL}	LOW-level input voltage	1.2 V inputs		-	-	0.3 × $V_{DD(1V2)}$	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	μA



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 6. ADC characteristics

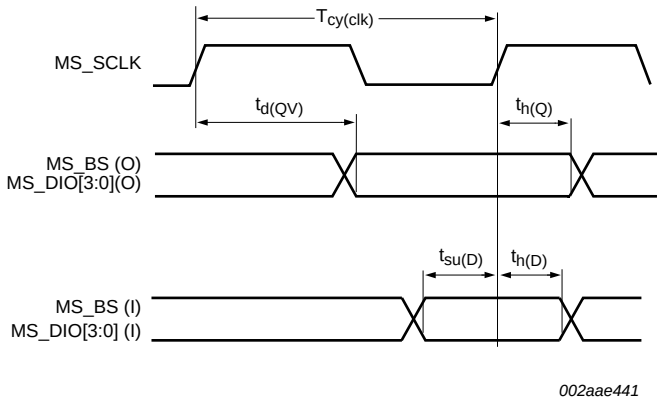


Fig 14. SD card pin interface timing

11.7 MLC NAND flash memory controller

Table 17. Dynamic characteristics of the MLC NAND flash memory controller
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{CELREL}	$\overline{CE}$ LOW to $\overline{RE}$ LOW time	[1][2]	-	$T_{HCLK} \times CEA_D$	-	ns
t_{RC}	$\overline{RE}$ cycle time	[1][5][6]	-	$T_{HCLK} \times (R_L + 1) + T_{HCLK} \times (R_H - R_L)$	-	ns
t_{REH}	$\overline{RE}$ HIGH hold time	[1][5][6]	-	$T_{HCLK} \times (R_H - R_L)$	-	ns
t_{RHZ}	$\overline{RE}$ HIGH to output high-impedance time	[1][5][7]	-	$T_{HCLK} \times (R_H - R_L) + T_{HCLK} \times R_{HZ}$	-	ns
t_{RP}	$\overline{RE}$ pulse width	[1][5]	-	$T_{HCLK} \times (R_L + 1)$	-	ns
t_{REHRBL}	$\overline{RE}$ HIGH to R/$\overline{B}$ LOW time	[1][8]	-	$T_{HCLK} \times B_D$	-	ns
t_{WB}	$\overline{WE}$ HIGH to R/$\overline{B}$ LOW time	[1][8]	-	$T_{HCLK} \times B_D$	-	ns
t_{WC}	$\overline{WE}$ cycle time	[1][3][4]	-	$T_{HCLK} \times (W_L + 1) + T_{HCLK} \times (W_H - W_L)$	-	ns
t_{WH}	$\overline{WE}$ HIGH hold time	[1][3][4]	-	$T_{HCLK} \times (W_H - W_L)$	-	ns
t_{WP}	$\overline{WE}$ pulse width	[1][3]	-	$T_{HCLK} \times (W_L + 1)$	-	ns

[1] T_{HCLK} = 1/HCLK

[2] CEA_D = bit field TCEA_DELAY[1:0] in register MLC_TIME_REG[25:24]

[3] W_L = bit field WR_LOW[3:0] in register MLC_TIME_REG[3:0]

[4] W_H = bit field WR_HIGH[3:0] in register MLC_TIME_REG[7:4]

[5] R_L = bit field RD_LOW[3:0] in register MLC_TIME_REG[11:8]

[6] R_H = bit field RD_HIGH [3:0] in register MLC_TIME_REG[15:12]

[7] R_{HZ} = bit field NAND_TA[2:0] in register MLC_TIME_REG[18:16]

[8] B_D = bit field BUSY_DELAY[4:0] in register MLC_TIME_REG[23:19]

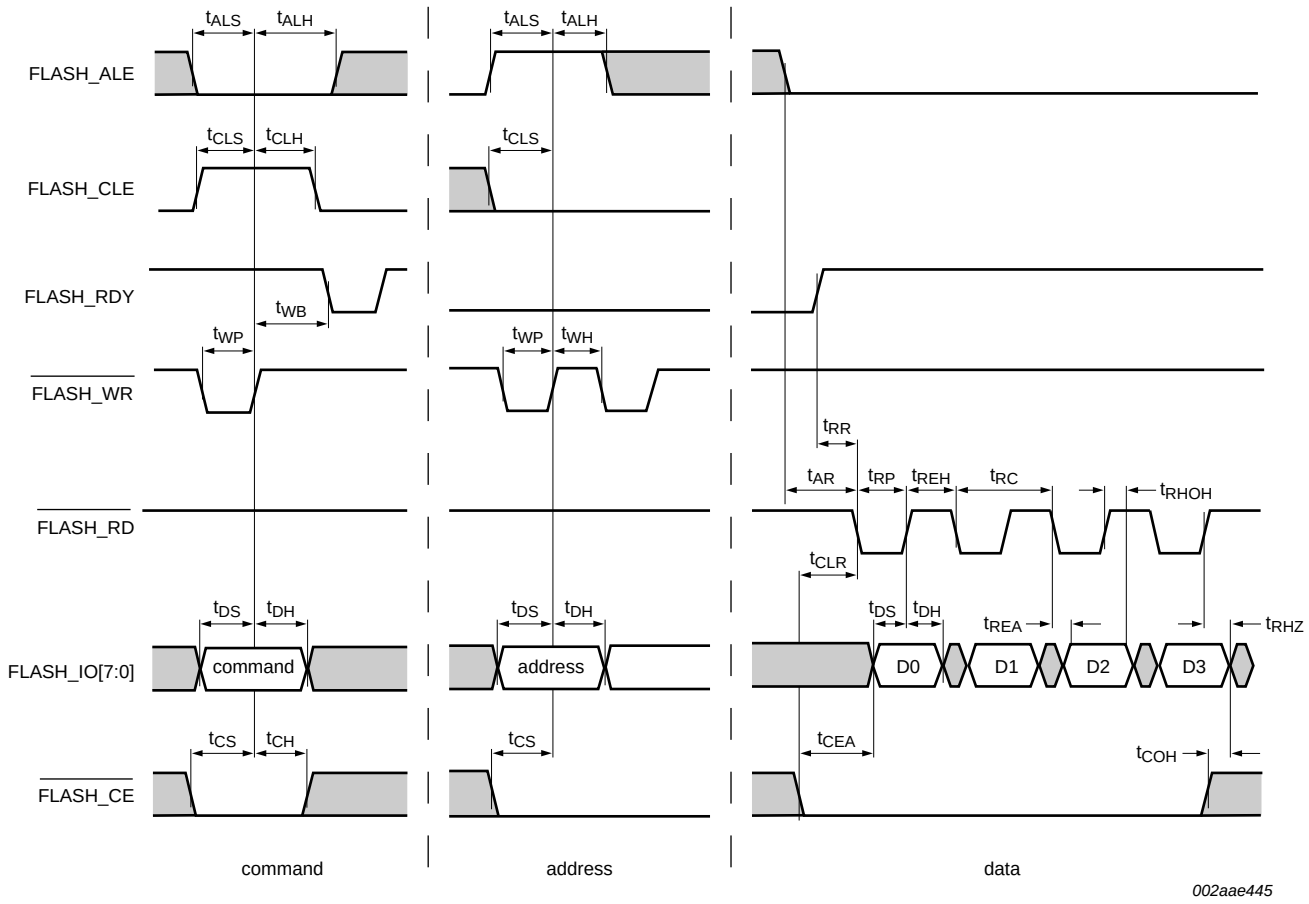


Fig 18. MLC NAND Flash memory read timing (reading from NAND flash)

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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