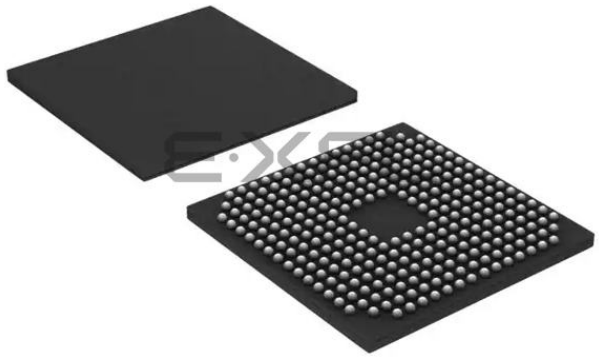

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3230fet296-01-5

4. Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
LPC3220FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3230FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3240FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3250FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1

[1] F = −40 °C to +85 °C temperature range. Note that Revision “A” parts with and without the /01 suffix are identical. For example, LPC3220FET296 Revision “A” is identical to LPC3220FET296/01 Revision “A”.

[2] Available starting with Revision “A”.

4.1 Ordering options

Table 2. Part options

Type number	SRAM (kB)	10/100 Ethernet	LCD controller	Temperature range (°C)	Package
LPC3220FET296/01	128	0	0	−40 to +85	TFBGA296
LPC3230FET296/01	256	0	1	−40 to +85	TFBGA296
LPC3240FET296/01	256	1	0	−40 to +85	TFBGA296
LPC3250FET296/01	256	1	1	−40 to +85	TFBGA296

5. Block diagram

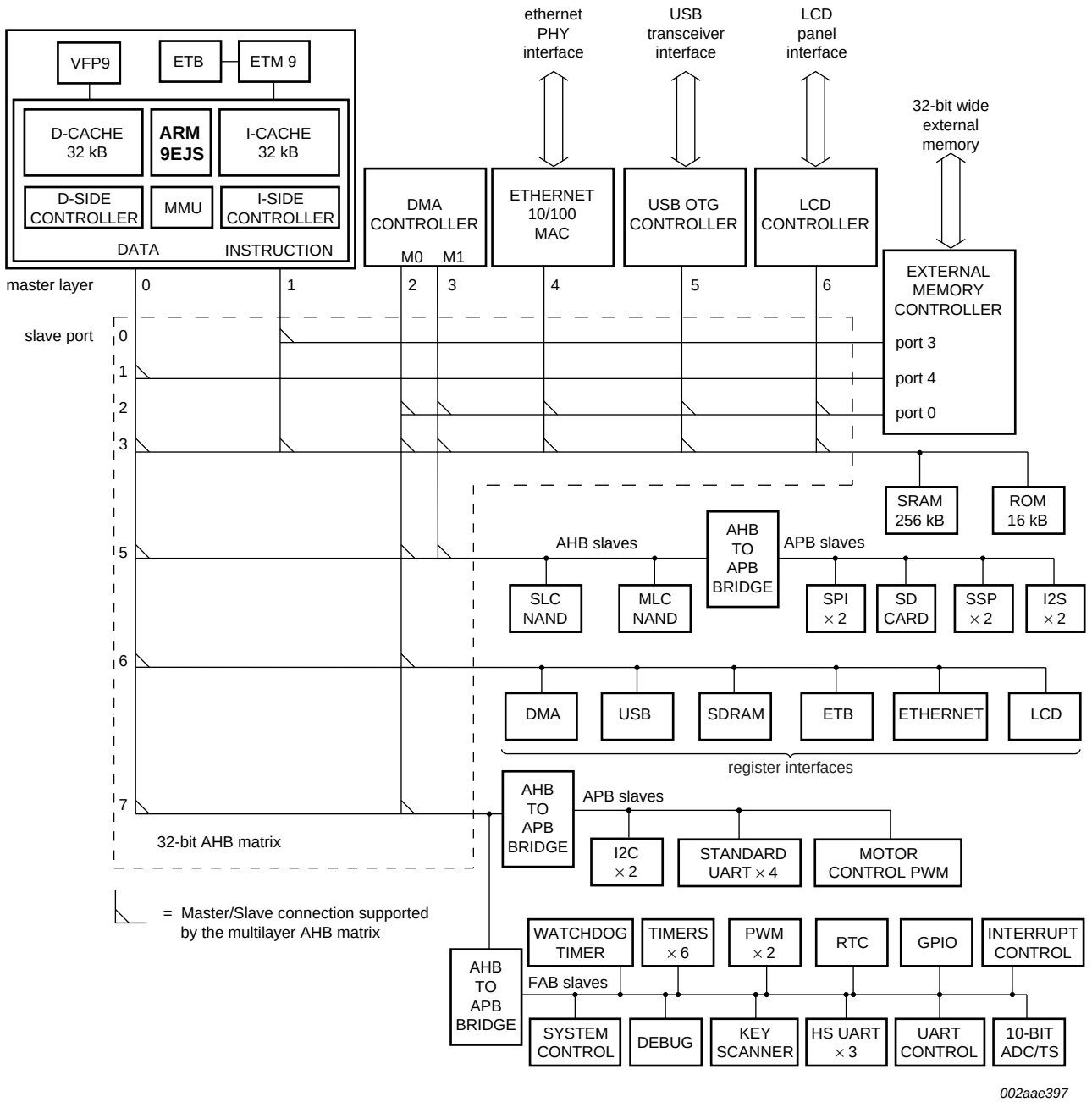


Fig 1. Block diagram of LPC3220/30/40/50

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
C10	SPI1_DATIN/MISO0/GPI_25/ MCI1	C11	GPIO_3/KEY_ROW7/ ENET_MDIO[2]	C12	GPO_9/LCDVD[9][1]
C13	GPO_8/LCDVD[8][1]	C14	GPI_2/CAP2[0]/ ENET_RXD3[2]	C15	GPI_1/$\overline{\text{SERVICE}}$
C16	GPI_0/I2S1RX_SDA	C17	KEY_ROW4/ENET_TXD0[2]	C18	KEY_ROW5/ENET_TXD1[2]
Row D					
D1	FLASH_RDY	D2	FLASH_ALE	D3	GPO_14
D4	GPO_1	D5	USB_DAT_VP/U5_RX	D6	$\overline{\text{USB\_OE\_TP}}$
D7	P0[1]/I2S1RX_WS	D8	GPO_4	D9	GPIO_2/KEY_ROW6/ENET_MDC[2]
D10	GPO_16/MCOB0/LCDENAB[1]/ LCDM[1]	D11	GPO_18/MCOA0/LCDLP[1]	D12	GPO_3/LCDVD[1][1]
D13	GPI_7/CAP4[0]/$\overline{\text{MCABORT}}$	D14	PWM_OUT1/LCDVD[16][1]	D15	PWM_OUT2/INTSTAT/LCDVD[19][1]
D16	KEY_ROW3/ENET_TX_EN[2]	D17	KEY_COL2/ENET_RX_ER[2]	D18	KEY_COL3/ENET_CRS[2]
Row E					
E1	FLASH_IO[3]	E2	FLASH_IO[7]	E3	$\overline{\text{FLASH\_CE}}$
E4	I2C2_SDA	E5	USB_I2C_SCL	E6	USB_I2C_SDA
E7	I2S1TX_SDA/MAT3[1]	E8	GPO_11	E9	GPIO_5/SSEL0/MCI0
E10	GPO_22/U7_HRTS/ LCDVD[14][1]	E11	GPO_10/MCOB2/LCDPWR[1]	E12	GPI_9/KEY_COL7/ENET_COL[2]
E13	GPI_4/SPI1_BUSY	E14	KEY_ROW1/ENET_TXD2[2]	E15	KEY_ROW0/ENET_TX_ER[2]
E16	KEY_COL1/ENET_RX_CLK[2]/ ENET_REF_CLK[2]	E17	U7_RX/CAP0[0]/ LCDVD[10][1]/GPI_23	E18	U7_TX/MAT1[1]/LCDVD[11][1]
Row F					
F1	FLASH_IO[2]	F2	$\overline{\text{FLASH\_WR}}$	F3	FLASH_CLE
F4	GPI_3	F5	VSS_IOC	F6	VSS_IOB
F7	VDD_IOC	F8	VDD_IOB	F9	VDD_IOD
F10	VSS_IOD	F11	VSS_IOD	F12	VSS_IOD
F13	VDD_IOD	F14	KEY_ROW2/ENET_TXD3[2]	F15	KEY_COL0/ENET_TX_CLK[2]
F16	KEY_COL5/ENET_RXD1[2]	F17	U6_IRRX/GPI_21	F18	U5_RX/GPI_20
Row G					
G1	$\overline{\text{EMC\_DYCS1}}$	G2	FLASH_IO[5]	G3	FLASH_IO[6]
G4	$\overline{\text{RESOUT}}$	G5	VSS_IOC	G6	VDD_IOC
G7	VDD_CORE	G8	VSS_CORE	G9	VDD_CORE
G10	VSS_CORE	G11	VDD_CORE	G12	VSS_CORE
G13	U7_HCTS/CAP0[1]/ LCDCLKIN[1]/GPI_22	G14	DBGEN	G15	KEY_COL4/ENET_RXD0[2]
G16	U6_IRTX	G17	SYSCLKEN/LCDVD[15][1]	G18	JTAG_TMS
Row H					
H1	$\overline{\text{EMC\_OE}}$	H2	FLASH_IO[0]	H3	FLASH_IO[1]
H4	FLASH_IO[4]	H5	VSS_IOC	H6	VDD_IOC
H7	VSS_CORE				
				H12	VSS_IOD
H13	VDD_IOA	H14	JTAG_TCK	H15	U5_TX

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
H16	HIGHCORE/LCDVD[17][1]	H17	JTAG_NTRST	H18	JTAG_RTCK
Row J					
J1	EMC_A[20]/P1[20]	J2	EMC_A[21]/P1[21]	J3	EMC_A[22]/P1[22]
J4	EMC_A[23]/P1[23]	J5	VDD_IOC	J6	VDD_EMC
J7	VDD_CORE				
				J12	VDD_CORE
J13	VDD_IOA	J14	U3_RX/GPI_18	J15	JTAG_TDO
J16	JTAG_TDI	J17	U3_TX	J18	U2_HCTS/U3_CTS/GPI_16
Row K					
K1	EMC_A[19]/P1[19]	K2	EMC_A[18]/P1[18]	K3	EMC_A[16]/P1[16]
K4	EMC_A[17]/P1[17]	K5	VSS_EMC	K6	VDD_EMC
K7	VDD_EMC				
				K12	VSS_CORE
K13	VSS_IOA	K14	VDD_RTC	K15	U1_RX/CAP1[0]/GPI_15
K16	U1_TX	K17	U2_TX/U3_DTR	K18	U2_RX/U3_DSR/GPI_17
Row L					
L1	EMC_A[15]/P1[15]	L2	EMC_CKE1	L3	EMC_A[0]/P1[0]
L4	EMC_A[1]/P1[1]	L5	VSS_EMC	L6	VDD_EMC
L7	VSS_CORE				
				L12	VDD_COREFXD
L13	VDD_RTCCORE	L14	VSS_RTCCORE	L15	P0[4]/I2S0RX_WS/LCDVD[6][1]
L16	P0[5]/I2S0TX_SDA/LCDVD[7][1]	L17	P0[6]/I2S0TX_CLK/ LCDVD[12][1]	L18	P0[7]/I2S0TX_WS/LCDVD[13][1]
Row M					
M1	EMC_A[2]/P1[2]	M2	EMC_A[3]/P1[3]	M3	EMC_A[4]/P1[4]
M4	EMC_A[8]/P1[8]	M5	VSS_EMC	M6	VDD_EMC
M7	VDD_CORE	M8	VDD_EMC	M9	VSS_CORE
M10	VSS_CORE	M11	VDD_CORE	M12	VSS_CORE
M13	VDD_COREFXD	M14	$\overline{\text{RESET}}$	M15	ONSW
M16	GPO_23/U2_HRTS/U3_RTS	M17	P0[2]/I2S0RX_SDA/ LCDVD[4][1]	M18	P0[3]/I2S0RX_CLK/LCDVD[5][1]
Row N					
N1	EMC_A[5]/P1[5]	N2	EMC_A[6]/P1[6]	N3	EMC_A[7/P1[7]
N4	EMC_A[12]/P1[12]	N5	VSS_EMC	N6	VSS_EMC
N7	VDD_EMC	N8	VDD_EMC	N9	VDD_EMC
N10	VDD_EMC	N11	VDD_EMC	N12	VDD_AD
N13	VDD_AD	N14	VDD_FUSE	N15	VDD_RTCOSC
N16	GPI_5/U3_DCD	N17	GPI_28/U3_RI	N18	GPO_17
Row P					
P1	EMC_A[9]/P1[9]	P2	EMC_A[10]/P1[10]	P3	EMC_A[11]/P1[11]
P4	EMC_DQM[1]	P5	EMC_DQM[3]	P6	VSS_EMC

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
EMC_DQM[1]	P4	VDD_EMC	O	SDRAM data mask 1 out
EMC_DQM[2]	T1	VDD_EMC	O	SDRAM data mask 2 out
EMC_DQM[3]	P5	VDD_EMC	O	SDRAM data mask 3 out
$\overline{\text{EMC\_DYCS0}}$	R6	VDD_EMC	O	SDRAM active LOW chip select 0
$\overline{\text{EMC\_DYCS1}}$	G1	VDD_EMC	O	SDRAM active LOW chip select 1
$\overline{\text{EMC\_OE}}$	H1	VDD_EMC	O	EMC static memory output enable
$\overline{\text{EMC\_RAS}}$	T2	VDD_EMC	O	SDRAM row address strobe, active LOW
$\overline{\text{EMC\_WR}}$	R4	VDD_EMC	O	EMC write strobe, active LOW
FLASH_ALE	D2	VDD_IOC	O	Flash address latch enable
$\overline{\text{FLASH\_CE}}$	E3	VDD_IOC	O	Flash chip enable
FLASH_CLE	F3	VDD_IOC	O	Flash command latch enable
FLASH_IO[0]	H2	VDD_IOC	I/O: BK	Flash data bus, bit 0
FLASH_IO[1]	H3	VDD_IOC	I/O: BK	Flash data bus, bit 1
FLASH_IO[2]	F1	VDD_IOC	I/O: BK	Flash data bus, bit 2
FLASH_IO[3]	E1	VDD_IOC	I/O: BK	Flash data bus, bit 3
FLASH_IO[4]	H4	VDD_IOC	I/O: BK	Flash data bus, bit 4
FLASH_IO[5]	G2	VDD_IOC	I/O: BK	Flash data bus, bit 5
FLASH_IO[6]	G3	VDD_IOC	I/O: BK	Flash data bus, bit 6
FLASH_IO[7]	E2	VDD_IOC	I/O: BK	Flash data bus, bit 7
$\overline{\text{FLASH\_RD}}$	C1	VDD_IOC	O	Flash read enable
FLASH_RDY	D1	VDD_IOC	I	Flash ready (from flash device)
$\overline{\text{FLASH\_WR}}$	F2	VDD_IOC	O	Flash write enable
GPI_0/I2S1RX_SDA	C16	VDD_IOD	I	General purpose input 0
			I	I^2S1 Receive data
GPI_1/$\overline{\text{SERVICE}}$	C15	VDD_IOD	I	General purpose input 1
			I	Boot select input
GPI_2/CAP2[0]/ ENET_RXD3	C14	VDD_IOD	I	General purpose input 2
			I	Timer 2 capture input 0
			I	Ethernet receive data 3 (LPC3240 and LPC3250 only)
GPI_3	F4	VDD_IOC	I	General purpose input 3
GPI_4/SPI1_BUSY	E13	VDD_IOD	I	General purpose input 4
			I	SPI1 busy input
GPI_5/U3_DCD	N16	VDD_IOA	I	General purpose input 5
			I	UART 3 data carrier detect input
GPI_6/ HSTIM_CAP/ ENET_RXD2	C7	VDD_IOB	I: BK	General purpose input 6
			I: BK	High-speed timer capture input
			I : BK	Ethernet receive data 2 (LPC3240 and LPC3250 only)

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
P0[1]/ I2S1RX_WS	D7	VDD_IOB	I/O	Port 0 GPIO bit 1
			I/O	I^2S1 receive word select
P0[2]/ I2S0RX_SDA/ LCDVD[4]	M17	VDD_IOA	I/O	Port 0 GPIO bit 2
			I/O	I^2S0 receive data
			I/O	LCD data bit 4 (LPC3230 and LPC3250 only)
P0[3]/ I2S0RX_CLK/ LCDVD[5]	M18	VDD_IOA	I/O	Port 0 GPIO bit 3
			I/O	I^2S0 receive clock
			I/O	LCD data bit 5 (LPC3230 and LPC3250 only)
P0[4]/ I2S0RX_WS/ LCDVD[6]	L15	VDD_IOA	I/O	Port 0 GPIO bit 4
			I/O	I^2S0 receive word select
			I/O	LCD data bit 6 (LPC3230 and LPC3250 only)
P0[5]/ I2S0TX_SDA/ LCDVD[7]	L16	VDD_IOA	I/O	Port 0 GPIO bit 5
			I/O	I^2S0 transmit data
			I/O	LCD data bit 7 (LPC3230 and LPC3250 only)
P0[6]/ I2S0TX_CLK/ LCDVD[12]	L17	VDD_IOA	I/O	Port 0 GPIO bit 6
			I/O	I^2S0 transmit clock
			I/O	LCD data bit 12 (LPC3230 and LPC3250 only)
P0[7]/ I2S0TX_WS/ LCDVD[13]	L18	VDD_IOA	I/O	Port 0 GPIO bit 7
			I/O	I^2S0 transmit word select
			I/O	LCD data bit 13 (LPC3230 and LPC3250 only)
PLL397_LOOP	R14	VDD_PLL397	analog filter	PLL397 loop filter (for external components)
PWM_OUT1/ LCDVD[16]	D14	VDD_IOD	O	PWM1 out
			O	LCD data bit 16 (LPC3230 and LPC3250 only)
PWM_OUT2/INTSTAT/ LCDVD[19]	D15	VDD_IOD	O	PWM2 output/internal interrupt status[1]
			O	LCD data bit 19 (LPC3230 and LPC3250 only)
$\overline{\text{RESET}}$	M14	VDD_RTC	I	Reset input, active LOW
$\overline{\text{RESOUT}}$	G4	VDD_IOC	O	Reset out. Reflects external and WDT reset
RTCX_IN	P16	VDD_RTC	analog in	RTC oscillator input
RTCX_OUT	P17	VDD_RTC	analog out	RTC oscillator output
SPI1_CLK/ SCK0	C9	VDD_IOD	O	SPI1 clock out
			O	SSP0 clock out
SPI1_DATIN/ MISO0/ GPI_25/ MCI1	C10	VDD_IOD	I/O	SPI1 data in
			I/O	SSP0 MISO
			I/O	General purpose input bit 25
			I	Motor control channel 1 input
SPI1_DATIO/ MOSI0/ MCI2	B9	VDD_IOD	I/O	SPI1 data out (and optional input)
			I/O	SSP0 MOSI
			I	Motor control channel 2 input

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
SPI2_CLK/ SCK1/ LCDVD[23]	B10	VDD_IOD	I/O	SPI2 clock out
			I/O	SSP1 clock out
			I/O	LCD data bit 23 (LPC3230 and LPC3250 only)
SPI2_DATIO/ MOSI1/ LCDVD[20]	A9	VDD_IOD	I/O	SPI2 data out (and optional input)
			I/O	SSP1 MOSI
			I/O	LCD data bit 20 (LPC3230 and LPC3250 only)
SPI2_DATIN/ MISO1/ LCDVD[21]/ GPI_27	A10	VDD_IOD	I/O	SPI2 data in
			I/O	SSP1 MISO
			I/O	LCD data 21 (LPC3230 and LPC3250 only)
			I/O	General purpose input bit 27
SYSCLKEN/ LCDVD[15]	G17	VDD_IOD	I/O T	Clock request out for external clock source
			I/O T	LCD data bit 15 (LPC3230 and LPC3250 only)
SYSX_IN	T17	VDD_OSC	analog in	System clock oscillator input
SYSX_OUT	R15	VDD_OSC	analog out	System clock oscillator output
TS_XP	R13	VDD_AD	I/O	Touchscreen X output
TS_YP	U16	VDD_AD	I/O	Touchscreen Y output
TST_CLK2	C6	VDD_IOB	O	Test clock 2 out
U1_RX/CAP1[0]/ GPI_15	K15	VDD_IOA	I/O	HS UART 1 receive
			I/O	Timer 1 capture input 0
			I/O	General purpose input bit 15
U1_TX	K16	VDD_IOA	O	HS UART 1 transmit
U2_HCTS/ U3_CTS/GPI_16	J18	VDD_IOA	I/O	HS UART 2 Clear to Send input
			I	UART 3 Clear to Send
			I/O	General purpose input bit 16
U2_RX/ U3_DSR/GPI_17	K18	VDD_IOA	I/O	HS UART 2 receive
			I/O	UART 3 data set ready
			I/O	General purpose input bit 17
U2_TX/U3_DTR	K17	VDD_IOA	O	HS UART 2 transmit
			O	UART 3 data terminal ready out
U3_RX/ GPI_18	J14	VDD_IOD	I/O	UART 3 receive
			I/O	General purpose input bit 18
U3_TX	J17	VDD_IOD	O	UART 3 transmit
U5_RX/ GPI_20	F18	VDD_IOD	I/O	UART 5 receive
			I	General purpose input bit 20
U5_TX	H15	VDD_IOD	O	UART 5 transmit
U6_IRRX/ GPI_21	F17	VDD_IOD	I/O	UART 6 receive (with IrDA)
			I	General purpose input bit 21
U6_IRTX	G16	VDD_IOD	O	UART 6 transmit (with IrDA)

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
VDD_IOC	F7, G6, H6, J5	VDD_IOC	power	1.8 V or 3.3 V supply for IOC domain
VDD_IOD	F13, F9	VDD_IOD	power	1.8 V to 3.3 V supply for IOD domain
VDD_OSC	T18	VDD_OSC	power	1.2 V supply for main oscillator
VDD_PLL397	T16	VDD_PLL397	power	1.2 V supply for 397x PLL
VDD_PLLHCLK	R17	VDD_PLLHCLK	power	1.2 V supply for HCLK PLL
VDD_PLLUSB	P15	VDD_PLLUSB	power	1.2 V supply for USB PLL
VDD_FUSE	N14	VDD_FUSE	power	1.2 V supply
VDD_RTC	K14	VDD_RTC	power	1.2 V supply for RTC I/O
VDD_RTCCORE	L13	VDD_RTCCORE	power	1.2 V supply for RTC
VDD_RTCOSC	N15	VDD_RTCOSC	power	1.2 V supply for RTC oscillator
VSS_AD	P13	-	power	Ground for ADC/touch screen
VSS_CORE	G8, G10, G12, H7, K12, L7, M9, M10, M12	-	power	Ground for core
VSS_EMC	K5, L5, M5, N5, N6, P6, P7, P8, P9, P10, P11	-	power	Ground for EMC
VSS_IOA	K13	-	power	Ground VDD_IOA domain
VSS_IOB	F6	-	power	Ground VDD_IOB domain
VSS_IOC	F5, G5, H5	-	power	Ground VDD_IOC domain
VSS_IOD	F10, F11, F12, H12	-	power	Ground VDD_IOD domain
VSS_OSC	P14	-	power	Ground for main oscillator
VSS_PLL397	T15	-	power	Ground for 397x PLL
VSS_PLLHCLK	R18	-	power	Ground for HCLK PLL

7. Functional description

7.1 CPU and subsystems

7.1.1 CPU

NXP created the LPC3220/30/40/50 using an ARM926EJ-S CPU core that includes a Harvard architecture and a 5-stage pipeline. To this ARM core, NXP implemented a 32 kB instruction cache, a 32 kB data cache and a Vector Floating Point coprocessor. The ARM926EJ-S core also has an integral Memory Management Unit (MMU) to provide the virtual memory capabilities required to support the multi-programming demands of modern operating systems. The basic ARM926EJ-S core V5TE instruction set includes DSP instruction extensions for native Jazelle Java Byte-code execution in hardware. The LPC3220/30/40/50 operates at CPU frequencies up to 266 MHz.

7.1.2 Vector Floating Point (VFP) coprocessor

The LPC3220/30/40/50 includes a VFP co-processor providing full support for single-precision and double-precision add, subtract, multiply, divide, and multiply-accumulate operations at CPU clock speeds. It is compliant with the IEEE 754 standard for binary Floating-Point Arithmetic. This hardware floating point capability makes the microcontroller suitable for advanced motor control and DSP applications. The VFP has 3 separate pipelines for floating-point MAC operations, divide or square root operations, and Load/Store operations. These pipelines operate in parallel and can complete execution out of order. All single-precision instructions execute in one cycle, except the divide and square root instructions. All double-precision multiply and multiply-accumulate instructions take two cycles. The VFP also provides format conversions between floating-point and integer word formats.

7.1.3 Emulation and debugging

The LPC3220/30/40/50 supports emulation and debugging via a dedicated JTAG serial port. An Embedded Trace Buffer allows tracing program execution. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

7.1.3.1 Embedded ICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an Embedded ICE protocol converter. The Embedded ICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel (DCC) function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or entering the debug state.

7.5.1.2 Single-Level Cell (SLC) NAND flash controller

The SLC NAND flash controller interfaces to single-level NAND flash devices. DMA page transfers are supported, including a 20-byte DMA read and write FIFO. Hardware support for ECC (Error Checking and Correction) is included for the main data area. Software can correct a single bit error.

7.5.2 SD card controller

The SD interface allows access to external SD memory cards. The SD card interface conforms to the *SD Memory Card Specification Version 1.01*.

7.5.2.1 Features

- 1-bit and 4-bit data line interface support.
- DMA is supported through the system DMA controller.
- Provides all functions specific to the SD memory card. These include the clock generation unit, power management control, command and data transfer.

7.5.3 External memory controller

The LPC3220/30/40/50 includes a memory controller that supports data bus SDRAM, DDR SDRAM, and static memory devices. The memory controller provides an interface between the system bus and external (off-chip) memory devices.

The controller supports 16-bit and 32-bit wide SDR SDRAM devices of 64 Mbit, 128 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit sizes, as well as 16-bit wide data bus DDR SDRAM devices of 64 Mbit, 128 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit sizes. Two dynamic memory chip selects are supplied, supporting two groups of SDRAM:

- DYCS0 in the address range 0x8000 0000 to 0x9FFF FFFF
- DYCS1 in the address range 0xA000 0000 to 0xBFFF FFFF

The memory controller also supports 8-bit, 16-bit, and 32-bit wide asynchronous static memory devices, including RAM, ROM, and flash, with or without asynchronous page mode. Four static memory chip selects are supplied for SRAM devices:

- CS0 in the address range 0xE000 0000 to 0xE0FF FFFF
- CS1 in the address range 0xE100 0000 to 0xE1FF FFFF
- CS2 in the address range 0xE200 0000 to 0xE2FF FFFF
- CS3 in the address range 0xE300 0000 to 0xE3FF FFFF

The SDRAM controller uses three data ports to allow simultaneous requests from multiple on-chip AHB bus masters and has the following features.

- Dynamic memory interface supports SDRAM, DDR-SDRAM, and low-power variants.
- Read and write buffers to reduce latency and improve performance.
- Static memory features include
  - asynchronous page mode read
  - programmable wait states
  - bus turnaround cycles
  - output enable and write enable delays

- Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices under software control. HNP is partially implemented in hardware.
- Provides programmable timers required for HNP and SRP.
- Supports slave mode operation through AHB slave interface.
- Supports the OTG ATX from NXP (ISP 1302) or any external CEA-2011OTG specification compliant ATX.

7.6.4 LCD controller

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode.

An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.6.4.1 Features

- AHB bus master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 k color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32 bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock or from a clock input pin.

output to be used directly. The maximum PLL output frequency supported by the CPU is 266 MHz. The only output frequency supported by the USB PLL is 48 MHz, and the clock has strict requirements for nominal frequency (500 ppm) and jitter (500 ps).

7.7.4.4 Power control modes

The LPC3220/30/40/50 supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: Run mode, Direct Run mode, and Stop mode.

Run mode is the normal operating mode for applications that require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. In Run mode, the CPU can run at up to 266 MHz and the AHB bus can run at up to 133 MHz.

Direct Run mode allows reducing the CPU and AHB bus rates in order to save power. Direct Run mode can also be the normal operating mode for applications that do not require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. Direct Run mode is the default mode following chip reset.

Stop mode causes all CPU and AHB operation to cease, and stops clocks to peripherals other than the USB block.

7.7.4.5 Reset

Reset is accomplished by an active LOW signal on the $\overline{\text{RESET}}$ input pin. A reset pulse with a minimum width of 10 main oscillator clocks after the oscillator is stable is required to guarantee a valid chip reset. At power-up, 10 milliseconds should be allowed for the oscillator to start up and stabilize after V_{DD} reaches operational voltage. An internal reset with a minimum duration of 10 clock pulses will also be applied if the watchdog timer generates an internal device reset.

The $\overline{\text{RESET}}$ pin is located in the RTC power domain. This means that the RTC power must be present for an external reset to have any effect. The RTC power domain nominally runs from 1.2 V, but the $\overline{\text{RESET}}$ pin can be driven as high as 1.95 V.

7.8 Communication peripheral interfaces

In addition to the Ethernet MAC and USB interfaces there are many more serial communication peripheral interfaces available on the LPC3220/30/40/50. Here is a list of the serial communication interfaces:

- Seven UARTs; four standard UARTs and three high-speed UARTs
- Two SPI serial I/O controllers
- Two SSP serial I/O controllers
- Two I^2C serial I/O controllers
- Two I^2S audio controllers

A short functional description of each of these peripherals is provided in the following sections.

7.8.1 UARTs

The LPC3220/30/40/50 contains seven UARTs. Four are standard UARTs, and three are high-speed UARTs.

7.8.1.1 Standard UARTs

The four standard UARTs are compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16, 32, 48, and 60 Bytes.
- Transmitter FIFO trigger points at 0, 4, 8, and 16 Bytes.
- Register locations conform to the “550” industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

7.8.1.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock for on-board communication in low noise conditions. This is accomplished by changing the over sampling from 16× to 14× and altering the rate generation logic.

Features

- Each high-speed UART has 64-byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1, 4, 8, 16, 32, and 48 B.
- Transmitter FIFO trigger points at 0, 4, and 8 B.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- The three high speed UARTs only support (8N1) 8-bit data word length, 1-stop bit, no parity, and no flow control as a the communications protocol.
- Each UART includes an internal loopback mode.

7.8.2 SPI serial I/O controller

The LPC3220/30/40/50 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

7.9 Other peripherals

In addition to the communication peripherals there are many general purpose peripherals available in the LPC3220/30/40/50. Here is a list of the general purpose peripherals.

- GPI/O
- Keyboard scanner
- Touch screen controller and 10-bit Analog-to-Digital-Converter
- Real-time clock
- High-speed timer
- Four general purpose 32-bit timer/external event counters
- Two simple PWMs
- One motor control PWM

A short functional description of each of these peripherals is provided in the following sections.

7.9.1 General purpose parallel I/O

Some device pins that are not dedicated to a specific peripheral function have been designed to be general purpose inputs, outputs, or input/outputs. Also, some pins may be configured either as a specific peripheral function or a general purpose input, output, or input/output. A total of 51 pins can potentially be used as general purpose input/outputs, 24 as general purpose outputs, and 22 as general purpose inputs.

GPIO pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of GPIO and GPO outputs controlled by that register simultaneously. The value of the output register for standard GPIOs and GPO pins may be read back, as well as the current actual state of the port pins.

In addition to GPIO pins on port 0, port 1, and port 2, there are 22 GPI, 24 GPO, and six GPIO pins. When the SDRAM bus is configured for 16 data bits, 13 of the remaining SDRAM data pins may be used as GPIOs.

7.9.1.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- A single register selects direction for pins that support both input and output modes.
- Direction control of individual bits.
- For input/output pins, both the programmed output state and the actual pin state can be read.
- There are a total of 12 general purpose inputs, 24 general purpose outputs, and six general purpose input/outputs.
- Additionally, 13 SDRAM data lines may be used as GPIOs if a 16-bit SDRAM interface is used (rather than a 32-bit interface).

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Notes	Min	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)		[2]	−0.5	+1.4	V
$V_{DD(EMC)}$	external memory controller supply voltage		[3]	−0.5	+4.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		[4]	−0.5	+4.6	V
$V_{DD(IO)}$	input/output supply voltage		[5]	−0.5	+4.6	V
V_{IA}	analog input voltage			−0.5	+4.6	V
V_I	input voltage	1.8 V pins	[6]	−0.5	+2.4	V
		3.3 V pins	[6]	−0.5	+4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
T_{stg}	storage temperature			−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	max. junction temp 125 °C max. ambient temp 85 °C	[7]	-	1.12	W
V_{ESD}	electrostatic discharge voltage	HBM	[8]	-	2500	V
		CDM	[9]	-	1000	V

[1] The following applies to Table 7:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core, PLL, oscillator, and RTC supplies; applies to pins VDD_CORE, VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, VDD_PLLUSB, VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[3] I/O pad supply; applies to domains VDD_EMC.

[4] Applies to VDD_AD pins.

[5] Applies to pins in the following domains VDD_IOA, VDD_IOB, VDD_IOC, and VDD_IOD.

[6] Including voltage on outputs in 3-state mode.

[7] Based on package heat transfer, not device power consumption. Calculated package thermal resistance ($Theta_{JA}$): 35.766 °C/W (with JEDEC Test Board and 0 m/s airflow, ±15 % accuracy).

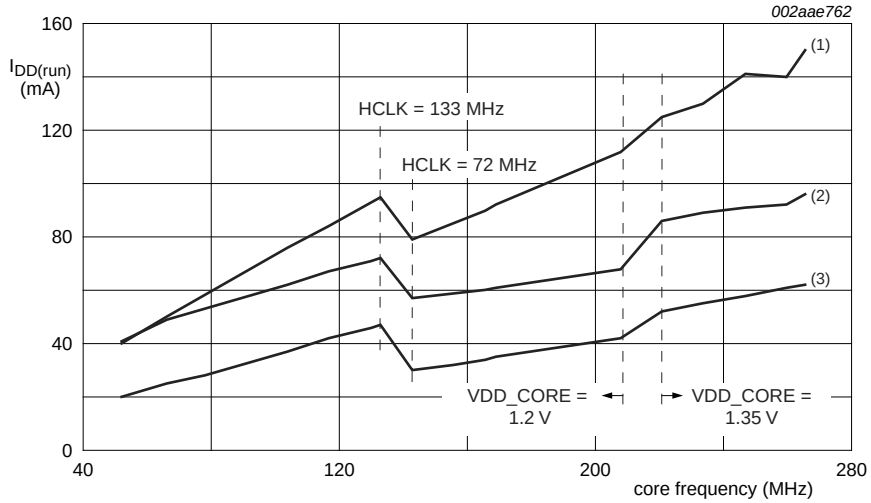
[8] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[9] Charge device model per AEC-Q100-011.

10.4 Power consumption in Run mode

Power consumption is shown in Figure 5 for WinCE applications running under typical conditions from SDRAM. MMU and I-cache/D-cache are enabled. The VFP is turned on but not used. I^2S-interface (channel 1), LCD, SLC NAND controller, I^2C1-bus, SD card, touchscreen ADC, and UART 3 are turned on. All other peripherals are turned off.

The AHB clock HCLK is identical to the core clock for frequencies up to 133 MHz, which is the maximum allowed HCLK frequency. For higher core frequencies, the HCLK PLL output must be divided by 2 to obtain an HCLK frequency lower than or equal to 133 MHz resulting in correspondingly lower power consumption by the AHB peripherals.



Conditions: T_{amb} = 25 °C; VDD_CORE = 1.2 V for core frequencies ≤ 208 MHz; VDD_CORE = 1.35 V for core frequencies > 208 MHz; $V_{DD(IO)}$ = 1.8 V.

(1) WinCE running from SDRAM; playing wmv file at 20 frames/s, 32 kHz mono.

(2) WinCE running from SDRAM; playing mp3 file at 128 kbit/s, stereo.

(3) WinCE running from SDRAM; no application running.

Fig 5. Core current versus core frequency for WinCE applications

Table 12. Dynamic characteristics: static external memory interface *…continued*
C_L = 25 pF, T_{amb} = 20 °C, $V_{DD(EMC)}$ = 1.8 V, 2.5 V, or 3.3 V.

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns

[1] T_{CLCL} = 1/HCLK

[2] Refer to the *LPC32x0 User manual* EMCStaticWaitOen0-3 register for the programming of WAITOEN value.

[3] Refer to the *LPC32x0 User manual* EMCStaticWaitRd0-3 register for the programming of WAITRD value.

[4] Refer to the *LPC32x0 User manual* EMCStaticWaitWen0-3 register for the programming of WAITWEN value.

[5] Refer to the *LPC32x0 User manual* EMCStaticWaitWr0-3 register for the programming of WAITWR value.

[6] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

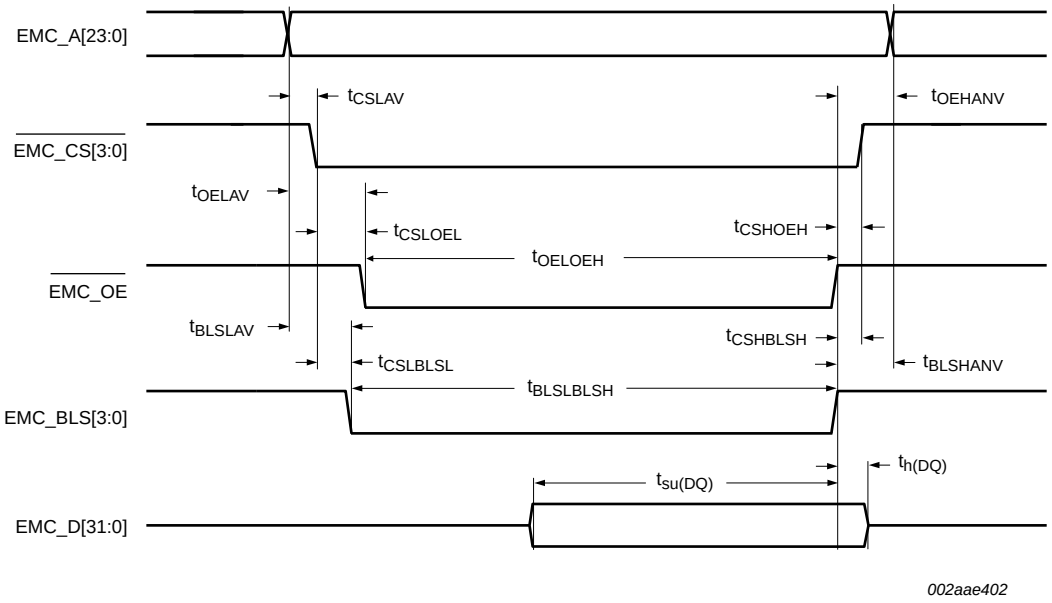


Fig 7. External memory read access

11.5 USB controller

Table 15. Dynamic characteristics USB digital I/O pins

$V_{DD(IO)}$ = 3.3 V; T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TIO}	bus turnaround time (I/O)	OE_N/INT_N to DAT/VP and SE0/VM	-	7	-	ns
t_{TOI}	bus turnaround time (O/I)	OE_N/INT_N to DAT/VP and SE0/VM	-	0	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

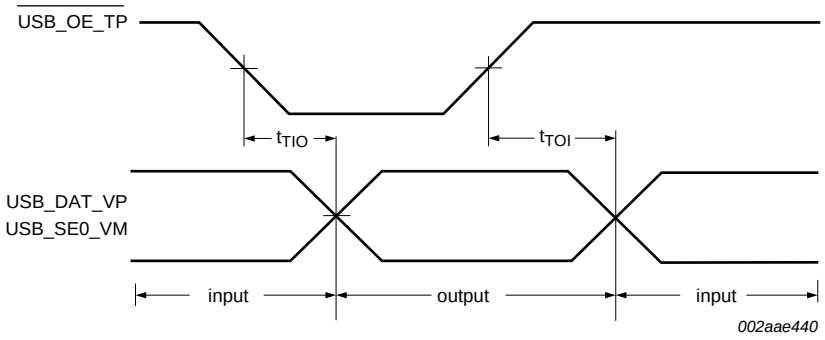


Fig 13. USB bus turnaround time

11.6 Secure Digital (SD) card interface

Table 16. Dynamic characteristics: SD card pin interface

T_{amb} = −40 °C to +85 °C for industrial applications; $V_{DD(IO)}$ over specified ranges.[1]

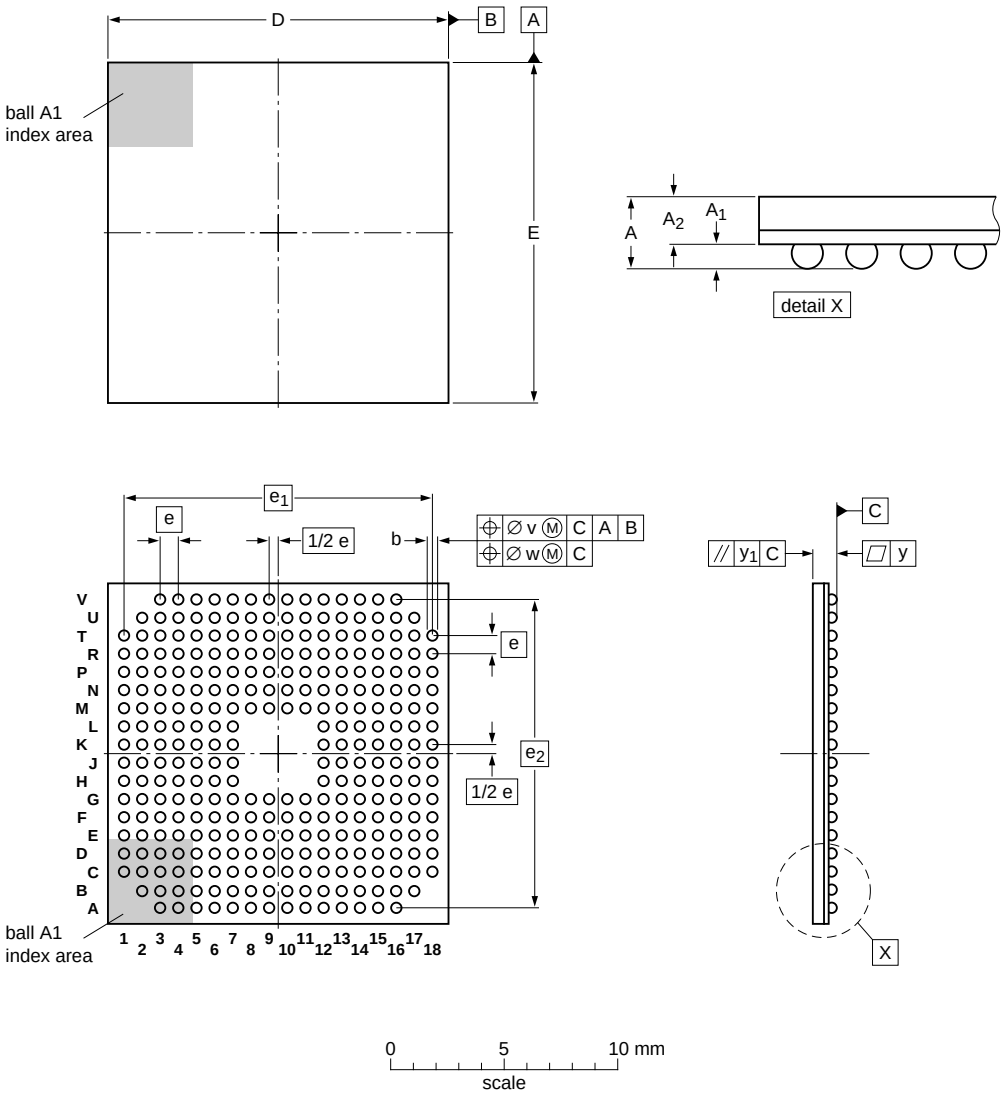
Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$T_{cy(clk)}$	clock cycle time	on pin MS_SCLK; Data transfer mode	-	-	25	MHz
		on pin MS_SCLK; Identification mode	-	-	400	kHz
$t_{su(D)}$	data input set-up time	on pins MS_BS, MS_DIO[3:0] as inputs	-	2.7	-	ns
$t_{h(D)}$	data input hold time	on pins MS_BS, MS_DIO[3:0] as inputs	-	0	-	ns
$t_{d(QV)}$	data output valid delay time	on pins MS_BS, MS_DIO[3:0] as outputs	-	9.7	-	ns
$t_{h(Q)}$	data output hold time	on pins MS_BS, MS_DIO[3:0] as outputs	-	7.7	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

13. Package outline

TFBGA296: plastic thin fine-pitch ball grid array package; 296 balls **SOT1048-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.80 0.65	0.5 0.4	15.1 14.9	15.1 14.9	0.8	13.6	13.6	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1048-1		MO-216				~~07-10-19~~ 07-11-02

Fig 25. Package outline SOT1048-1 (TFBGA296)

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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