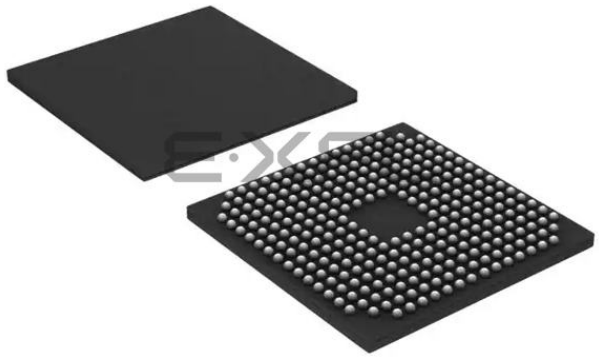

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3230fet296-551

- Multi-layer AHB system that provides a separate bus for each AHB master, including both an instruction and data bus for the CPU, two data busses for the DMA controller, and another bus for the USB controller, one for the LCD, and a final one for the Ethernet MAC. There are no arbitration delays in the system unless two masters attempt to access the same slave at the same time.
- External memory controller for DDR and SDR SDRAM as well as for static devices.
- Two NAND flash controllers: One for single-level NAND flash devices and the other for multi-level NAND flash devices.
- Master Interrupt Controller (MIC) and two Slave Interrupt Controllers (SIC), supporting 74 interrupt sources.
- Eight channel General Purpose DMA (GPDMA) controller on the AHB that can be used with the SD card port, the high-speed UARTs, I^2S-bus interfaces, and SPI interfaces, as well as memory-to-memory transfers.
- Serial interfaces:
  - 10/100 Ethernet MAC with dedicated DMA Controller.
  - USB interface supporting either device, host (OHCI compliant), or On-The-Go (OTG) with an integral DMA controller and dedicated PLL to generate the required 48 MHz USB clock.
  - Four standard UARTs with fractional baud rate generation and 64 byte FIFOs. One of the standard UARTs supports IrDA.
  - Three additional high-speed UARTs intended for on-board communications that support baud rates up to 921 600 when using a 13 MHz main oscillator. All high-speed UARTs provide 64 byte FIFOs.
  - Two SPI controllers.
  - Two SSP controllers.
  - Two I^2C-bus interfaces with standard open-drain pins. The I^2C-bus interfaces support single master, slave, and multi-master I^2C-bus configurations.
  - Two I^2S-bus interfaces, each with separate input and output channels. Each channel can be operated independently on three pins, or both input and output channels can be used with only four pins and a shared clock.
- Additional peripherals:
  - LCD controller supporting both STN and TFT panels, with dedicated DMA controller. Programmable display resolution up to 1024×768.
  - Secure Digital (SD) memory card interface, which conforms to the *SD Memory Card Specification Version 1.01*.
  - General Purpose (GP) input, output, and I/O pins. Includes 12 GP input pins, 24 GP output pins, and 51 GP I/O pins.
  - 10-bit, 400 kHz Analog-to-Digital Converter (ADC) with input multiplexing from three pins. Optionally, the ADC can operate as a touch screen controller.
  - Real-Time Clock (RTC) with separate power pin and dedicated 32 kHz oscillator. NXP implemented the RTC in an independent on-chip power domain so it can remain active while the rest of the chip is not powered. The RTC also includes a 32-byte scratch pad memory.
  - 32-bit general purpose high-speed timer with a 16-bit pre-scaler. This timer includes one external capture input pin and a capture connection to the RTC clock. Interrupts may be generated using three match registers.

4. Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
LPC3220FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3230FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3240FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3250FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1

[1] F = −40 °C to +85 °C temperature range. Note that Revision “A” parts with and without the /01 suffix are identical. For example, LPC3220FET296 Revision “A” is identical to LPC3220FET296/01 Revision “A”.

[2] Available starting with Revision “A”.

4.1 Ordering options

Table 2. Part options

Type number	SRAM (kB)	10/100 Ethernet	LCD controller	Temperature range (°C)	Package
LPC3220FET296/01	128	0	0	−40 to +85	TFBGA296
LPC3230FET296/01	256	0	1	−40 to +85	TFBGA296
LPC3240FET296/01	256	1	0	−40 to +85	TFBGA296
LPC3250FET296/01	256	1	1	−40 to +85	TFBGA296

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
EMC_D[9]	U6	VDD_EMC	I/O: BK	EMC data bit 9
EMC_D[10]	V6	VDD_EMC	I/O: BK	EMC data bit 10
EMC_D[11]	T7	VDD_EMC	I/O: BK	EMC data bit 11
EMC_D[12]	U7	VDD_EMC	I/O: BK	EMC data bit 12
EMC_D[13]	V7	VDD_EMC	I/O: BK	EMC data bit 13
EMC_D[14]	T8	VDD_EMC	I/O: BK	EMC data bit 14
EMC_D[15]	U8	VDD_EMC	I/O: BK	EMC data bit 15
EMC_D[16]/ EMC_DQS0	V8	VDD_EMC	I/O: BK	EMC data bit 16
			I/O: BK	DDR data strobe 0
EMC_D[17]/ EMC_DQS1	R9	VDD_EMC	I/O: BK	EMC data bit 17
			I/O: BK	DDR data strobe 1
EMC_D[18]/ EMC_CLK	V9	VDD_EMC	I/O: P	EMC data bit 18
			I/O: P	DDR inverted clock output
EMC_D[19]/P2[0]	U9	VDD_EMC	I/O: P	EMC data bit 19
			I/O: P	Port 2 GPIO bit 0
EMC_D[20]/P2[1]	T9	VDD_EMC	I/O: P	EMC data bit 20
			I/O: P	Port 2 GPIO bit 1
EMC_D[21]/P2[2]	V10	VDD_EMC	I/O: P	EMC data bit 21
			I/O: P	Port 2 GPIO bit 2
EMC_D[22]/P2[3]	U10	VDD_EMC	I/O: P	EMC data bit 22
			I/O: P	Port 2 GPIO bit 3
EMC_D[23]/P2[4]	T10	VDD_EMC	I/O: P	EMC data bit 23
			I/O: P	Port 2 GPIO bit 4
EMC_D[24]/P2[5]	R10	VDD_EMC	I/O: P	EMC data bit 24
			I/O: P	Port 2 GPIO bit 5
EMC_D[25]/P2[6]	V11	VDD_EMC	I/O: P	EMC data bit 25
			I/O: P	Port 2 GPIO bit 6
EMC_D[26]/P2[7]	U11	VDD_EMC	I/O: P	EMC data bit 26
			I/O: P	Port 2 GPIO bit 7
EMC_D[27]/P2[8]	T11	VDD_EMC	I/O: P	EMC data bit 27
			I/O: P	Port 2 GPIO bit 8
EMC_D[28]/P2[9]	V12	VDD_EMC	I/O: P	EMC data bit 28
			I/O: P	Port 2 GPIO bit 9
EMC_D[29]/P2[10]	V13	VDD_EMC	I/O: P	EMC data bit 29
			I/O: P	Port 2 GPIO bit 10
EMC_D[30]/P2[11]	U12	VDD_EMC	I/O: P	EMC data bit 30
			I/O: P	Port 2 GPIO bit 11
EMC_D[31]/P2[12]	V14	VDD_EMC	I/O: P	EMC data bit 31
			I/O: P	Port 2 GPIO bit 12
EMC_DQM[0]	R3	VDD_EMC	O	SDRAM data mask 0 out

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
GPI_7/CAP4[0]/ $\overline{\text{MCABORT}}$	D13	VDD_IOD	I	General purpose input 7
			I	Timer 4 capture input 0
			I	Motor control PWM LOW-active fast abort input
GPI_8/KEY_COL6/ SPI2_BUSY/ ENET_RX_DV	B16	VDD_IOD	I	General purpose input 8
			I	Keyscan column 6 input
			I	SPI2 busy input
			I	Ethernet receive data valid input (LPC3240 and LPC3250 only)
GPI_9/KEY_COL7/ ENET_COL	E12	VDD_IOD	I	General purpose input 9
			I	Keyscan column 7 input
			I	Ethernet collision input (LPC3240 and LPC3250 only)
GPI_19/U4_RX	B15	VDD_IOD	I	General purpose input 19
			I	UART 4 receive
GPI_28/U3_RI	N17	VDD_IOA	I	General purpose input 28
			I	UART 3 ring indicator input
GPIO_0	A12	VDD_IOD	I/O	General purpose input/output 0
GPIO_1	A11	VDD_IOD	I/O	General purpose input/output 1
GPIO_2/ KEY_ROW6/ ENET_MDC	D9	VDD_IOD	I/O	General purpose input/output 2
			O	Keyscan row 6 output
			O	Ethernet PHY interface clock (LPC3240 and LPC3250 only)
GPIO_3/ KEY_ROW7/ ENET_MDIO	C11	VDD_IOD	I/O	General purpose input/output 3
			I/O	Keyscan row 7 output
			I/O	Ethernet PHY interface data (LPC3240 and LPC3250 only)
GPIO_4/ SSEL1/ LCDVD[22]	B11	VDD_IOD	I/O	General purpose input/output 4
			I/O	SSP1 Slave Select
			I/O	LCD data bit 22 (LPC3230 and LPC3250 only)
GPIO_5/ SSEL0/ MCI0	E9	VDD_IOD	I/O	General purpose input/output 5
			I/O	SSP0 Slave Select
			I/O	Motor control channel 0 input
GPO_0/ TST_CLK1	C3	VDD_IOC	O	General purpose output 0
			O	Test clock 1 out
GPO_1	D4	VDD_IOC	O	General purpose output 1
GPO_2/ MAT1[0]/ LCDVD[0]	B14	VDD_IOD	O	General purpose output 2
			O	Timer 1 match output 0
			O	LCD data bit 0 (LPC3230 and LPC3250 only)
GPO_3/ LCDVD[1]	D12	VDD_IOD	O	General purpose output 3
			O	LCD data bit 1 (LPC3230 and LPC3250 only)
GPO_4	D8	VDD_IOB	O	General purpose output 4

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
KEY_COL4/ ENET_RXD0	G15	VDD_IOD	I	Keyscan column 4 input
			I	Ethernet receive data 0 (LPC3240 and LPC3250 only)
KEY_COL5/ ENET_RXD1	F16	VDD_IOD	I	Keyscan column 5 input
			I	Ethernet receive data 1 (LPC3240 and LPC3250 only)
KEY_ROW0/ ENET_TX_ER	E15	VDD_IOD	I/O T	Keyscan row 0 out
			I/O T	Ethernet transmit error (LPC3240 and LPC3250 only)
KEY_ROW1/ ENET_TXD2	E14	VDD_IOD	I/O T	Keyscan row 1 out
			I/O T	Ethernet transmit data 2 (LPC3240 and LPC3250 only)
KEY_ROW2/ ENET_TXD3	F14	VDD_IOD	I/O T	Keyscan row 2 out
			I/O T	Ethernet transmit data 3 (LPC3240 and LPC3250 only)
KEY_ROW3/ ENET_TX_EN	D16	VDD_IOD	I/O T	Keyscan row 3 out
			I/O T	Ethernet transmit enable (LPC3240 and LPC3250 only)
KEY_ROW4/ ENET_TXD0	C17	VDD_IOD	I/O T	Keyscan row 4 out
			I/O T	Ethernet transmit data 0 (LPC3240 and LPC3250 only)
KEY_ROW5/ ENET_TXD1	C18	VDD_IOD	I/O T	Keyscan row 5 out
			I/O T	Ethernet transmit data 1 (LPC3240 and LPC3250 only)
MS_BS/MAT2[1]	A6	VDD_IOD	I/O: P	MS/SD card command out
			O	Timer 2 match output 1
MS_DIO0/MAT0[0]	A8	VDD_IOD	I/O: P	MS/SD card data 0
			O	Timer 0 match output 0
MS_DIO1/ MAT0[1]	A7	VDD_IOD	I/O: P	MS/SD card data 1
			O	Timer 0 match output 1
MS_DIO2/ MAT0[2]	B8	VDD_IOD	I/O: P	MS/SD card data 2
			O	Timer 0 match output 2
MS_DIO3/ MAT0[3]	C8	VDD_IOD	I/O: P	MS/SD card data 3
			O	Timer 0 match output 3
MS_SCLK/ MAT2[0]	B7	VDD_IOD	I/O	MS/SD card clock output
			O	Timer 2 match output 0
n.c.	B17, U17, U2	-	-	not connected
ONSW	M15	VDD_RTC	O	RTC match output for external power control
P0[0]/ I2S1RX_CLK	B5	VDD_IOB	I/O	Port 0 GPIO bit 0
			I/O	I^2S1 receive clock

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
P0[1]/ I2S1RX_WS	D7	VDD_IOB	I/O	Port 0 GPIO bit 1
			I/O	I^2S1 receive word select
P0[2]/ I2S0RX_SDA/ LCDVD[4]	M17	VDD_IOA	I/O	Port 0 GPIO bit 2
			I/O	I^2S0 receive data
			I/O	LCD data bit 4 (LPC3230 and LPC3250 only)
P0[3]/ I2S0RX_CLK/ LCDVD[5]	M18	VDD_IOA	I/O	Port 0 GPIO bit 3
			I/O	I^2S0 receive clock
			I/O	LCD data bit 5 (LPC3230 and LPC3250 only)
P0[4]/ I2S0RX_WS/ LCDVD[6]	L15	VDD_IOA	I/O	Port 0 GPIO bit 4
			I/O	I^2S0 receive word select
			I/O	LCD data bit 6 (LPC3230 and LPC3250 only)
P0[5]/ I2S0TX_SDA/ LCDVD[7]	L16	VDD_IOA	I/O	Port 0 GPIO bit 5
			I/O	I^2S0 transmit data
			I/O	LCD data bit 7 (LPC3230 and LPC3250 only)
P0[6]/ I2S0TX_CLK/ LCDVD[12]	L17	VDD_IOA	I/O	Port 0 GPIO bit 6
			I/O	I^2S0 transmit clock
			I/O	LCD data bit 12 (LPC3230 and LPC3250 only)
P0[7]/ I2S0TX_WS/ LCDVD[13]	L18	VDD_IOA	I/O	Port 0 GPIO bit 7
			I/O	I^2S0 transmit word select
			I/O	LCD data bit 13 (LPC3230 and LPC3250 only)
PLL397_LOOP	R14	VDD_PLL397	analog filter	PLL397 loop filter (for external components)
PWM_OUT1/ LCDVD[16]	D14	VDD_IOD	O	PWM1 out
			O	LCD data bit 16 (LPC3230 and LPC3250 only)
PWM_OUT2/INTSTAT/ LCDVD[19]	D15	VDD_IOD	O	PWM2 output/internal interrupt status[1]
			O	LCD data bit 19 (LPC3230 and LPC3250 only)
$\overline{\text{RESET}}$	M14	VDD_RTC	I	Reset input, active LOW
$\overline{\text{RESOUT}}$	G4	VDD_IOC	O	Reset out. Reflects external and WDT reset
RTCX_IN	P16	VDD_RTC	analog in	RTC oscillator input
RTCX_OUT	P17	VDD_RTC	analog out	RTC oscillator output
SPI1_CLK/ SCK0	C9	VDD_IOD	O	SPI1 clock out
			O	SSP0 clock out
SPI1_DATIN/ MISO0/ GPI_25/ MCI1	C10	VDD_IOD	I/O	SPI1 data in
			I/O	SSP0 MISO
			I/O	General purpose input bit 25
			I	Motor control channel 1 input
SPI1_DATIO/ MOSI0/ MCI2	B9	VDD_IOD	I/O	SPI1 data out (and optional input)
			I/O	SSP0 MOSI
			I	Motor control channel 2 input

7.1.3.2 Embedded trace buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer (ETB) of 2048 × 24 bits captures the trace information under software debugger control. Data from the ETB is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

7.2 AHB matrix

The LPC3220/30/40/50 has a multi-layer AHB matrix for inter-block communication. AHB is an ARM defined high-speed bus, which is part of the ARM bus architecture. AHB is a high-bandwidth low-latency bus that supports multi-master arbitration and a bus grant/request mechanism. For systems that have only one (CPU), or two (CPU and DMA) bus masters a simple AHB works well. However, if a system requires multiple bus masters and the CPU needs access to external memory, a single AHB bus can cause a bottleneck.

To increase performance, the LPC3220/30/40/50 uses an expanded AHB architecture known as Multi-layer AHB. A Multi-layer AHB replaces the request/grant and arbitration mechanism used in a simple AHB with an interconnect matrix that moves arbitration out toward the slave devices. Thus, if a CPU and a DMA controller want access to the same memory, the interconnect matrix arbitrates between the two when granting access to the memory. This advanced architecture allows simultaneous access by bus masters to different resources with an increase in arbitration complexity. In this architectural implementation, removing guaranteed central arbitration and allowing more than one bus master to be active at the same time provides better overall microcontroller performance.

In the LPC3220/30/40/50, the multi-Layer AHB system has a separate bus for each of seven AHB Masters:

- CPU data bus
- CPU instruction bus
- General purpose DMA Master 0
- General purpose DMA Master 1
- Ethernet controller
- USB controller
- LCD controller

There are no arbitration delays unless two masters attempt to access the same slave at the same time.

  - extended wait
- Power-saving modes dynamically control EMC_CKE[1:0] and EMC_CLK.
- Dynamic memory self-refresh mode supported by software.
- Controller supports 2 k, 4 k, and 8 k row address synchronous memory parts. That is, typical 512 MB, 256 MB, 128 MB, and 16 MB parts, with 8, 16, or 32 data bits per device.
- Two reset domains enable dynamic memory contents to be preserved over a soft reset.
- This controller does not support synchronous static memory devices (burst mode devices).

7.6 AHB master peripherals

The LPC3220/30/40/50 implements four AHB master peripherals, which include a General Purpose Direct Memory Access (GPDMA) controller, a 10/100 Ethernet Media Access Controller (MAC), a Universal Serial Bus (USB) controller, and an LCD controller. Each of these four peripherals contain an integral DMA controller optimized to support the performance demands of the peripheral.

7.6.1 General Purpose DMA (GPDMA) controller

The GPDMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the same AHB master, or one area by each master. The DMA controller supports the following peripheral device transfers.

- Secure Digital (SD) Memory interface
- High-speed UARTs
- I^2S0 and I^2S1 ports
- SPI1 and SPI2 interfaces
- SSP0 and SSP1 interfaces
- Memory

The DMA controls eight DMA channels with hardware prioritization. The DMA controller interfaces to the system via two AHB bus masters, each with a full 32-bit data bus width. DMA operations may be set up for 8-bit, 16-bit, and 32-bit data widths, and can be either big-endian or little-endian. Incrementing or non-incrementing addressing for source and destination are supported, as well as programmable DMA burst size. Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.

7.6.2 Ethernet MAC

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive

- Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices under software control. HNP is partially implemented in hardware.
- Provides programmable timers required for HNP and SRP.
- Supports slave mode operation through AHB slave interface.
- Supports the OTG ATX from NXP (ISP 1302) or any external CEA-2011OTG specification compliant ATX.

7.6.4 LCD controller

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode.

An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.6.4.1 Features

- AHB bus master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 k color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32 bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock or from a clock input pin.

7.8.1 UARTs

The LPC3220/30/40/50 contains seven UARTs. Four are standard UARTs, and three are high-speed UARTs.

7.8.1.1 Standard UARTs

The four standard UARTs are compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16, 32, 48, and 60 Bytes.
- Transmitter FIFO trigger points at 0, 4, 8, and 16 Bytes.
- Register locations conform to the “550” industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

7.8.1.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock for on-board communication in low noise conditions. This is accomplished by changing the over sampling from 16× to 14× and altering the rate generation logic.

Features

- Each high-speed UART has 64-byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1, 4, 8, 16, 32, and 48 B.
- Transmitter FIFO trigger points at 0, 4, and 8 B.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- The three high speed UARTs only support (8N1) 8-bit data word length, 1-stop bit, no parity, and no flow control as a the communications protocol.
- Each UART includes an internal loopback mode.

7.8.2 SPI serial I/O controller

The LPC3220/30/40/50 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master. The SPI implementation on the LPC3220/30/40/50 does not support operation as a slave.

7.8.2.1 Features

- Supports slaves compatible with SPI modes 0 to 3.
- Half duplex synchronous transfers.
- DMA support for data transmit and receive.
- 1-bit to 16-bit word length.
- Choice of LSB or MSB first data transmission.
- 64 × 16-bit input or output FIFO.
- Bit rates up to 52 Mbit/s.
- Busy input function.
- DMA time out interrupt to allow detection of end of reception when using DMA.
- Timed interrupt to facilitate emptying the FIFO at the end of a transmission.
- SPI clock and data pins may be used as general purpose pins if the SPI is not used.
- Slave selects can be supported using GPO or GPIO pins

7.8.3 SSP serial I/O controller

The LPC3220/30/40/50 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.8.3.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of $\frac{1}{2}$ (Master mode) and $\frac{1}{2}$ (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.8.4 I^2C-bus serial I/O controller

There are two I^2C-bus interfaces in the LPC32x0 family of controllers. These I^2C blocks can be configured as a master, multi-master or slave supporting up to 400 kHz. The I^2C blocks also support 7 or 10 bit addressing. Each has a four word FIFO for both transmit and receive. An interrupt signal is available from each block.

7.9 Other peripherals

In addition to the communication peripherals there are many general purpose peripherals available in the LPC3220/30/40/50. Here is a list of the general purpose peripherals.

- GPI/O
- Keyboard scanner
- Touch screen controller and 10-bit Analog-to-Digital-Converter
- Real-time clock
- High-speed timer
- Four general purpose 32-bit timer/external event counters
- Two simple PWMs
- One motor control PWM

A short functional description of each of these peripherals is provided in the following sections.

7.9.1 General purpose parallel I/O

Some device pins that are not dedicated to a specific peripheral function have been designed to be general purpose inputs, outputs, or input/outputs. Also, some pins may be configured either as a specific peripheral function or a general purpose input, output, or input/output. A total of 51 pins can potentially be used as general purpose input/outputs, 24 as general purpose outputs, and 22 as general purpose inputs.

GPIO pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of GPIO and GPO outputs controlled by that register simultaneously. The value of the output register for standard GPIOs and GPO pins may be read back, as well as the current actual state of the port pins.

In addition to GPIO pins on port 0, port 1, and port 2, there are 22 GPI, 24 GPO, and six GPIO pins. When the SDRAM bus is configured for 16 data bits, 13 of the remaining SDRAM data pins may be used as GPIOs.

7.9.1.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- A single register selects direction for pins that support both input and output modes.
- Direction control of individual bits.
- For input/output pins, both the programmed output state and the actual pin state can be read.
- There are a total of 12 general purpose inputs, 24 general purpose outputs, and six general purpose input/outputs.
- Additionally, 13 SDRAM data lines may be used as GPIOs if a 16-bit SDRAM interface is used (rather than a 32-bit interface).

Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; no pull-down	[10]	-	-	1	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[10]	-	-	1	μA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[10]	-	-	100	mA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Applies to VDD_CORE pins.

[3] Applies to pins VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[4] Applies to pins VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, and VDD_PLLUSB.

[5] Applies when using 1.8 V Mobile DDR or Mobile SDR SDRAM.

[6] Applies when using 2.5 V DDR memory.

[7] Applies when using 3.3 V SDR SDRAM and SRAM.

[8] Specifies current on combined VDD_RTCx during normal chip operation: VDD_RTC, VDD_CORE, VDD_OSC = 1.2 V and VDD_CORE, VDD_IOx at typical voltage.

[9] Specifies current on combined VDD_RTCx during backup operation: VDD_RTC, VDD_CORE, VDD_OSC = 1.2 V and all other VDD_x at 0 V.

[10] Referenced to the applicable V_{DD} for the pin.

[11] Including voltage on outputs in 3-state mode.

[12] The applicable V_{DD} voltage for the pin must be present.

[13] 3-state outputs go into 3-state mode when the applicable V_{DD} voltage for the pin is grounded.

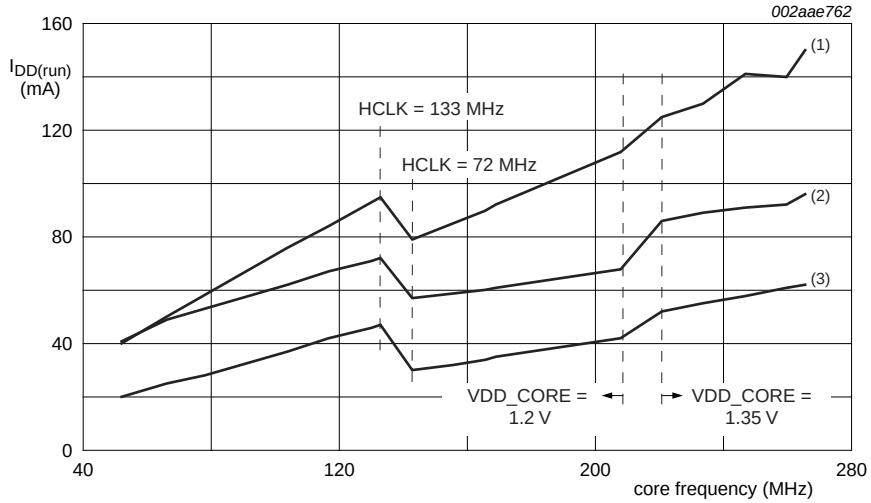
[14] Accounts for 100 mV voltage drop in all supply lines.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

10.4 Power consumption in Run mode

Power consumption is shown in Figure 5 for WinCE applications running under typical conditions from SDRAM. MMU and I-cache/D-cache are enabled. The VFP is turned on but not used. I^2S-interface (channel 1), LCD, SLC NAND controller, I^2C1-bus, SD card, touchscreen ADC, and UART 3 are turned on. All other peripherals are turned off.

The AHB clock HCLK is identical to the core clock for frequencies up to 133 MHz, which is the maximum allowed HCLK frequency. For higher core frequencies, the HCLK PLL output must be divided by 2 to obtain an HCLK frequency lower than or equal to 133 MHz resulting in correspondingly lower power consumption by the AHB peripherals.



Conditions: T_{amb} = 25 °C; VDD_CORE = 1.2 V for core frequencies ≤ 208 MHz; VDD_CORE = 1.35 V for core frequencies > 208 MHz; $V_{DD(IO)}$ = 1.8 V.

(1) WinCE running from SDRAM; playing wmv file at 20 frames/s, 32 kHz mono.

(2) WinCE running from SDRAM; playing mp3 file at 128 kbit/s, stereo.

(3) WinCE running from SDRAM; no application running.

Fig 5. Core current versus core frequency for WinCE applications

Table 12. Dynamic characteristics: static external memory interface *…continued*
C_L = 25 pF, T_{amb} = 20 °C, $V_{DD(EMC)}$ = 1.8 V, 2.5 V, or 3.3 V.

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns

[1] T_{CLCL} = 1/HCLK

[2] Refer to the *LPC32x0 User manual* EMCStaticWaitOen0-3 register for the programming of WAITOEN value.

[3] Refer to the *LPC32x0 User manual* EMCStaticWaitRd0-3 register for the programming of WAITRD value.

[4] Refer to the *LPC32x0 User manual* EMCStaticWaitWen0-3 register for the programming of WAITWEN value.

[5] Refer to the *LPC32x0 User manual* EMCStaticWaitWr0-3 register for the programming of WAITWR value.

[6] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

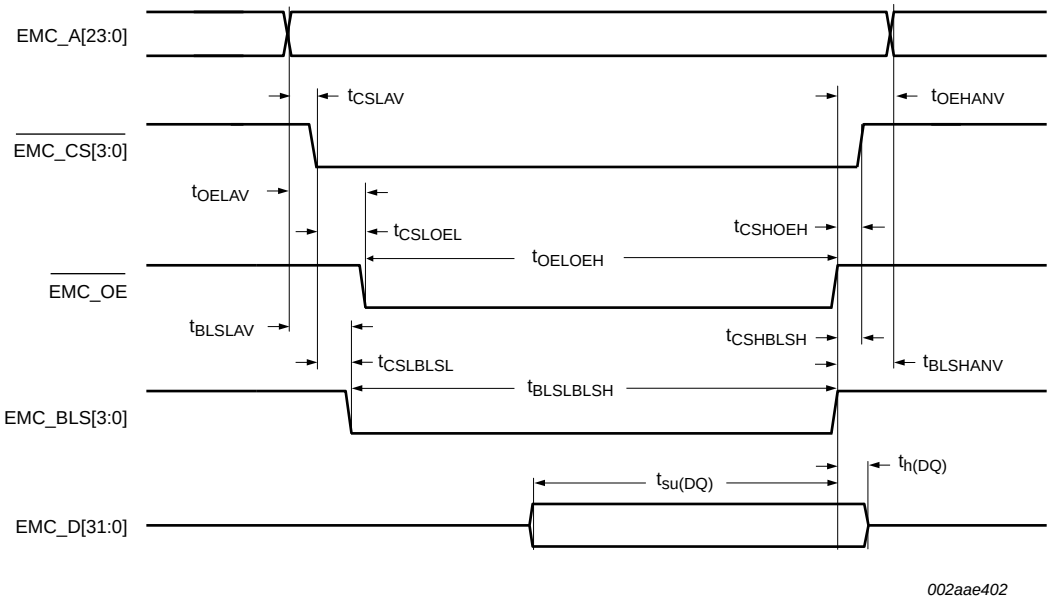


Fig 7. External memory read access

11.4 DDR SDRAM controller

Table 14. EMC DDR SDRAM memory interface dynamic characteristics[1]

C_L = 25 pF, T_{amb} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typical	Max	Unit
f_{oper}	operating frequency			-	104	133	MHz
t_{CK}	clock cycle time			7.5	9.6	-	ns
t_{CL}	CK LOW-level width			-	$0.5 \times t_{CK}$	-	ns
t_{CH}	CK HIGH-level width			-	$0.5 \times t_{CK}$	-	ns
$t_{d(V)ctrl}$	control valid delay time		[2][3]	-	(CMD_DLY × 0.25) + 1.5	-	ns
$t_{h(ctrl)}$	control hold time		[2][3]	-	(CMD_DLY × 0.25) − 1.5	-	ns
$t_{d(AV)}$	address valid delay time		[2]	-	(CMD_DLY × 0.25) + 1.5	-	ns
$t_{h(A)}$	address hold time		[2]	-	(CMD_DLY × 0.25) − 1.5	-	ns
$t_{su(Q)}$	data output set-up time	EMC_D[31:0] and EMC_DQM[3:0] to EMC_DQS[1:0] out	[5]	$0.08 \times t_{CK}$	$0.15 \times t_{CK}$	$0.25 \times t_{CK}$	ns
$t_{h(Q)}$	data output hold time	EMC_D[31:0] and EMC_DQM[3:0] to EMC_DQS[1:0] out	[5]	$0.25 \times t_{CK}$	$0.35 \times t_{CK}$	$0.42 \times t_{CK}$	ns
t_{DQSH}	DQS HIGH time	for WRITE command		-	$0.5 \times t_{CK}$	-	ns
t_{DQSL}	DQS LOW time	for WRITE command		-	$0.5 \times t_{CK}$	-	ns
t_{DQSS}	WRITE command to first DQS latching transition time	for DQS out		-	t_{CK} + 0.7	-	ns
t_{DSS}	DQS falling edge to CK set-up time	for DQS in		-	$0.5 \times t_{CK}$	-	ns
t_{DSH}	DQS falling edge hold time from CK	for DQS in		-	$0.5 \times t_{CK}$	-	ns
$t_{d(DQS)}$	DQS delay time	for DQS in	[4]	-	DQS_DELAY	-	ns
$t_{su(D)}$	data input set-up time			-	0.3	-	ns
$t_{h(D)}$	data input hold time			-	0.5	-	ns

[1] All values valid for EMC pads set to fast slew rate at 1.8 V unless otherwise specified (see SDRAMCLK_CTRL register in the *LPC32x0 User manual*).

[2] CMD_DLY = COMMAND_DELAY bit field in SDRAMCLK_CTRL[18:14] register, see *External Memory Controller (EMC) chapter in LPC32x0 User manual*.

[3] Applies to signals EMC_DQM[3:0], $\overline{\text{EMC\_DYCS}}$[1:0], $\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_WR}}$, EMC_CKE[1:0].

[4] DQS_DELAY, see *LPC32x0 User manual, External Memory Controller Chapter, Section 8 DDR DQS delay calibration* for details on configuring this value.

[5] Test conditions for measurements: T_{amb} = −40 °C to +85 °C; operating frequency range f_{oper} = 52 MHz to 133 MHz; EMC_DQM[3:0] and EMC_D[31:0] driving 2 inches of 50 Ω characteristic impedance trace with 10 pF capacitive load; no external source series termination resistors used. EMC pads set to fast slew rate at 1.8 V or 2.5 V (see SDRAMCLK_CTRL register in the *LPC32x0 User manual*).

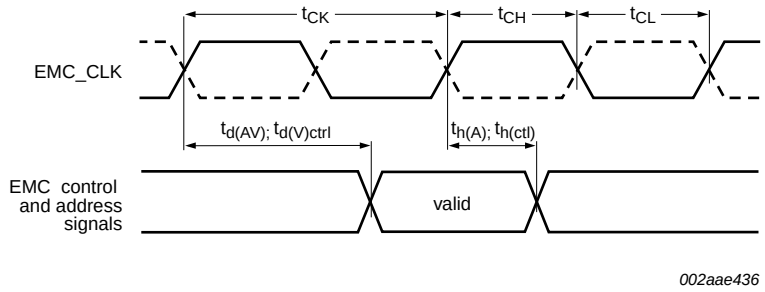


Fig 10. DDR control timing parameters

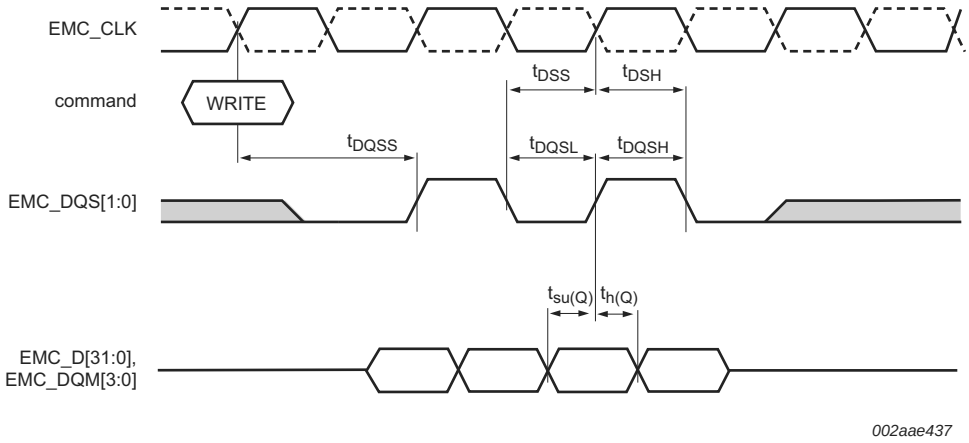
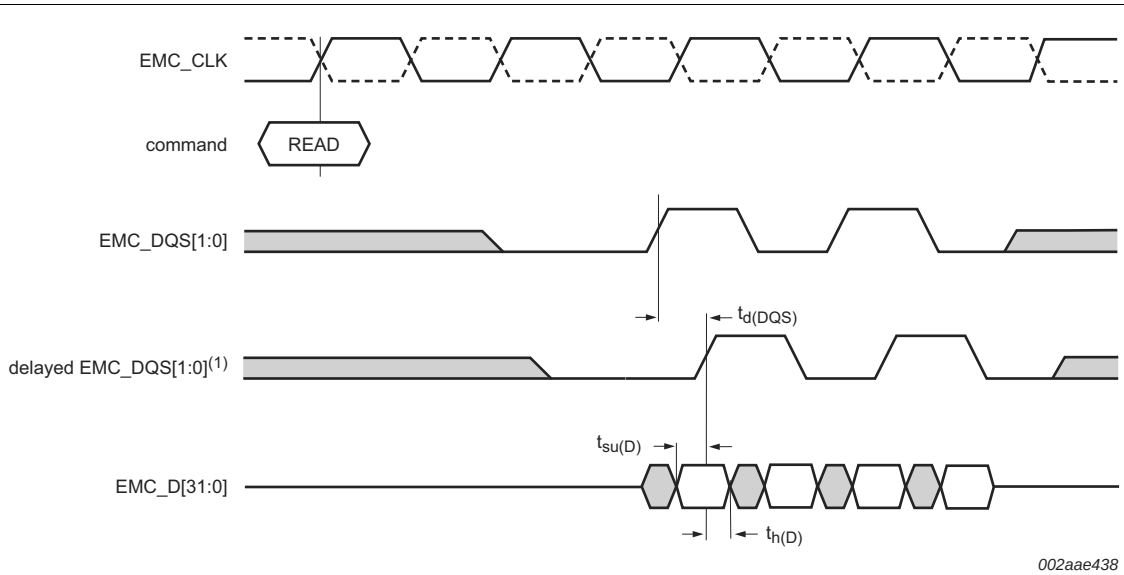


Fig 11. DDR write timing parameters



(1) The delay of the EMC_DQS[1:0] signal is determined by the DQS_DELAY settings. See *LPC32x0 User manual, External Memory Controller Chapter, section DDR DQS delay calibration* for details on configuring this value.

Fig 12. DDR read timing parameters

11.5 USB controller

Table 15. Dynamic characteristics USB digital I/O pins

$V_{DD(IO)}$ = 3.3 V; T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TIO}	bus turnaround time (I/O)	OE_N/INT_N to DAT/VP and SE0/VM	-	7	-	ns
t_{TOI}	bus turnaround time (O/I)	OE_N/INT_N to DAT/VP and SE0/VM	-	0	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

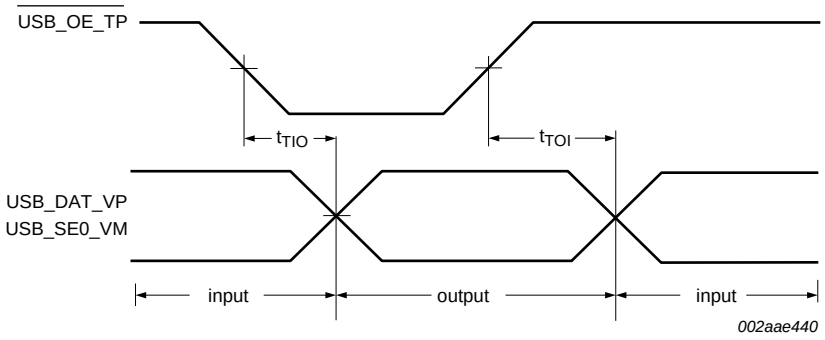


Fig 13. USB bus turnaround time

11.6 Secure Digital (SD) card interface

Table 16. Dynamic characteristics: SD card pin interface

T_{amb} = −40 °C to +85 °C for industrial applications; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$T_{cy(clk)}$	clock cycle time	on pin MS_SCLK; Data transfer mode	-	-	25	MHz
		on pin MS_SCLK; Identification mode	-	-	400	kHz
$t_{su(D)}$	data input set-up time	on pins MS_BS, MS_DIO[3:0] as inputs	-	2.7	-	ns
$t_{h(D)}$	data input hold time	on pins MS_BS, MS_DIO[3:0] as inputs	-	0	-	ns
$t_{d(QV)}$	data output valid delay time	on pins MS_BS, MS_DIO[3:0] as outputs	-	9.7	-	ns
$t_{h(Q)}$	data output hold time	on pins MS_BS, MS_DIO[3:0] as outputs	-	7.7	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

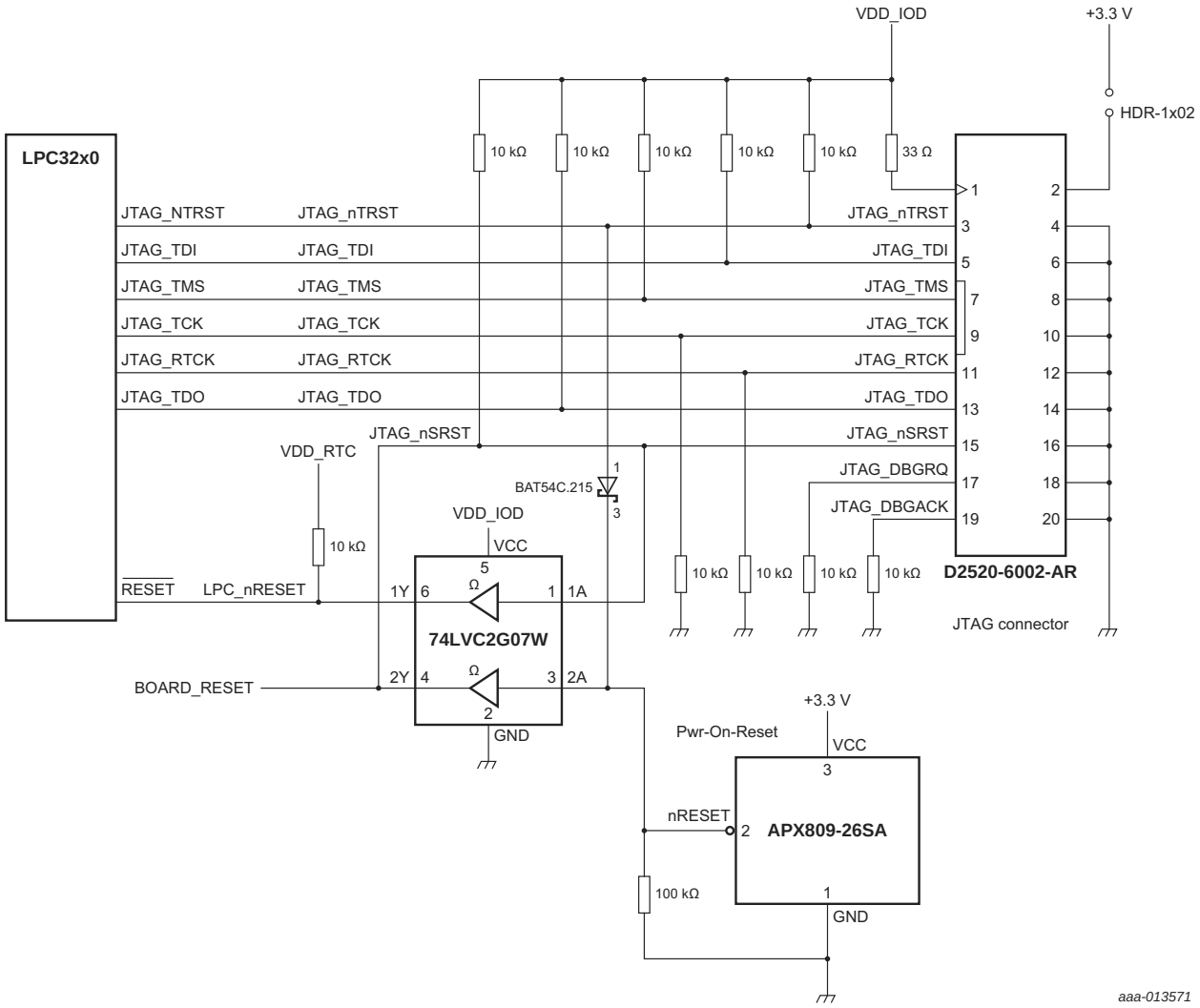


Fig 24. Circuit for holding JTAG_NTRST LOW during POR

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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